General Standards Corporation

High Performance Bus Interface Solutions

Rev: 081620

PCIe-24DSI64C200K

24-Bit, 64-Channel, 250KSPS, PCI-Express Module

With 64 Differential Delta-Sigma Input Channels

REFERENCE MANUAL

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SECTION 1.0

INTRODUCTION

1.1 General Description

The PCIe-24DSI64C200K provides 24-bit analog input capability for the PCIe bus at sample rates up to 250 KSPS per channel. In addition to providing 64 differential analog input channels, this product supports multiboard clocking and synchronization. The board is functionally and mechanically compatible with the PCI Express Specification revision 1.0a. Power requirements consist of +3.3 VDC and +12 VDC in accordance with the PCI Express specification, and operation over the specified temperature range is achieved with conventional air cooling. Specific details pertaining to physical characteristics and performance are provided in the PCIe-24DSI64C200K product specification.

This product is designed for minimum off-line maintenance, and includes internal monitoring features that eliminate the need for disconnecting or removing the module from the system for calibration. All system input and output connections are made at the panel bracket through two high-density system I/O connectors. Figure 1.1-1 shows the physical configuration of the board.

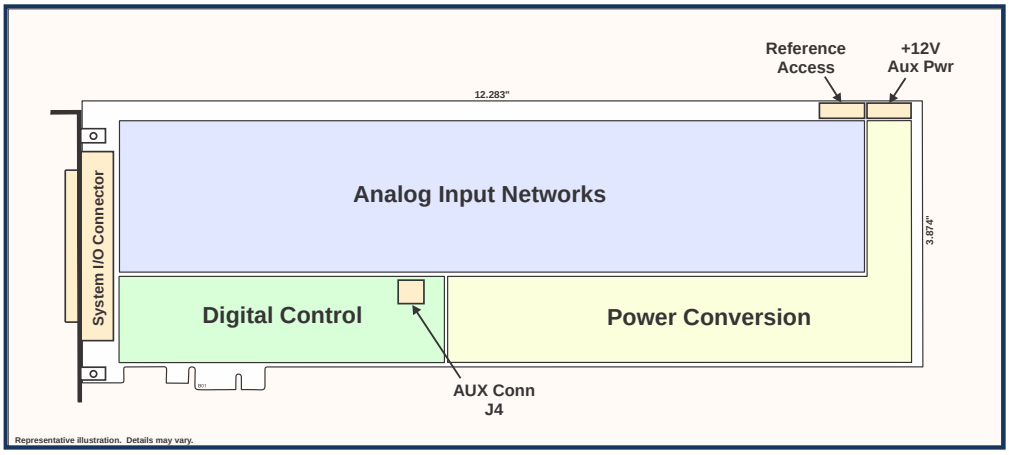

Figure 1.1-1. Physical Configuration

1.2 Functional Overview

A PCI Express interface adapter provides the interface between the controlling bus and the internal local controller through a 32-bit local bus (Figure 1.2-1). Inputs are organized into eight channel groups, any of which can be designated as either active or inactive independently of the other groups. Each input channel contains selftest switches for selftest and autocalibration operations, as well as a low-order lowpass analog image filter. Each channel also contains a 24-bit delta-sigma A/D converter (ADC) that generates serial input data for the local controller. An internal voltage reference can be applied to all channels to support selftest operations and autocalibration. Gain and offset trimming of the input channels is performed by applying correction values obtained during autocalibration.

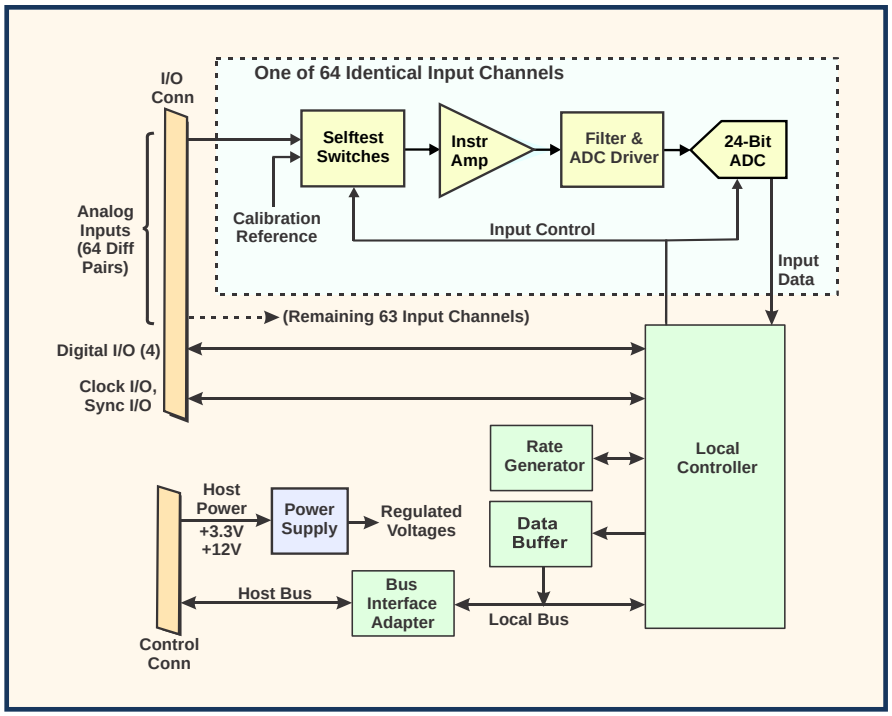

Figure 1.2-1. Functional Organization

An internal sample-rate clock generator is adjustable from 34 MHz to 68 MHz, and is divided down within the local controller to provide sample rates from 1.0 KSPS to 250 KSPS. Triggered acquisition bursts are supported. Input bandwidth varies from approximately 500 Hz to 110 kHz, depending upon the selected sample rate, and extends down to DC. Conversion data from all active channels is transferred to the PCI Express bus through a 256K-sample FIFO data buffer.

Multiple channels or boards can be synchronized to perform sampling in "lockstep", either by a software command, or by external hardware sync and clock input signals. Hardware sync and clock input/output signals permit multiple boards to be connected together for phase-locked operation from a common clock.

SECTION 2.0
INSTALLATION AND MAINTENANCE

2.1 Board Configuration

This product has no field-alterable configuration features, and is completely configured at the factory for field use.

2.2 Installation

2.2.1 Physical Installation

To minimize the opportunity for accidental damage before installation, the board should be stored in the original protective shipping envelope. System power must be turned OFF before proceeding with the installation.

CAUTION: This product is susceptible to damage from electrostatic discharge (ESD). Before removing the board from the conductive shipping envelope, ensure that the work surface, the installer and the host system are adequately discharged to ground.

Before removing the board from the protective shipping envelope, select an empty 1-lane or greater PCI Express slot in the host computer and, if a blank panel bracket is located in the slot position, remove the bracket. Then remove the board from the shipping envelope and position the board with the panel bracket oriented toward the expansion panel opening. Align the board's PCI Express edge-connector with the mating connector on the motherboard, and carefully press the board into position. Verify that the connector has mated completely, and that the panel bracket is seated against the fastener bracket above the panel opening. To complete the installation, secure the panel bracket with an appropriate machine or panhead screw; do not overtighten.

2.2.2 Input/Output Cable Connections

System cable signal pin assignments are listed in Table 2.2.2-1 and shown in Figure 2.2.2-1. Unused input pins may be left disconnected in most applications. However, if very long cables are used or if excessive cable noise is anticipated, the unused analog inputs should be grounded to the input return to minimize the injection of noise into the board.

Each of the two 85-Pin system I/O connectors is intended to mate with a cable containing 42 twisted wire pairs, terminated with an Omnetics connector #MNPO-85-DD-N-EJS-C. Contact General Standards with specific requirements.

An internal auxiliary sync connector shown in Figure 1.1-1 and Table 2.2.2-2 supports the synchronization of multiple boards using behind-the-panel cabling.

Table 2.2.2-1. System Connector Pin Assignments

P4				P3			
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
43	DGND	---	---	43	DGND	---	---
42	DGND	85	DGND	42	DGND	85	DIO_00
41	CLK_INP_LO	84	CLK_INP_HI	41	DGND	84	DIO_01
40	CLK_OUT_LO	83	CLK_OUT_HI	40	DGND	83	DIO_02
39	SYNC_INP_LO	82	SYNC_INP_HI	39	DGND	82	DIO_03
38	SYNC_OUT_LO	81	SYNC_OUT_HI	38	DGND	81	DGND
37	AGND	80	AGND	37	AGND	80	AGND
36	IN_LO_00	79	IN_HI_00	36	IN_LO_32	79	IN_HI_32
35	IN_LO_01	78	IN_HI_01	35	IN_LO_33	78	IN_HI_33
34	IN_LO_02	77	IN_HI_02	34	IN_LO_34	77	IN_HI_34
33	IN_LO_03	76	IN_HI_03	33	IN_LO_35	76	IN_HI_35
32	IN_LO_04	75	IN_HI_04	32	IN_LO_36	75	IN_HI_36
31	IN_LO_05	74	IN_HI_05	31	IN_LO_37	74	IN_HI_37
30	IN_LO_06	73	IN_HI_06	30	IN_LO_38	73	IN_HI_38
29	IN_LO_07	72	IN_HI_07	29	IN_LO_39	72	IN_HI_39
28	AGND	71	AGND	28	AGND	71	AGND
27	IN_LO_08	70	IN_HI_08	27	IN_LO_40	70	IN_HI_40
26	IN_LO_09	69	IN_HI_09	26	IN_LO_41	69	IN_HI_41
25	IN_LO_10	68	IN_HI_10	25	IN_LO_42	68	IN_HI_42
24	IN_LO_11	67	IN_HI_11	24	IN_LO_43	67	IN_HI_43
23	IN_LO_12	66	IN_HI_12	23	IN_LO_44	66	IN_HI_44
22	IN_LO_13	65	IN_HI_13	22	IN_LO_45	65	IN_HI_45
21	IN_LO_14	64	IN_HI_14	21	IN_LO_46	64	IN_HI_46
20	IN_LO_15	63	IN_HI_15	20	IN_LO_47	63	IN_HI_47
19	AGND	62	AGND	19	AGND	62	AGND
18	IN_LO_16	61	IN_HI_16	18	IN_LO_48	61	IN_HI_48
17	IN_LO_17	60	IN_HI_17	17	IN_LO_49	60	IN_HI_49
16	IN_LO_18	59	IN_HI_18	16	IN_LO_50	59	IN_HI_50
15	IN_LO_19	58	IN_HI_19	15	IN_LO_51	58	IN_HI_51
14	IN_LO_20	57	IN_HI_20	14	IN_LO_52	57	IN_HI_52
13	IN_LO_21	56	IN_HI_21	13	IN_LO_53	56	IN_HI_53
12	IN_LO_22	55	IN_HI_22	12	IN_LO_54	55	IN_HI_54
11	IN_LO_23	54	IN_HI_23	11	IN_LO_55	54	IN_HI_55
10	AGND	53	AGND	10	AGND	53	AGND
9	IN_LO_24	52	IN_HI_24	9	IN_LO_56	52	IN_HI_56
8	IN_LO_25	51	IN_HI_25	8	IN_LO_57	51	IN_HI_57
7	IN_LO_26	50	IN_HI_26	7	IN_LO_58	50	IN_HI_58
6	IN_LO_27	49	IN_HI_27	6	IN_LO_59	49	IN_HI_59
5	IN_LO_28	48	IN_HI_28	5	IN_LO_60	48	IN_HI_60
4	IN_LO_29	47	IN_HI_29	4	IN_LO_61	47	IN_HI_61
3	IN_LO_30	46	IN_HI_30	3	IN_LO_62	46	IN_HI_62
2	IN_LO_31	45	IN_HI_31	2	IN_LO_63	45	IN_HI_63
1	AGND	44	AGND	1	AGND	44	AGND

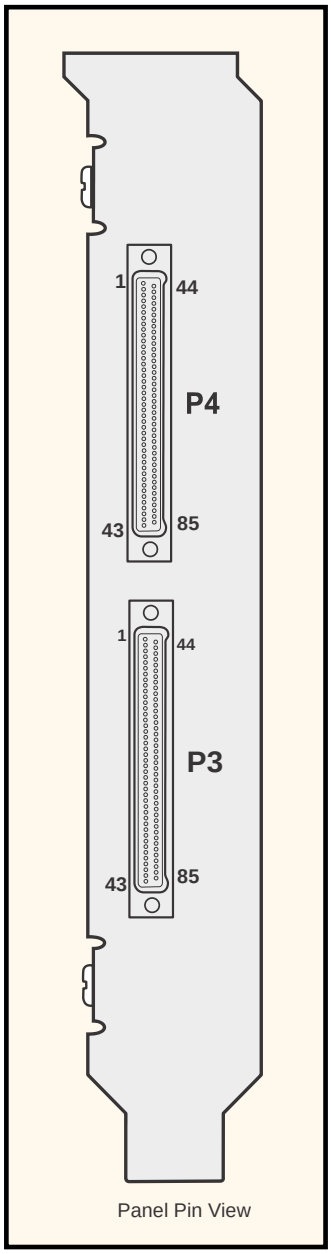

Figure 2.2.2-1. Panel Bracket

Table 2.2.2-2. Aux Sync I/O Connector

Pin	Signal
1	DIGITAL RTN
2	AUX CLOCK
3	DIGITAL RTN
4	AUX SYNC
5	DIGITAL RTN
6	Reserved. Ground or leave disconnected.

2.3 Analog Input Configuration

The analog inputs are configured as 64 differential input pairs. Differential operation provides the highest noise immunity, and is recommended for the majority of applications. Pull-down resistors are provided on all analog inputs. Although the input configuration is differential, single-ended signal sources can be accommodated (2.3.2).

2.3.1 Differential Inputs

Differential operation is essential when the input source returns are at different potentials. This operating mode also offers the highest rejection of the common mode noise that is characteristic of long unshielded cables. When operating in the differential mode, shown in Figure 2.3.1a, the wire pair from each signal source is connected between the HI(+) and LO(-) inputs of a single input channel. The input return should be connected to system ground (remote common) as closely as possible to the input sources. The average HI/LO signal level relative to the input return is the common mode voltage **Vcm,** which must not exceed the maximum value indicated in the product specification.

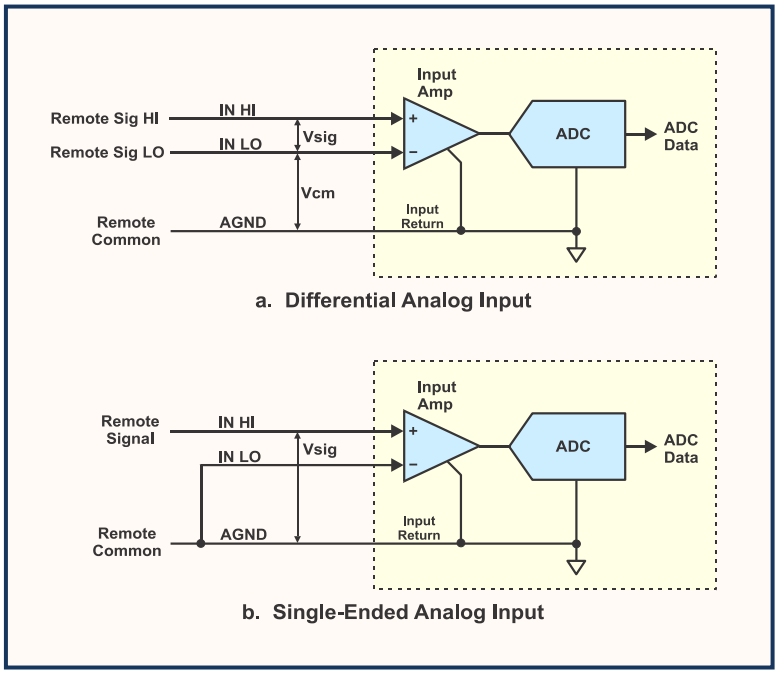

Figure 2.3.1-1. Analog Input Configurations

2.3.2 Single-Ended Input Sources

Single-ended signal sources can be accommodated as shown in Figure 2.3.1-1b, with the signal line connected to INP HI xx, and the associated INP LO xx input connected to Remote Common at the source, and to AGND at the board connector. The single-ended operating connection provides suitable performance only when the input signal sources either are isolated from each other, or are common only to a single isolated signal return.

CAUTION: If a significant potential difference exists between the remote common and the AGND pin at the board, a low impedance between the two returns can cause excessive current to flow, which in turn can cause erroneous measurements or possible damage to the board. Return-current should be controlled to less than a few milliamps for best performance, and to less than 100 milliamps to avoid damage.

2.4 Multiboard Clocking and Synchronization

Analog input converters on multiple boards can be:

a. Clocked from a single clock source (Multiboard clocking), and/or:

b. Synchronized to a common time reference (Multiboard synchronization).

Clocking multiple converters from a single source prevents the *sampling drift* that occurs when converters are clocked from different sources. *Synchronizing* the converters on multiple boards causes the converters to initiate conversions simultaneously, and can be used to eliminate *sampling skew* between channels.

Clock and Sync I/O lines support the synchronization of conversion clocking and burst triggering among multiple boards in an initiator-target configuration (Figure 2.4.1-1), and allow these functions to be controlled by external signal sources. The Clock/Sync interface can be software-configured for differential LVDS Clock and sync signaling or for TTL signaling. TTL inputs are pulled up to +3.3 Volts internally through 5 K-Ohms. Maximum TTL output loading is 8 milliamps.

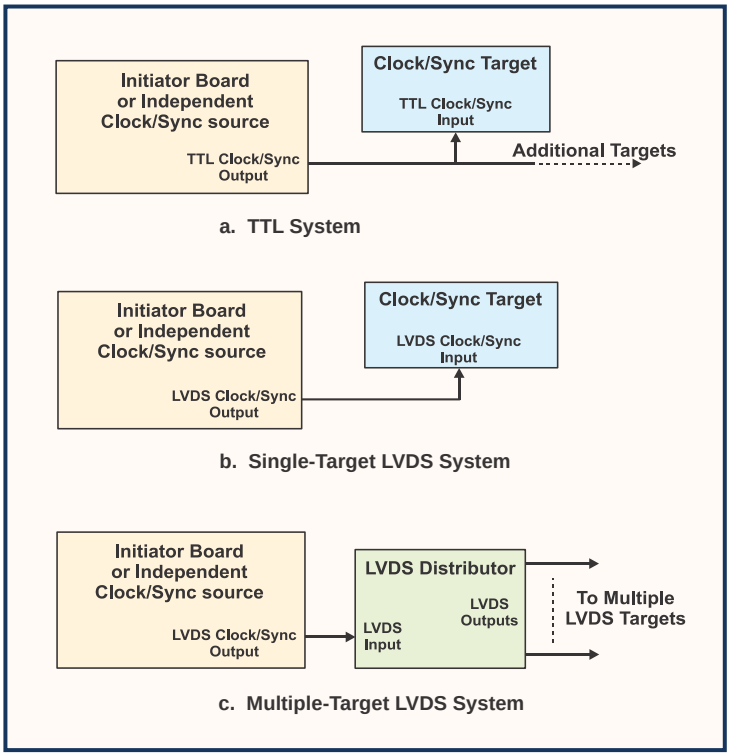

Figure 2.4.1-1. Multiboard Clock and Sync Connections

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2.4.1 Interboard Connections

Multiple PCIe-24DSI64C200K boards can be interconnected in an initiator-target sequence to provide common clocking between boards. An initiator can directly control up to four target boards (Figure 2.4.1-1a) using TTL signaling, if total cable length is 50 centimeters (20 inches) or less. An LVDS initiator can directly control a single target (Figure 2.4.1-1b), or can control multiple LVDS targets through an LVDS distributor in a 'Star' configuration. LVDS signaling is effective up to several meters at the frequencies involved in the synchronization of multiple PCIe-24DSI64C20K boards. Application software controls the designation of each board as an initiator or a target.

NOTE: Multiple targets also could be interconnected in a daisy-chain fashion, with the Clock and Sync outputs from each target driving the Clock inputs of the next target in the chain. The disadvantage of this scheme is the accumulation of delays introduced by multiple boards.

The clock output signal is generated internally on an initiator board, or is a duplicate of the clock input signal on a target board. Similarly, the sync output is the software-generated sync signal on an initiator board, or a duplicate of the sync input signal on a target board.

NOTE: External clock and sync inputs can be provided from external sources other than an initiator board.

NOTE: An auxiliary clock and sync connector (Table 2.2.2-2) supports interboard clock and sync connections behind the front panel.

2.4.2 Multiboard Synchronization

Boards that are daisy-chained together for multiboard synchronization initiate internal *synchronization sequences* each time a sync pulse is generated by the initiator board. The sequence has a duration of approximately 100 milliseconds, after which all synchronized channels operating from a common clock will sample their inputs simultaneously.

The SYNC I/O line can also be used to reset (clear) the data buffers on target boards.

2.5 Maintenance

This product requires no scheduled hardware maintenance other than periodic reference verification. The optimum adjustment interval will vary, depending upon the specific application, but in most instances an interval of one year is recommended. In the event of a suspected malfunction, all associated system parameters, such as I/O cabling, power voltages, and control bus integrity should be evaluated before a board is returned to the factory for problem analysis and repair.

2.6 Reference Verification and Adjustment

All input and output channels are software-calibrated to an internal voltage reference by an embedded autocalibration software utility. This procedure describes the adjustment of the internal reference. For applications in which the system must not be powered down, the adjustment can be performed while the board is installed in an operating system.

2.6.1 Equipment Required

Table 2.6.1-1 lists the equipment requirements for calibrating the PCIe-24DSI64C200K board. Alternative equivalent equipment may be used.

Table 2.6.1-1. Reference Adjustment Equipment

Equipment Description	Manufacturer	Model
Digital Multimeter, 5-1/2 digit, 0.005% accuracy for DC voltage measurements at +10 Volts.	Hewlett Packard	34401A
Host system with PCIe expansion slot.	---	---
Test leads, as required.	---	---

2.6.2 Adjustment Procedure

The following procedure describes the single adjustment that is necessary to ensure conformance to the product specification. Adjustment of the internal reference (Vtest) is performed with an internal trimmer that is accessible at the top of the board, as shown in Figure 1.1-1. This procedure assumes that the board is installed in an operating system.

1. Connect the digital multimeter (DMM) between Pin-3 (+) and Pin-4(-) of the J5 test connector located at the top of the board in the area indicated as 'Reference Access' in Figure 1.21.

2. If power has been removed from the board, apply power now and wait at least 15 minutes before proceeding.

3. Identify the installed input range indicated in Table 3.10-1. The DMM indication should display the voltage indicated for the range as:

   *±10V => +9.9000 VDC ±0.0007 VDC

   ±5V => +4.9500 VDC ±0.0005 VDC

   ±2.5V => +2.4750 VDC ±0.0004 VDC

   ±2V => +1.9800 VDC ±0.0004 VDC

   *±1.5V => +1.4850 VDC ±0.0003 VDC

   ±1V => +0.9900 VDC ±0.0003 VDC

   If the DMM indication does not conform to the associated test limits, adjust the reference adjustment trimmer adjacent to J5 until the indication is within the specified limits.

   *The ±10V and ±1.5V ranges are the only non-custom ranges

SECTION 3.0

CONTROL SOFTWARE

3.1 Introduction

The PCIe-24DSI64C200K board is compatible with the PCI Express local bus specification revision 1.0a, and a PLX^{tm} PEX8311 adapter controls the one-lane interface. Configuration-space registers are initialized internally to support the location of the board on any 16-longword boundary in memory space.

After initialization, communication between the PCIe bus and the board takes place through the control and data registers shown in Table 3.1. All data transfers are long-word D32. Reserved bits in each register are ignored during write operations, and are forced LOW during read operations. To ensure compatibility of applications with subsequent product upgrades, reserved bits should be written LOW.

Table 3.1-1. Control and Data Registers

Local Addr	Mode	Designation	Default	Description	Ref
00	R/W	**Board Control (BCR)**	0000 3830h	Board Control Register (BCR)	3.2
04	R/W	**Rate-A Generator Control**	0028 0037h	PLL reference oscillator control integers.	3.6.4
08	R/W	**Digital I/O Port**	0000 000Xh	Digital I/O Port control	3.12
0C	R/W	**Analog Input Configuration**	0002 20FFh	Analog input sampling parameters	3.4
10-14	RO	**(Reserved)**	0000 0000h	---	---
18	RW	**Burst Block Size**	0000 0001h	Specifies the number of sample sets to be acquired in a triggered burst	3.11
1C	R/W	**Burst Trigger Timer**	0000 C000h	Internal trigger timer rate divisor	3.11
20	R/W	**Buffer Control**	0X03 FFFEh	Input buffer control and status	3.5.3
24	RO	**Board Configuration**	00XX XXXXh	Installed firmware and hardware options	3.10
28	RO	**Buffer Size**	0XXX XXXXh	Number of ADC values in the input buffer.	3.5.4
2C	RO	Autocal Values [1]	---	---	---
30	RO [2]	**Input Data Buffer**	XXXX XXXXh	Input Data Buffer; Data and channel tag	3.5
34	R/W	**Aux Sync I/O Register**	0000 0000hh	Auxiliary clock and sync I/O port	3.14
38-3C	--	(Reserved)	---	---	--

[1] Maintenance register shown for reference only. [2] DMA access.

3.2 Board Control Register

The Board Control Register (BCR) controls primary board functions, including analog input mode and input range selections, and consists of 32 control bits and status flags (Table 3.2). Control and monitoring functions of the BCR are described in detail throughout the remainder of this section.

Table 3.2-1. Board Control Register

Offset: 0000h **Default: 0000 3830h**

Data Bit	Mode	Designation	Def	Description	Ref
D00-D01	R/W	AIM[1..0]	0	Analog input mode. Selects system inputs or selftest mode. Defaults to system inputs.	3.4
D02-D03	R/W	(Reserved)	0	---	---
D04	R/W	OFFSET BINARY	1	Selects offset binary or two's complement input data format. Defaults HIGH to offset binary.	3.5.2
D05	R/W	INITIATOR	1	Selects INITIATOR or TARGET mode for external clock and sync signals. Defaults HIGH to Initiator mode.	3.6.7
D06	R/W	* SYNCHRONIZE INPUTS	0	Initiates a local ADC sync operation when asserted. Also generates an external sync output if INITIATOR mode is selected. Clears automatically.	3.6.6 3.6.7.2 3.6.9
D07	R/W	* AUTOCAL	0	Initiates an autocalibration operation when asserted. Clears automatically upon autocal completion.	3.7
D08-D10	R/W	INTERRUPT A[2..0]	0	Interrupt event selection. Default is zero.	3.8
D11	R/W	INTERRUPT REQUEST FLAG	1	Set HIGH when the board requests an interrupt. Clears the request when cleared LOW by the bus.	
D12	RO	AUTOCAL PASS	1	Set HIGH at reset or autocal initialization. Cleared LOW if autocalibration terminates unsuccessfully.	3.7
D13	RO	CHANNELS READY	1	LOW during any change in channel parameters. Asserted HIGH when inputs are ready to acquire data.	3.4.3
D14	RO	BUFFER THRESHOLD FLAG	0	Asserted HIGH when buffer contents exceed the assigned threshold.	3.5.3.1
D15	R/W	* INITIALIZE	0	Initializes the board when asserted. Sets all defaults.	3.3.2
D16	R/W	ENABLE TRIGGER TIMER	0	Enables the internal burst trigger timer.	3.11.2
D17	R/W	CLEAR BUFFER ON SYNC	0	When this bit is HIGH, the context of the SYNCHRONIZE INPUTS control bit changes to CLEAR BUFFER.	3.5.3.2 3.6.7.2
D18	R/W	RATE-A CLOCK OUT (Initiator Mode only)	0	When HIGH, selects the internal Rate-A generator as the external clock output source. When LOW, selects the ADC master clock Mclk as the output.	3.6.7.1
D19	R/W	* INITIALIZE ADCS	0	Initializes (resets) all local ADCs.	3.6.10
D20	R/W	(Reserved)	0	---	---
D21	R/W	TTL EXTERNAL SYNC I/O	0	Selects TTL external sync I/O configuration.	3.6.7
D22	R/W	ENABLE INPUT BURST	0	Selects triggered-burst acquisition when HIGH.	3.11
D23	R/W	S/W BURST TRIGGER	0	Initiates a triggered burst when asserted. Forced HIGH during any triggered burst.	
D24-D31	RO	(Reserved)	- 0 -	---	---

* Clears automatically.

3.3 Configuration and Initialization

3.3.1 Control Logic Configuration

Configuration is initiated by a PCI Express bus RESET, and should be required only once after the initial application of power. During board configuration, initial values for both the PCIe configuration registers and the internal control logic are extracted from internal nonvolatile read-only memory. Configuration operations are executed in the sequence shown in Table 3.3.1-1.

Table 3.3.1-1. Configuration Operations

Operation	Duration
PCI configuration registers are loaded from internal EEPROM	3 ms
Internal control logic is configured from internal ROM	100 ms
Internal control logic is initialized	3 ms
A/D converters and clocks are initialized	200 ms

Board configuration terminates with the PCI Express interrupts disabled. Attempts to access the local bus during configuration should be avoided until the interrupt is enabled and the initialization-complete interrupt request is asserted.

3.3.2 Initialization

Internal control logic can be initialized without invoking configuration by setting the INITIALIZE control bit HIGH in the BCR. This action causes the internal logic to be initialized, but does not affect the PCI Express configuration registers, and does not reconfigure the internal control logic. Initialization has a maximum duration of 0.4 seconds, and produces the following conditions:

- All control registers are initialized; all defaults are invoked. (3.1).
- Input buffer is reset to empty and disabled. (3.5.3).
- Buffer threshold equals 0003 FFFEh. (3.5.3).
- The width of the buffer data field is adjusted to 16 bits. 3.5.3).
- Internal rate generator frequency is 45.056 MHz. (3.6.4).
- Selected sample rate is 44.000 KSPS. (3.6.4).
- The Initiator mode is selected. (3.6.7).
- External clock output is the ADC modulator clock Mclk. (3.6.7.1).
- The internal rate generator is the ADC clock source. 3.6.7.1).
- All ADCs are initialized. (3.6.10).
- The local interrupt request is asserted as an initialization-completed event. (3.8).
- Triggered-burst rate is 1.000 kHz; Burst block size is 1. (3.11)

Upon completion of initialization, the INITIALIZE control bit is cleared automatically.

3.4 Analog Input Configuration

Configuration of the analog input networks is controlled by the BCR control bits designated as AIM[1..0], the effects of which are summarized in Table 3.4-1. The analog input selection arranges all input channels in differential configuration during normal operation, or invokes one of two selftest modes.

Table 3.4-1. Analog Input Function Selection

Aim[1..0]	Function or Mode
0	Differential analog input mode.
1	(Reserved).
2	ZERO test. Internal ground reference is connected to all analog input channels.
3	+VREF test. Internal voltage reference is connected to all analog input channels.

3.4.1 Input Range

The analog input range is factory configured to one of the range options listed in the product specification. The assigned range is identified in the Board Configuration register (3.10).

3.4.2 Selftest Modes

Two selftest modes provide the ability to verify the accuracy of any or all input channels by replacing the system input connections with either a precision internal reference voltage (+VREF) or a zero reference (ZERO). The +VREF test produces a positive value equal to 99.00 percent of the selected input range (e.g. +9.900 Volts for the ±10 Volt range) from all input channels, and the ZERO test should produce a value of 0.000 Volts. The accuracy of selftest measurements should correspond to the product accuracy specification.

NOTE: For maximum test accuracy, the internal reference voltage must be allowed to settle completely when the test mode is changed. After selecting either of the selftest modes, insert a 100 millisecond delay before acquiring test values.

3.4.3 Settling Delays and the Channels Ready Flag

When a critical parameter such as input mode or sample rate is changed, a settling transition occurs during which input measurements are unpredictable. A settling delay is inserted automatically when any or all of these parameters are changed, and the CHANNELS READY status flag in the BCR goes LOW during the delay. Both LOW-to-HIGH and HIGH-to-LOW transitions of this flag are selectable as interrupt request "channels ready" events (Section 3.8.1). The CHANNELS READY flag goes low during the following operations for the approximate maximum intervals and filter-selections indicated (3.6.8):

Wideband Filter (3.6.8):	Low-Latency Filter (3.6.8):	
400 ms	**---**	*Board initialization (3.3),*
3 ms	**3 ms**	*Buffer reset (3.5.3.2) or Buffer enable/disable (3.5.3.2),*
100 ms	**10 ms**	▪ *Sample rate change (3.6.3, 3.6.4).* ▪ *Write-access to the Analog Input Configuration register (3.6).* ▪ *Inputs synchronization (3.6.6) or ADC initialization (3.6.10).*

3.5 Input Data Buffer

3.5.1 General Characteristics

Analog input samples accumulate in the analog input data FIFO data buffer, which has a capacity of 256K (262,144) data values. Data accumulates in the buffer until extracted by the host bus from a single register location listed in Table 3.1-1. Reading an empty buffer returns an indeterminate value.

3.5.2 Data Organization

Each value in the data buffer consists of a 6-bit channel tag field, a zero-pad field, and a data field, as shown in Table 3.5.2-1. The width of the right-justified data field is adjustable from 16 bits to 24 bits by the buffer control register (Table 3.5.3-1), and the width of the zero-pad field is adjusted accordingly. The Data Zero-pad field becomes a sign-extension field if two's complement data coding is selected.

Table 3.5.2-1. Input Data Buffer Organization

Offset: 0000 0030h **Default: XXXX XXXXh**

Data Width (Bits)	Reserved (All-zero)	Channel Tag	Data Zero-Pad *	Data Value
16	D[31..30]	D[29..24]	D[23..16]	D[15..0]
18	D[31..30]	D[29..24]	D[23..18]	D[17..0]
20	D[31..30]	D[29..24]	D[23..20]	D[19..0]
24	D[31..30]	D[29..24]	---	D[23..0]

* Sign extension field if Two's Complement coding is selected.

Input data values can be represented either in offset binary format by asserting the OFFSET BINARY control bit HIGH (default state) in the BCR, or in two's complement format by clearing the control bit LOW. Both coding conventions are illustrated for 16-Bit data in Table 3.5.2.2-1.

Table 3.5.2.2-1. Analog Input Data Coding; 16-Bit Data Field

	Digital Value (Hex)	
Analog Input Level	**Offset Binary**	**Two's Complement**
Positive Full Scale minus 1 LSB	FFFFh	7FFFh
Zero plus 1 LSB	8001h	0001h
Zero	8000h	0000h
Zero minus 1 LSB	7FFFh	FFFFh
Negative Full Scale plus 1 LSB	0001h	8001h
Negative Full Scale	0000h	8000h

Positive Full Scale is a positive level that equals the selected input voltage range for the board (e.g.: +10.000 Volts for the ±10V range). *Negative Full Scale* is the negative equivalent of positive full-scale. *Full-scale Range* (FSR*)* is the total input voltage range. For 16-Bit data, one LSB equals the full-scale range divided by 65,536. (e.g.: 305.175 microvolts for the ±10V range).

3.5.3 Buffer Control Register

The buffer control register (Table 3.5.3-1) contains the threshold value for the buffer status flag, and also provides control bits for clearing the buffer and for disabling the buffer input.

Table 3.5.3-1. Buffer Control Register

Offset: 0000 0020h **Default: 0X03 FFFEh**

Bit Field	Mode	Designation	Def	Function
D00-D18	R/W	BUFFER THRESHOLD	3 FFFEh	Buffer Flag Threshold
D19	R/W	ENABLE BUFFER INPUT	0	Enables inputs to the buffer
D20	R/W	CLEAR BUFFER *	0	Clears (empties) the buffer
D21-D22	R/W	DATA WIDTH	0	Controls the width of the buffer data field as: 0 => 16 bits 1 => 18 bits 2 => 20 bits 3 => 24 bits.
D23	R/W	(Reserved)	0	---
D24	R/W	BUFFER OVERFLOW **	0	Reports buffer overflow (Write on full)
D25	R/W	BUFFER UNDERFLOW **	0	Reports buffer underflow (Read on empty)
D26-D31	RO	(Reserved)	0h	---

* Clears automatically. ** Clear by writing LOW, or by board reset.

3.5.3.1 Threshold and Status Flag

The amount of data contained in the input buffer can be used to control the BUFFER THRESHOLD FLAG status bit, which can be selected as an interrupt request event. The interrupt request event can be selected to occur on either the rising or falling edge of the flag (Table 3.8.1-1).

The threshold flag is asserted HIGH when the number of samples in the buffer ***exceeds*** the BUFFER THRESHOLD value in the buffer control register. A buffer-empty event is produced when the threshold value is adjusted to equal 0000 0000h and the threshold flag undergoes a HIGH-to-LOW transition.

3.5.3.2 Buffer Clearing and Disabling

Asserting the CLEAR BUFFER control bit in the buffer control register resets (empties) the buffer. This control bit clears automatically. To prevent a partial sample set from entering the buffer after the Clear signal is removed, the buffer is maintained in the Clear state until the last channel in a sample set is detected. For this reason, the buffer clearing interval can be as long as 3 milliseconds at very low sample rates.

NOTE: The buffer can be cleared also by writing a "one" to the SYNCHRONIZE INPUTS control bit in the BCR when the CLEAR BUFFER ON SYNC control bit is HIGH.

Asserting the ENABLE BUFFER INPUT control bit HIGH enables inputs to the buffer from the ADC input channels, and allows the accumulation of input data. Clearing the control bit LOW disables inputs to the buffer. Data already present in the buffer when this bit is cleared remains in the buffer.

Buffer enabling and disabling operations both are synchronous with the input data stream. That is, regardless of when the enabling control bit is set or cleared, actual enabling of the buffer always occurs immediately prior to a complete sample set arriving, and disabling always occurs immediately after the last active channel in a sample set is loaded into the buffer.

NOTE: Because delta-sigma ADC's perform conversions continuously, the initiation and termination of acquisition sequences are controlled by the buffer's 'Clear' and 'Enable' controls.

3.5.4 Buffer Size Register

This read-only register (Table 3.5.4-1) reports the number of analog input values currently stored in the input data buffer.

Table 3.5.4-1. Buffer Size Register

Offset: 0000 0028h **Default: XXXX XXXXh**

Bit Field	Mode	Designation	Function
D00-D18	RO	BUFFER SIZE [00..18]	Number of sample values contained in the input buffer.
D19-D31	RO	(Reserved)	---

3.5.5 Overflow and Underflow Flags

BUFFER OVERFLOW and BUFFER UNDERFLOW status bits in the buffer control register report overflow (write on full) or underflow (read on empty) events. Once set, these status bits remain HIGH until cleared by writing them LOW directly, or by a board initialization sequence.

3.6 Input Sampling Control

The Analog Input Configuration register (Table 3.6-1) controls the analog input configuration and sampling parameters:

Table 3.6-1. Analog Input Configuration Register

Offset: 000Ch **Default: 0002 20FFh**

Bit Field	Mode	Designation	Def	Function	Ref
D00	R/W	CHAN GROUP 0 ACTIVE	1	Channel Group-0 Active (Chan 00-07)	3.6.1
D01	R/W	CHAN GROUP 1 ACTIVE	1	Channel Group-1 Active (Chan 08-15)	
D02	R/W	CHAN GROUP 2 ACTIVE	1	Channel Group-2 Active (Chan 16-23)	
D03	R/W	CHAN GROUP 3 ACTIVE	1	Channel Group-3 Active (Chan 24-31)	
D04	R/W	CHAN GROUP 4 ACTIVE	1	Channel Group-4 Active (Chan 32-39)	
D05	R/W	CHAN GROUP 5 ACTIVE	1	Channel Group-5 Active (Chan 40-47)	
D06	R/W	CHAN GROUP 6 ACTIVE	1	Channel Group-6 Active (Chan 48-55)	
D07	R/W	CHAN GROUP 7 ACTIVE	1	Channel Group-7 Active (Chan 56-63)	
D08-D11	R/W	FGEN_DIV_SLCT	0	Selects the Fgen divisor FGEN_DIV: 0 => ÷1 1 => ÷2 2 => ÷4 3 => ÷8 4 => ÷16 5-15 => (Reserved)	3.6.3
D12-D15	R/W	MCLK_DIV_SLCT	2	Selects the Mclk divisor MCLK_DIV: 0 => ÷32 ('Eco' mode: Lowest bandwidth, lowest power) 1 => ÷8 ('Median' mode: Intermed bandwidth and power) 2 => ÷4 ('Fast' mode: Highest bandwidth, Max power) 3-15 => (Reserved)	3.6.3
D16-D19	R/W	OSF_SLCT	2	Selects the Oversampling factor (Decimation rate): 0 => OSF= 32 1 => OSF= 64 2 => OSF= 128 3 => OSF= 1024 4-15 => (Reserved)	3.6.3
D20-D21	R/W	CLOCK SOURCE	0	Selects the ADC clocking source: 0 => Internal Rate-A generator 1 => External Fgen Input. (Through the Fgen divider) 2 => External Mclk Input. (Routed directly to the ADC mclk inputs). 3 => (Reserved)	3.6.2 3.6.5
D22	R/W	SYNC SOURCE	0	Selects the Sync source: 0 => Internal trigger timer, or BCR sync. 1 => External Sync/Trigger Input, or BCR sync.	3.6.6 3.11
D23	R/W	LOW LATENCY FILTER	0	Selects the Low Latency filter if HIGH, or the Wideband Low-Ripple filter if LOW.	3.6.10
D24-D31	R/W	(Reserved)	- 0 -	---	---

* Clears automatically

3.6.1 Active Channel Assignments

The analog inputs are partitioned into groups of eight channels, with eight groups available on a 64-Channel board. Each group can be independently assigned either active or inactive status, and all active groups operate at the same sample rate. A group is designated as ***active*** by asserting the associated CHAN GROUP x ACTIVE control bit HIGH in the Analog Input Configuration register, or as **inactive** by clearing the bit LOW. Only active groups provide data to the input buffer, and all groups default to active status upon initialization.

3.6.2 Sample Clock Frequency Source

Sample rates are derived either from an adjustable internal Rate-A generator as the source when HIGH, or the external clock input when LOW,

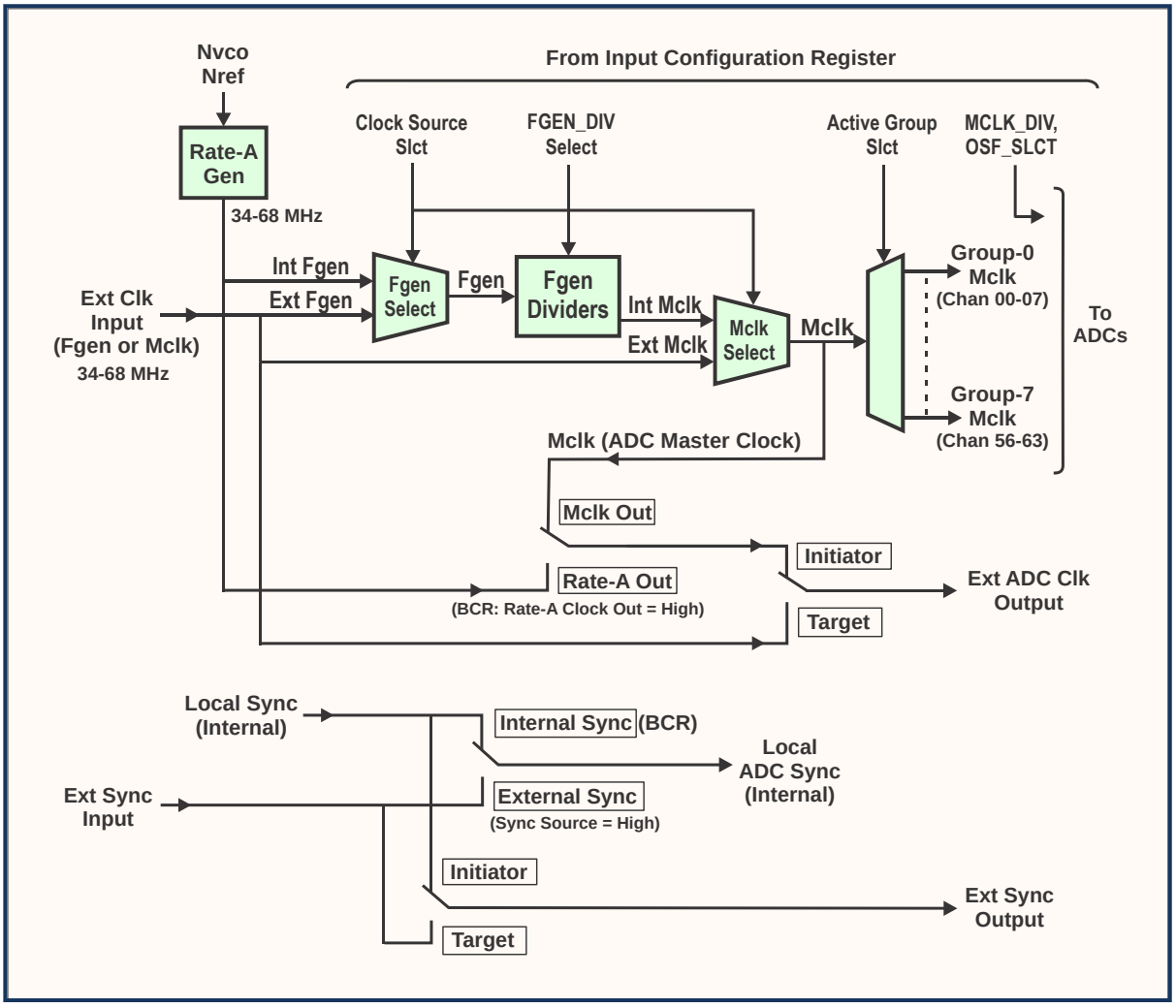

Figure 3.6.2-1. Clock and Sync Organization

The selected source **Fgen** is processed further to obtain the required sampling parameters, including the ADC master clock **Mclk** which is then distributed to the active analog input groups. Using **Mclk** as a local master clock, each ADC applies the MCLK_DIV and OSF_SLCT parameters to establish the final sample rate, power level and oversampling factor, as shown in Figure 3.6.3-1. MCLK_DIV and OSF_SLCT are distributed unconditionally to all analog input groups, but affect only active groups.

NOTE: In order to associate text in this document with related references in data sheets and other documents, the following terms are used interchangeably:

- **'Mclk' and 'ADC Master Clock',**
- **'Fmod' and 'ADC Modulator Clock' or 'ADC Sampling Clock',**
- **'Sample Rate' (Fsamp) and 'Output Data Rate' (ODR),**
- **'Oversampling Factor' (OSF) and 'Decimation Rate'.**

3.6.3 Sampling Parameters

Analog input levels are converted into digital values at a sample rate (**Fsamp**) determined by the ADC modulator clock **Fmod**, and by the Oversampling Factor (**OSF**), also referred to as the decimation rate (Figure 3.6.3-1). ADC timing is derived from **Fgen**, which can be supplied either by an external source or by the internal Rate-A generator (3.6.4), and which has a frequency range of 34-68 MHz.

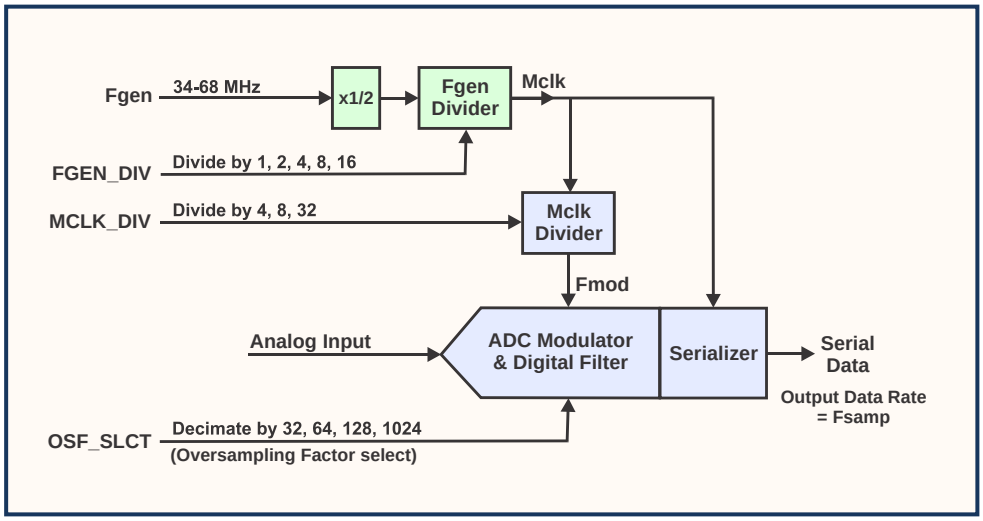

Figure 3.6.3-1. ADC Control Parameters

Fgen is divided down to the ADC master clock frequency **Mclk**, which is further divided to provide the ADC modulator clocking frequency **Fmod**. A digital filter shapes the data output spectrum, and the resulting decimated, processed signal is passed through a serializer for acquisition by the local controller.

The sample rate Fsamp is related to the frequency source **Fgen** and the control parameters **FGEN_DIV** and **MCLK_DIV** as:

$$\text{Fsamp} = \text{Fgen} / [\ 2 * \text{FGEN\_DIV} * \text{MCLK\_DIV} * \text{OSF}\ ] \qquad \textbf{(3-1)}$$

or:

$$\text{Fsamp} = \text{Mclk} / [\ \text{MCLK\_DIV} * \text{OSF}\ ] \qquad \textbf{(3-2)}$$

Fmod (Mclk/MCLK_DIV) is the modulator clock, and establishes one of three selectable speed modes: 'Fast' (÷4), 'Med'(÷8), and 'Eco' (÷32). The *Fast* mode supports higher sample rates and *bandwidth* at the expense of increased power consumption, while the *Eco* and *Med* modes normally would be used for lower sample rates. (Division by two before the Mclk Divider ensures a 50-percent duty cycle for Mclk when FGEN_DIV is 'divide by one').

These parameters can be arranged in a variety of configurations, and Tables 3.6.3-1 and 3.6.3-2 tabulate the control sets that optimize either the Oversampling Factor (OSF), or the Bandwidth. High *oversampling factors* provide maximum antialias protection, and are useful in sonar and similar acoustic applications. *Bandwidth* normally would be optimized (maximized) when analyzing rapidly changing levels such as would be encountered in pulse acquisition.

Table 3.6.3-3 provides control examples, and illustrates how a single sample rate can be obtained with different sets of control parameters.

Table 3.6.3-1. ADC Parameters; Oversampling-Factor Optimized

Fsamp Range (KSPS)	Fgen	FGEN_DIV (_SLCT)	MCLK_DIV (_SLCT)	OSF (_SLCT)
132.8 - 250.0	256 * Fsamp	1 (0)	4 (2)	**32 (0)**
66.41 - 132.8	512 * Fsamp	1 (0)	4 (2)	**64 (1)**
33.20 - 66.41	1024 * Fsamp	1 (0)	4 (2)	**128 (2)**
16.60 - 33.20	2048 * Fsamp	2 (1)	4 (2)	**128 (2)**
8.301 - 16.60	4096 * Fsamp	4 (2)	4 (2)	**128 (2)**
4.150 - 8.301	8192 * Fsamp	1 (0)	4 (2)	**1024 (3)**
2.076 - 4.150	16384 * Fsamp	1 (0)	8 (1)	**1024 (3)**
1.038 - 2.076	32768 * Fsamp	2 (1)	8 (1)	**1024 (3)**
1.000 - 1.038	65536 * Fsamp	4 (2)	8 (1)	**1024 (3)**

Table 3.6.3-2. ADC Parameters; Bandwidth Optimized

Fsamp Range (KSPS)	Fgen	FGEN_DIV (_SLCT)	MCLK_DIV (_SLCT)	OSF (_SLCT)
132.8 - 250.0	256 * Fsamp	1 (0)	**4 (2)**	32 (0)
66.4 - 132.8	512 * Fsamp	2 (1)	**4 (2)**	32 (0)
33.20 - 66.41	1024 * Fsamp	4 (2)	**4 (2)**	32 (0)
16.60 - 33.20	2048 * Fsamp	8 (3)	**4 (2)**	32 (0)
8.301 - 16.60	4096 * Fsamp	16 (4)	**4 (2)**	32 (0)
4.150 - 8.301	8192 * Fsamp	16 (4)	**4 (2)**	64 (1)
2.076 - 4.150	16384 * Fsamp	16 (4)	**4 (2)**	128 (2)
1.038 - 2.076	32768 * Fsamp	4 (2)	**4 (2)**	1024 (3)
1.000 - 1.038	65536 * Fsamp	8 (3)	**4 (2)**	1024 (3)

Table 3.6.3-3. Sample Rate Control Examples

Required Fsamp KSPS	Fgen / Fsamp	Fgen* MHz	FGEN_DIV (_SLCT)	MCLK_DIV (_SLCT)	OSF (_SLCT)	Fmod* MHz
250.00	256	64.000	1 (0)	4 (2)	32 (0)	8.000
44.000	1024	45.056	4 (2)	4 (2)	32 (0)	1.408
			1 (0)	4 (2)	128 (2)	5.632
9.375	4096	38.400	16 (4)	4 (2)	32 (0)	0.300
			4 (2)	4 (2)	128 (2)	1.200
1.000	65536	65.536	4 (2)	8 (1)	1024 (3)	1.024
			8 (3)	4 (2)	1024 (3)	1.024

* **Fgen = Fsamp * [2 * FGEN_DIV * MCLK_DIV * OSF]**. **Fmod = Fgen / [2*FGEN_DIV * MCLK_DIV].**
Values shown are nominal. Adjustment resolution of the internal Rate-A generator is constrained by the ratio of two integers (3.6.4). (Fmod shown for reference only).

3.6.4 Internal Rate-A Generator Control

Fgen can be obtained either externally through the system I/O connector or from the internal phase-locked loop (PLL) oscillator, and has a nominal frequency range of 34-68 MHz. The frequency **Fgen** of the internal Rate-A generator is related to a reference frequency **Fref** by integers **Nref** and **Nvco** controlled through the Rate-A Generator Control register (Table 3.6.4-1) as:

$$\mathbf{Fgen} = \mathbf{Fref} * \frac{\mathbf{Nvco}}{\mathbf{Nref}} \qquad \textbf{(3-3)}$$

where **Nvco** and **Nref** each has a maximum range from 20 to 300, with the optimum range being 25-100. **Fref** is the frequency of the reference oscillator, which has a standard frequency of **32.768 MHz**. Table 3.6.4-2 summarizes the rate generator control parameters, and sample rate examples are provided in Table 3.6.4-3. To establish a specific sample rate Fsamp, determine the in-range values of **Nvco and Nref** that produce the closest available rate.

Table 3.6.4-1. Rate-A Generator Control Register

Offset: 0004h **Default: 0028 0037h**

Bit Field	Mode	Designation	Function *
D[11..00]	R/W	VCO FACTOR **(Nvco)**	Rate-A VCO factor; 20-300.
D[15..12]	R/W	(Reserved)	---
D[27..16]	R/W	REF FACTOR **(Nref)**	Rate-A REF factor; 20-300.
D[31..28]	R/W	(Reserved)	---

Table 3.6.4-2. Rate-A Generator Control Parameters

Parameter	Notation	Valid Range or Value
VCO Frequency Range	**Fgen**	34 - 68 MHz
Reference Frequency	**Fref**	Standard value = 32.768 MHz
VCO Factor	**Nvco**	20-300; Optimum at 25-100.
Reference Factor	**Nref**	20-300; Optimum at 25-100.
Nvco/Nref Factor Ratio	**Nvco/Nref**	1.04- 2.08

NOTE: The nominal range of Fgen (34-68 MHz) and a Fref value of 32.768 MHz imply a valid range of 1.04-2.08 for the ratio Nvco/Nref. Performance is essentially uniform for all Nvco/Nref ratios in this range. The absolute values of Nvco and Nref are important however, because spectrum spread is minimized with smaller values. Nvco and Nref can have values up to 300, but the spectrum can exhibit increased spreading for values approaching 150 and higher. The spreading may not be objectionable for many applications, but as a general rule, use the smallest possible values for Nvco and Nref.

Table 3.6.4-3. Rate-A Generator Control Examples

Sample Rate (KSPS)	Nvco	Nref	Fgen (Mhz)
250.00	125	64	64.000
44.000	55	40	45.056
9.375	75	64	38.400
1.000	50	25	65.536

Fref = 32.768MHz. All values shown in decimal format.

NOTE: The default frequency of the Rate-A generator after initialization is 45.056 MHz.

3.6.5 External Clocking

If 'Fgen External Input' is selected by the CLOCK SOURCE control field, the signal at the external clock input is routed to the **Fgen** divider. This clocking mode would be used generally for clocking a single board from an external frequency source.

If the selected CLOCK SOURE is 'External Mclk Input', the external signal is routed directly to the ADC Mclk inputs. This clocking mode provides the optimum synchronization of multiple boards, since all ADC internal timing is referred to Mclk.

Both Fgen and Mclk external clocking eliminate the effect of the **Nvco** and **Nref** control variables, and allows the sample rate to be derived directly from the external clock source. In general, all boards operating as synchronization targets in a synchronized multiboard configuration would use the same value for this control bit.

Because **Nvco** and **Nref** have no effect in this configuration, the sample rate is calculated by assigning the external frequency as **Fgen** in Equation 3-1, or as **Mclk** in Equation 3-2.

3.6.6 Channel Synchronization

Clocking multiple converters from a single frequency source prevents the *sampling drift* that occurs when converters are clocked from different sources. *Synchronization* causes the converters in all channels to initiate conversions simultaneously, and can be used to eliminate *sampling skew* between channels.

Due to the oversampling nature of delta-sigma conversion, each conversion represents a sampling interval consisting of multiple clock cycles, and simply operating all converters from a common clock does not ensure simultaneous, or skew-free, sampling. To ensure simultaneous sampling, the converters must be synchronized to perform conversions simultaneously relative to a common point in time. Thereafter, the converters will continue to sample simultaneously while operating from a common clock.

Synchronization is invoked by setting the SYNCHRONIZE INPUTS control bit HIGH in the BCR, or by injecting an external sync pulse at the SYNC INP pins in the I/O connector with external sync selected in the Analog Input Configuration register. Completion of the synchronization sequence is indicated by the CHANNELS READY flag in the BCR undergoing a Low-to-High transition. The CHANNELS READY transition can be selected as a condition for an interrupt request event (3.8.1). *The ADCs should be synchronized after any of the analog input parameters specified in the 'Analog Input Configuration' or 'Rate-A Generator' registers are modified.* ***The input buffer is cleared during the synchronization sequence.***

3.6.7 Multiboard Operation

Multiple PCIe-24DSI64C200K boards can be connected together to share a common sampling clock and synchronization command. One of the boards is designated as the ***initiator***, and the remaining boards are designated as ***targets***. A board is designated as an initiator by setting the INITIATOR control bit HIGH in the BCR, or as a target when the control bit is LOW. *The INITIATOR control bit controls only the source of the external clock and sync outputs, and has no other effect.*

External clock and sync inputs can be provided from LVDS sources other than an initiator board.

NOTE: External I/O signals EXT CLK INP/OUT and EXT SYNC INP/OUT are configured as LVDS HI/LO pairs if the TTL EXTERNAL SYNC I/O control bit is LOW in the BCR, or for TTL signals on the HI lines if the bit is HIGH.

3.6.7.1 External Sample Clock

Target boards receive an external clock from the external clock input connection, and duplicate the input clock at the external clock output connection (Figure 3.6.2-1). The external clock input is designated as the clocking source by the CLOCK SOURCE control field HIGH in the Analog Input Configuration register (Table 3.6-1). For calculation of target board sample rates, the external sample clock corresponds to the internal Rate-A generator frequency if control bit RATE-A CLOCK OUT in the initiator board's BCR is HIGH, or to the modulator clock **Mclk** if the bit is LOW. Paragraph 3.6.5 describes clock source selection.

An ***initiator*** provides an external clock output from either of two sources. If the RATE-A CLOCK OUT control bit in the BCR is LOW (default), the external clock output is identical to the ADC master clock **Mclk**. If the control bit is HIGH, the Rate-A generator unmodified output provides the external clock.

NOTE: The INITIATOR control bit controls only the sources of the external clock and sync output signals, and has no other effect.

Multiple boards can all be configured as initiators and operated in a "star" configuration to operate from a single rate generator. To avoid overloading the LVDS source driver, an LVDS distribution module usually is required in this configuration.

3.6.7.2 External Sync

Boards that are hardware-configured for multiboard synchronization initiate a *synchronization sequence* each time a sync pulse is generated by the initiator board. A synchronization sequence is initiated by setting the SYNCHRONIZE INPUTS control bit HIGH in the BCR. This bit clears automatically.

The SYNCHRONIZE INPUTS control bit can be used also to clear the buffers on the initiator and target boards simultaneously, by first setting the CLEAR BUFFER ON SYNC control bit HIGH in the BCR on all boards.

Paragraphs 3.11.1.1 and 3.11.1.2 describe the selection of internal and external trigger or sync sources.

3.6.8 Filter Selection

Either of two lowpass filter characteristics can be selected with the LOW LATENCY FILTER control bit in the Input Configuration register (Table 3.6-1). In the default (LOW) state, this bit selects the Wideband Low-Ripple filter that provides the sharpest cutoff characteristics and the greatest anti-alias protection. This filter has a group delay of 34/Fsamp, and a settling time of 68/Fsamp.

When HIGH, this bit selects the Low Latency filter, which has the faster response usually required for pulse analysis and similar applications. The group delay for this filter is only 3/Fsamp, while the settling time is 7/Fsamp.

3.6.9 Acquisition Example

This example outlines one method of initiating an acquisition sequence, and represents one of numerous possibilities. The following conditions are assumed:

- Required sample rate: 44.000KSPS.
- Required Optimization: Oversampling factor (3.6.3).
- Input buffer: Disabled and cleared (Table 3.5.3-1).
- Clock frequency source: Internal Rate-A generator (Table 3.6-1).
- The Rate-A reference frequency Fref is 32.768MHz (3.6.4).
- Single-board configuration.

1. Use Table 3.6-1 to establish the analog input configuration for a sample rate of 44KSPS.

   In this case, Table 3.6.3-1 is used to obtain control values necessary to *optimize the oversampling factor* (OSF):

   - **FGEN_DIV = 1** (FGEN_DIV_SLCT = 0).
   - **MCLK_DIV = 4** (MCLK_DIV_SLCT = 2).
   - **OSF = 128** (OSF_SLCT = 2).

2. Determine the required Rate-A generator (**Fgen**) frequency.

   For sample rates in the range of 33.20-66.41KSPS, Table 3.6.3-1 indicates a value of 1024*Fsamp, or **45.056MHz** (1024 * 0.044000MHz) for **Fgen**.

3. Determine the values for **Nvco** and **Nref** necessary to adjust **Fgen** to the required frequency (3.6.4), and write the values to the Rate-A Generator control register.

   For sample rates in the range of 33.20-66.41KSPS. Equation 3.3 indicates:

   Nvco/Nref = Fgen/Fref

   = 45.056Mhz / 32.768MHz $(2^{15} * 5^3 * 11) / (2^{18} * 5^3)$.

   (Although other methods can be used to calculate the ratio Nvco/Nref, prime factors are used here since all factors involved are relatively small).

   = 11/8 (*4 to obtain minimum values of 25 or higher):

   Nvco = 44.

   Nref = 32.

4. For fully synchronous operation, Set the SYNCHRONIZE INPUTS control bit HIGH in the BCR.

5. Wait for CHANNELS READY = HIGH in the BCR

6. Enable the input buffer. Acquisition will commence with the next complete data set from all active channels.

3.6.10 ADC Initialization

The ADCs should be initialized, or reset, after any of the analog input parameters specified in the 'Analog Input Configuration' or 'Rate-A Generator' registers are modified. For this reason, all ADCs are reset during initialization, or when the 'Analog Input Configuration' or 'Rate-A Generator' control register is modified. The ADCs can be reset also by setting the INITIALIZE ADCS control bit HIGH in the BCR. The duration of ADC reset can be as long as 200 milliseconds, and during this interval the CHANNELS READY flag in the BCR is LOW.

3.7 Autocalibration

Autocalibration is an embedded utility that calibrates all input channels to a single internal voltage reference. Offset and gain error corrections for each channel are determined and stored during autocalibration, and then are applied to each channel in real-time during data acquisition. The correction values are retained until either: (a) power is removed, (b) a PCI reset occurs, or (c) autocalibration is invoked again. Autocalibration is invoked by setting the AUTOCAL control bit HIGH in the BCR. Completion of autocalibration is indicated by the AUTOCAL flag clearing automatically to the LOW state. The end of autocalibration is selectable as an interrupt request event (3.8). Autocalibration calibrates all channels on all ranges in a single sequence.

An autocalibration sequence can have an approximate duration of 3-4 seconds or less for sample rates of 10KSPS or higher, or up to 25 seconds for the minimum sample rate of 1KSPS. For 64 active channels operating at a sample rate of Fsamp, the ***approximate*** autocal duration is:

$$\mathbf{T_{autocal}\ (seconds) = 0.7 + (25 / Fsamp).}\quad \text{(Fsamp in KSPS).}$$

For a board with fewer than 64 channels, the autocal duration is reduced in direct proportion to the number of available channels. Read or write access from the PCI Express bus during autocalibration could disrupt the calibration process, and should be avoided. Either a suitable delay or the "Autocal Completed" interrupt should be used to detect the end of autocalibration.

If a board is defective, the autocalibration process may be unable to successfully calibrate all input channels. If this situation occurs, the AUTOCAL PASS status flag in the BCR will be LOW when the autocal sequence is completed. A HIGH state for AUTOCAL PASS indicates that autocalibration was successful for all channels.

To ensure full conformance to the product specification, autocalibration should always be invoked after:

- Power has been applied to the board,
- A PCI Express reset event has occurred,
- A sampling parameter or sampling rate has been altered.

Autocalibration can be invoked at any time, but should not occur while the system is experiencing a major environmental transition such as that which usually occurs directly after power is applied. For optimum performance, a warmup delay of 15 minutes is recommended.

NOTE: Disabled or inactive channels would autocalibration to fail. Consequently, all input groups are forced to active status temporarily during autocalibration.

3.8 Interrupt Control

In order for the board to generate a PCI Express interrupt, *both* of the following conditions must occur:

a. The internal controller must generate a Local Interrupt Request
b. The *PCI Express interrupt emulation* must be enabled.

If the internal controller generates a local interrupt request, a PCI Express interrupt will not occur unless the PCI Express interrupt has been enabled.

3.8.1 Local Interrupt Request

The single local interrupt request line is controlled by the INTERRUPT A[2:0] and INTERRUPT REQUEST FLAG control bits in the BCR. The condition for the interrupt request is selected as shown in Table 3.8.1-1. When the selected condition occurs, a local interrupt request is generated and the INTERRUPT REQUEST FLAG bit is set in the BCR. The request remains asserted until the PCI Express bus clears the BCR request flag. A local interrupt request is generated automatically at the end of initialization.

Detection of an interrupt condition or event is *edge-sensitive*. An interrupt request is generated if, and only if, a specific interrupt condition undergoes a *transition* from 'false' (not-true) to 'true' while that condition is selected.

Table 3.8.1-1. Interrupt Event Selection

Interrupt A[2:0]	Interrupt Event Condition
0	Initialization completed. Default state.
1	Autocal completed
2	Channels Ready; LOW-to-HIGH transition
3	Data Buffer threshold flag, LOW-to-HIGH transition
4	Data Buffer threshold flag, HIGH-to-LOW transition
5	Triggered Burst Completed
6	Channels Ready; HIGH-to-LOW transition
7	(Reserved)

3.8.2 Enabling the PCI Express Interrupt

A local interrupt request will not produce an interrupt on the PCI Express bus unless interrupt emulation is enabled. Refer to the PEX-8311 reference manual for details pertaining to this function.

3.9 DMA Operation

DMA transfers from the analog input FIFO buffer are supported in either **block-mode** or **demand mode**, with the board operating as bus master. Demand mode operation requires the ***slow terminate*** mode. Refer to the PEX-8311 reference manual for a detailed description of the associated DMA configuration registers.

NOTE: The PEX-8311 adapter extracts data from the 32-Bit (Lword) local bus in 64-Bit (quad-word) increments. Consequently, *if the buffer runs empty or nearly empty*, the situation can arise in which the last one or two samples in an active channel group are retained until subsequent data is acquired. If this occurs, the next sample set flushes the retained data through the PEX-8311 adapter to the PCI Express bus, and no samples are lost.

3.10 Board Configuration Register

The read-only board configuration register (Table 3.10-1) contains the existing firmware revision, and a status field that indicates the availability of optional features.

Table 3.10-1. Board Configuration Register

Offset: 0000 0024h **Default: 0000 XXXXh**

Bit Field	Description
D00-D11	Firmware Revision
D12-D15	(Reserved status flags).
D16-D17	Number of input channels: 0 => 64 Channels 1 => 48 Channels 2 => 32 Channels 3 => (Reserved)
D18-D19	Range Set: 0 => ±10V 1-3 => (Reserved)
D20-D21	Image Filter Frequency: 0 => 500kHz 1 => 100kHz 2-3 => (Reserved)
D22-D23	Master Clock Frequency: 0 => 49.152MHz 1-3 => (Reserved)
D24-D31	(Reserved; all-zero)

3.11 Triggered Burst Sampling

3.11.1 Burst Control

If burst sampling is enabled by setting the ENABLE INPUT BURST control bit HIGH in the BCR, a Burst Trigger initiates the acquisition of a specific number of samples for each active channel. During a burst, sampling proceeds at the selected input sample rate until the specified number of samples has been acquired. Sampling then terminates until a subsequent trigger occurs. The number of samples acquired during a triggered burst is specified by the 24-Bit Input Burst Block Size control register (Table 3.11.1-1). The number of samples acquired in a burst *for each channe*l equals the value contained in this register. The total number of samples acquired equals this value *times* the number of active channels. If a BURST BLOCK SIZE of zero is selected, a trigger initiates a nonterminating burst that continues as long as bursting is enabled, the buffer is enabled, and a sample clock is present.

Note: The end of a triggered burst can be detected by a High-to-Low transition of the S/W Burst Trigger control bit in the BCR, or by an interrupt (3.8).

Table 3.11.1-1. Burst Block Size Control Register

Offset: 0018h **Default: 0000 0001h**

Bit Field	Mode	Designation	Function *
D00-D23	R/W	BURST BLOCK SIZE [23..0]	Number of samples acquired per channel in a triggered burst.
D24-D31	RO	(Reserved)	---

3.11.1.1 Internal Trigger or Sync Source

If the SYNC SOURCE control bit in the Analog Input Configuration register (Table 3.6-1) is LOW, an internal source is selected for the trigger or sync. An internal (local) trigger can be generated either by asserting the S/W BURST TRIGGER control bit in the BCR, or by implementing the internal burst trigger timer (Table 3.11.2-1).

3.11.1.2 External Trigger or Sync Source

If the SYNC SOURCE control bit is HIGH, the source of trigger or sync is either the EXT SYNC INP input signal at the system I/O connector as a 120 nanosecond or greater positive TTL pulse, or the S/W BURST TRIGGER bit in the BCR. The BCR control bit clears automatically.

Regardless of the source of the trigger, the S/W BURST TRIGGER bit in the BCR will always be HIGH during a triggered burst, and the trigger will appear also as a 120 nanosecond positive pulse at the EXT SYNC OUT output in the I/O connecter for synchronously triggering other boards. *Input triggers are ignored when S/W BURST TRIGGER is HIGH, of if the buffer is disabled.*

Note: If the ENABLE INPUT BURST control bit is HIGH in the BCR, an external SYNC input will be regarded as a burst trigger, and synchronization as described in Paragraph 3.6.6 will not occur. To burst-trigger multiple boards, synchronize the boards before asserting ENABLE INPUT BURST.

Note: Although External Sync I/O is active as a Burst Trigger I/O port when bursting is enabled, the SOFTWARE SYNC control bit in the BCR is ignored in this mode.

3.11.2 Internal Burst Timer

If triggered bursting is enabled, when the ENABLE TRIGGER TIMER control bit is HIGH in the BCR, the internal trigger timer generates a continuous series of burst triggers. The trigger rate is determined as:

TRIGGER RATE (Hz) = Fclk / TRIGGER RATE DIVISOR,

where Fclk is the master clock frequency in Hertz, and TRIGGER RATE DIVISOR is defined in the 24-Bit Trigger Rate Timer register shown in Table 3.11.2-1. Fclk has a standard value of 49.152MHz.

Table 3.11.2-1. Burst Trigger Timer Register

Offset: 0000 001Ch **Default: 0000 C000h**

Bit Field:	Designation	Function
D00-D23	TRIGGER RATE DIVISOR	Rate divisor for internally timed triggered bursts.
D24-D31	(Reserved)	---

3.12 Digital I/O Port

The bidirectional digital I/O port consists of four independently controlled data bits, as shown in Table 3.12-1. Each data bit DIG IO xx DATA is a hardware input if the corresponding direction control bit DIG IO xx OUTPUT SELECT is LOW, or is an output if the control bit is HIGH. Logic polarities are retained, with a HIGH level at a connector pin associated with a HIGH level for the corresponding bit in the Digital I/O Port register. All digital I/O lines default to inputs.

Table 3.12-1 Digital Port Register

Offset: 0008h **Default: 0000 000Xh**

Data Bit	Mode	Designation	Default	Description
D00	RW	DIG IO 00 DATA	X	Digital I/O Data; Bits 00-03
D01	RW	DIG IO 01 DATA	X	
D02	RW	DIG IO 02 DATA	X	
D03	RW	DIG IO 03 DATA	X	
D04-D07	RW	(Reserved)	0h	---
D08	RW	DIG IO 00 OUTPUT SELECT	0	DIO direction control; High for output.
D09	RW	DIG IO 01 OUTPUT SELECT	0	
D10	RW	DIG IO 02 OUTPUT SELECT	0	
D11	RW	DIG IO 03 OUTPUT SELECT	0	
D12-D31	RO	(Reserved)	0h	---

3.13 Settling Time Considerations

An abrupt change in the analog configuration generally is followed by a 'settling' interval during which the analog networks are transitioning to a new state, and during which specified performance is suspended. Abrupt changes include:

- A change in voltage range or sample rate,
- A major input step-change,
- Transitioning into or out of a selftest mode, or out of autocalibration,
- A system or local reset,
- Power application.

The settling time required to reestablish specified performance depends upon the type of disruption, and can vary from tens of milliseconds for a change in voltage-range, to as long as 10-15 minutes after the initial application of power. For *most* configuration changes other than the application of power, specified performance should resume after a settling interval of 20-100 milliseconds. Low-frequency filters will extend the settling interval by an amount that depends upon the filter characteristics. In general, the longest settling delay consistent with application requirements should be implemented.

3.14 Auxiliary External Clock and Sync I/O

Two auxiliary external connections provide an alternate method of synchronizing sample clocking to external events. These bidirectional TTL connections are accessible in a 6-Pin header as AUX CLOCK and AUX SYNC (Table 2.2.2-2). When active as inputs, they *replace* the corresponding external CLK_INP and SYNC_INP signals in the system I/O connector. As outputs, they *duplicate* the CLK_OUT and SYNC_OUT signals in the system I/O connector.

AUX clock and sync signals are designated independently through the Auxiliary Sync I/O Control register (Table 3.14-1) as inputs, outputs, or inactive. AUX I/O pins are pulled up internally to +3.3VDC through 33KΩ.

Table 3.14-1. Auxiliary Sync I/O Control Register

Offset: 0000 0034h **Default: 0000 0000h**

Data Bit	Mode	Designation	Default	Description
D00-D01	R/W	AUX CLOCK Control Mode	0	AUX CLOCK I/O Control Mode: 0 => Inactive 1 => Active Input * 2, 3 => Active Output
D02-D03	R/W	AUX SYNC Control Mode	0	AUX SYNC I/O Control Mode 0 => Inactive 1 => Active Input * 2, 3 => Active Output
D04-D31	RO	(Reserved)	0	Read-back as all-zero.

* The Clock and Sync Source fields in the Analog Input Configuration register apply to these functions.

SECTION 4.0

PRINCIPLES OF OPERATION

4.1 General Description

The PCIe-24DSI64C200K contains 64 delta-sigma 24-Bit A/D converters and all supporting functions necessary for adding analog I/O capability to a PCIe expansion system. A PCIe interface adapter (Figure 4.1-1) provides the interface between the controlling PCIe bus and an internal local controller through a 32-bit local bus. The local controller performs all internal configuration and data manipulation functions, including autocalibration.

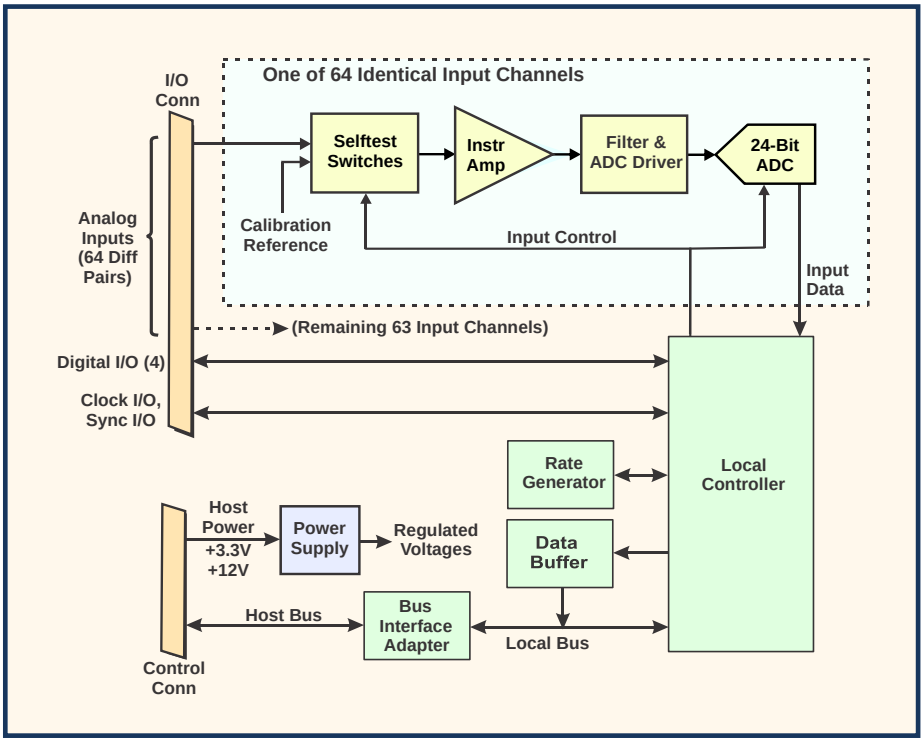

Figure 4.1-1. Functional Block Diagram

Input configuration switches allow the controller to select any of several signal sources as inputs to the ADC's. This feature is used to establish the internal connections necessary during autocalibration, and also permits verification from the PCIe bus of the integrity of all analog input channels. All channels are calibrated against a single precision voltage reference. The offset and gain calibrations of each input channel are adjusted with correction values that are determined during on-demand autocalibration.

4.2 Analog Inputs

64 differential analog input channels are arranged into eight identical 8-channel groups, with each group software-designated as either active or inactive. Only active groups provide acquisition samples to the input data buffer. Analog-to-digital conversions can be performed on signals from any of several sources, which are selected by the input configuration switches shown in Figure 4.1. During normal operation, the analog input signal passes through a differential amplifier which removes any common mode voltage that might be present. During selftest and autocalibration operations, the input configuration switches can be used to replace the system input signal with either a precision zero (ground) or positive full-scale reference voltage.

A range control attenuator adjusts the maximum level of the signal to the full-scale input range required by the ADC. High frequency noise and digital filter images are attenuated by a first order lowpass filter.

The final scaled, conditioned and filtered input signal is digitized by each ADC into a 24-BIt serial data word that is deserialized into parallel format by the local controller. The local controller then applies offset and gain correction factors, attaches a 6-bit channel tag to each data value, and finally transfers the corrected value to the input data buffer.

Antialias filtering is provided by each ADC in the form of a lowpass digital filter with a sharp cutoff frequency at approximately 48 percent of the sampling frequency. Like most digital filters, the digital filter has no filtering effect at multiples of the sampling clock, which is a multiple (x32-1024) of the sampling frequency. To prevent extraneous signal frequency components within these "filter images" from appearing in the passband, the hardware image filter shown in Figure 4.1-1 can be factor-configured to provide attenuation of the digital filter images.

4.3 Autocalibration

Autocalibration is an embedded firmware utility that calibrates all input channels to a single internal voltage reference. The utility can be invoked at any time by the control software.

The offset error of each channel is determined first, by selecting a zero input reference level and by storing the values reported from all channels. A precision internal voltage reference then is used to calculate the gain error, and finally both offset and gain correction values are stored in static RAM for retrieval during data acquisition.

The internal voltage reference is adjusted to equal 99.000 percent of the selected input voltage range. This in-range value ensures that the ADC's will provide the nonsaturated, or in-range, responses that are necessary during the calibration adjustment process.

4.4 Sampling Clocks

An internal sample rate generator provides a frequency range of 34-68 MHz, which is divided down by a software-specified integer to provide sample rates from 1.0 KSPS to 250 KSPS.

An external clock output also can be designated as the rate generator. A board from which a rate generator or ADC sample clock originates is a *clock initiator*. Boards that receive the external clock are *clock targets, which can also retransmit the clock to subsequent targets*. Multiple targets can be controlled from a single initiator.

4.5 Power Conversion

Regulated supply voltages of +5 Volts, and ±14 Volts are required by the analog networks. Multiple DC/DC converters in the power conditioner use +3.3V and +12V input power from the PCI Express bus to produce preregulated DC voltages. These switching-regulated voltages subsequently are postregulated with linear regulators to the required supply voltages. Linear regulators ensure that the final power voltages delivered to the analog networks are well-regulated and free of noise.

APPENDIX A

LOCAL REGISTER QUICK REFERENCE

APPENDIX A

LOCAL REGISTER QUICK REFERENCE

This appendix summarizes all local registers in the order in which they appear in Section 3.

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Table 3.1-1. Control and Data Registers

Local Addr	Mode	Designation	Default	Description	Ref
00	R/W	**Board Control (BCR)**	0000 3830h	Board Control Register (BCR)	3.2
04	R/W	**Rate-A Generator Control**	0028 0037h	PLL reference oscillator control integers.	3.6.4
08	R/W	**Digital I/O Port**	0000 000Xh	Digital I/O Port control	3.12
0C	R/W	**Analog Input Configuration**	0002 20FFh	Analog input sampling parameters	3.4
10-14	RO	**(Reserved)**	0000 0000h	---	---
18	RW	**Burst Block Size**	0000 0001h	Specifies the number of sample sets to be acquired in a triggered burst	3.11
1C	R/W	**Burst Trigger Timer**	0000 C000h	Internal trigger timer rate divisor	3.11
20	R/W	**Buffer Control**	0X03 FFFEh	Input buffer control and status	3.5.3
24	RO	**Board Configuration**	00XX XXXXh	Installed firmware and hardware options	3.10
28	RO	**Buffer Size**	0XXX XXXXh	Number of ADC values in the input buffer.	3.5.4
2C	RO	Autocal Values [1]	---	---	---
30	RO [2]	**Input Data Buffer**	XXXX XXXXh	Input Data Buffer; Data and channel tag	3.5
34	R/W	**Aux Sync I/O Register**	0000 0000hh	Auxiliary clock and sync I/O port	3.14
38-3C	--	(Reserved)	---	---	--

[1] Maintenance register; shown for reference only. [2] DMA access.

Table 3.2-1. Board Control Register

Offset: 0000h **Default: 0000 3830h**

Data Bit	Mode	Designation	Def	Description	Ref
D00-D01	R/W	AIM[1..0]	0	Analog input mode. Selects system inputs or selftest mode. Defaults to system inputs.	3.4
D02-D03	R/W	(Reserved)	0	---	---
D04	R/W	OFFSET BINARY	1	Selects offset binary or two's complement input data format. Defaults HIGH to offset binary.	3.5.2
D05	R/W	INITIATOR	1	Selects INITIATOR or TARGET mode for external clock and sync signals. Defaults HIGH to Initiator mode.	3.6.7
D06	R/W	* SYNCHRONIZE INPUTS	0	Initiates a local ADC sync operation when asserted. Also generates an external sync output if INITIATOR mode is selected. Clears automatically.	3.6.6 3.6.7.2 3.6.9
D07	R/W	* AUTOCAL	0	Initiates an autocalibration operation when asserted. Clears automatically upon autocal completion.	3.7
D08-D10	R/W	INTERRUPT A[2..0]	0	Interrupt event selection. Default is zero.	3.8
D11	R/W	INTERRUPT REQUEST FLAG	1	Set HIGH when the board requests an interrupt. Clears the request when cleared LOW by the bus.	
D12	RO	AUTOCAL PASS	1	Set HIGH at reset or autocal initialization. Cleared LOW if autocalibration terminates unsuccessfully.	3.7
D13	RO	CHANNELS READY	1	LOW during any change in channel parameters. Asserted HIGH when inputs are ready to acquire data.	3.4.3
D14	RO	BUFFER THRESHOLD FLAG	0	Asserted HIGH when buffer contents exceed the assigned threshold.	3.5.3.1
D15	R/W	* INITIALIZE	0	Initializes the board when asserted. Sets all defaults.	3.3.2
D16	R/W	ENABLE TRIGGER TIMER	0	Enables the internal burst trigger timer.	3.11.2
D17	R/W	CLEAR BUFFER ON SYNC	0	When this bit is HIGH, the context of the SYNCHRONIZE INPUTS control bit changes to CLEAR BUFFER.	3.5.3.2 3.6.7.2
D18	R/W	RATE-A CLOCK OUT (Initiator Mode only)	0	When HIGH, selects the internal Rate-A generator as the external clock output source. When LOW, selects the ADC master clock Mclk as the output.	3.6.7.1
D19	R/W	* INITIALIZE ADCS	0	Initializes (resets) all local ADCs.	3.6.10
D20	R/W	(Reserved)	0	---	---
D21	R/W	TTL EXTERNAL SYNC I/O	0	Selects TTL external sync I/O configuration.	3.6.7
D22	R/W	ENABLE INPUT BURST	0	Selects triggered-burst acquisition when HIGH.	3.11
D23	R/W	S/W BURST TRIGGER	0	Initiates a triggered burst when asserted. Forced HIGH during any triggered burst.	
D24-D31	RO	(Reserved)	- 0 -	---	---

* Clears automatically.

Table 3.4-1. Analog Input Function Selection

Aim[..0]	Function or Mode
0	Differential analog input mode.
1	(Reserved).
2	ZERO test. Internal ground reference is connected to all analog input channels.
3	+VREF test. Internal voltage reference is connected to all analog input channels.

Table 3.5.2-1. Input Data Buffer Organization

Offset: 0000 0030h **Default: XXXX XXXXh**

Data Width (Bits)	Reserved (All-zero)	Channel Tag	Data Zero-Pad *	Data Value
16	D[31..30]	D[29..24]	D[23..16]	D[15..0]
18	D[31..30]	D[29..24]	D[23..18]	D[17..0]
20	D[31..30]	D[29..24]	D[23..20]	D[19..0]
24	D[31..30]	D[29..24]	---	D[23..0]

* Sign extension field if Two's Complement coding is selected.

Table 3.5.2.2-1. Analog Input Data Coding; 16-Bit Data Field

	Digital Value (Hex)	
Analog Input Level	**Offset Binary**	**Two's Complement**
Positive Full Scale minus 1 LSB	FFFFh	7FFFh
Zero plus 1 LSB	8001h	0001h
Zero	8000h	0000h
Zero minus 1 LSB	7FFFh	FFFFh
Negative Full Scale plus 1 LSB	0001h	8001h
Negative Full Scale	0000h	8000h

Table 3.5.3-1. Buffer Control Register

Offset: 0000 0020h **Default: 0X03 FFFEh**

Bit Field	Mode	Designation	Def	Function
D00-D18	R/W	BUFFER THRESHOLD	3 FFFEh	Buffer Flag Threshold
D19	R/W	ENABLE BUFFER INPUT	0	Enables inputs to the buffer
D20	R/W	CLEAR BUFFER *	0	Clears (empties) the buffer
D21-D22	R/W	DATA WIDTH	0	Controls the width of the buffer data field as: 0 => 16 bits 1 => 18 bits 2 => 20 bits 3 => 24 bits.
D23	R/W	(Reserved)	0	---
D24	R/W	BUFFER OVERFLOW **	0	Reports buffer overflow (Write on full)
D25	R/W	BUFFER UNDERFLOW **	0	Reports buffer underflow (Read on empty)
D26-D31	RO	(Reserved)	0h	---

* Clears automatically. ** Clear by writing LOW, or by board reset.

Table 3.5.4-1. Buffer Size Register

Offset: 0000 0028h **Default: XXXX XXXXh**

Bit Field	Mode	Designation	Function
D00-D18	RO	BUFFER SIZE [00..18]	Number of sample values contained in the input buffer.
D19-D31	RO	(Reserved)	---

Table 3.6-1. Analog Input Configuration Register

Offset: 000Ch **Default: 0002 20FFh**

Bit Field	Mode	Designation	Def	Function	Ref
D00	R/W	CHAN GROUP 0 ACTIVE	1	Channel Group-0 Active (Chan 00-07)	3.6.1
D01	R/W	CHAN GROUP 1 ACTIVE	1	Channel Group-1 Active (Chan 08-15)	
D02	R/W	CHAN GROUP 2 ACTIVE	1	Channel Group-2 Active (Chan 16-23)	
D03	R/W	CHAN GROUP 3 ACTIVE	1	Channel Group-3 Active (Chan 24-31)	
D04	R/W	CHAN GROUP 4 ACTIVE	1	Channel Group-4 Active (Chan 32-39)	
D05	R/W	CHAN GROUP 5 ACTIVE	1	Channel Group-5 Active (Chan 40-47)	
D06	R/W	CHAN GROUP 6 ACTIVE	1	Channel Group-6 Active (Chan 48-55)	
D07	R/W	CHAN GROUP 7 ACTIVE	1	Channel Group-7 Active (Chan 56-63)	
D08-D11	R/W	FGEN_DIV_SLCT	0	Selects the Fgen divisor FGEN_DIV: 0 => ÷1 1 => ÷2 2 => ÷4 3 => ÷8 4 => ÷16 5-15 => (Reserved)	3.6.3
D12-D15	R/W	MCLK_DIV_SLCT	2	Selects the Mclk divisor MCLK_DIV: 0 => ÷32 ('Eco' mode: Lowest bandwidth, lowest power) 1 => ÷8 ('Median' mode: Intermed bandwidth and power) 2 => ÷4 ('Fast' mode: Highest bandwidth, Max power) 3-15 => (Reserved)	3.6.3
D16-D19	R/W	OSF_SLCT	2	Selects the Oversampling factor (Decimation rate): 0 => OSF= 32 1 => OSF= 64 2 => OSF= 128 3 => OSF= 1024 4-15 => (Reserved)	3.6.3
D20-D21	R/W	CLOCK SOURCE	0	Selects the ADC clocking source: 0 => Internal Rate-A generator 1 => External Fgen Input. (Through the Fgen divider) 2 => External Mclk Input. (Routed directly to the ADC mclk inputs). 3 => (Reserved)	3.6.2 3.6.5
D22	R/W	SYNC SOURCE	0	Selects the Sync source: 0 => Internal trigger timer, or BCR sync. 1 => External Sync/Trigger Input, or BCR sync.	3.6.6 3.11
D23	R/W	LOW LATENCY FILTER	0	Selects the Low Latency filter if HIGH, or the Wideband Low-Ripple filter if LOW.	3.6.8
D24-D31	R/W	(Reserved)	- 0 -	---	---

Table 3.6.3-1. ADC Parameters; Oversampling-Factor Optimized

Fsamp Range (KSPS)	Fgen	FGEN_DIV (_SLCT)	MCLK_DIV (_SLCT)	OSF (_SLCT)
132.8 - 250.0	256 * Fsamp	1 (0)	4 (2)	**32 (0)**
66.41 - 132.8	512 * Fsamp	1 (0)	4 (2)	**64 (1)**
33.20 - 66.41	1024 * Fsamp	1 (0)	4 (2)	**128 (2)**
16.60 - 33.20	2048 * Fsamp	2 (1)	4 (2)	**128 (2)**
8.301 - 16.60	4096 * Fsamp	4 (2)	4 (2)	**128 (2)**
4.150 - 8.301	8192 * Fsamp	1 (9)	4 (2)	**1024 (3)**
2.076 - 4.150	16384 * Fsamp	1 (0)	8 (1)	**1024 (3)**
1.038 - 2.076	32768 * Fsamp	2 (1)	8 (1)	**1024 (3)**
1.000 - 1.038	65536 * Fsamp	4 (2)	8 (1)	**1024 (3)**

Table 3.6.3-2. ADC Parameters; Bandwidth Optimized

Fsamp Range (KSPS)	Fgen	FGEN_DIV (_SLCT)	MCLK_DIV (_SLCT)	OSF (_SLCT)
132.8 - 250.0	256 * Fsamp	1 (0)	**4 (2)**	32 (0)
66.4 - 132.8	512 * Fsamp	2 (1)	**4 (2)**	32 (0)
33.20 - 66.41	1024 * Fsamp	4 (2)	**4 (2)**	32 (0)
16.60 - 33.20	2048 * Fsamp	8 (3)	**4 (2)**	32 (0)
8.301 - 16.60	4096 * Fsamp	16 (4)	**4 (2)**	32 (0)
4.150 - 8.301	8192 * Fsamp	16 (4)	**4 (2)**	64 (1)
2.076 - 4.150	16384 * Fsamp	16 (4)	**4 (2)**	128 (2)
1.038 - 2.076	32768 * Fsamp	4 (2)	**4 (2)**	1024 (3)
1.000 - 1.038	65536 * Fsamp	8 (3)	**4 (2)**	1024 (3)

Table 3.6.3-3. Sample Rate Control Examples

Required Fsamp KSPS	Fgen / Fsamp	Fgen* MHz	FGEN_DIV (_SLCT)	MCLK_DIV (_SLCT)	OSF (_SLCT)	Fmod* MHz
250.00	256	64.000	1 (0)	4 (2)	32 (0)	8.000
44.000	1024	45.056	4 (2)	4 (2)	32 (0)	1.408
			1 (0)	4 (2)	128 (2)	5.632
9.375	4096	38.400	16 (4)	4 (2)	32 (0)	0.300
			4 (2)	4 (2)	128 (2)	1.200
1.000	65536	65.536	4 (2)	8 (1)	1024 (3)	1.024
			8 (3)	4 (2)	1024 (3)	1.024

* **Fgen = Fsamp * [2 * FGEN_DIV * MCLK_DIV * OSF]**. **Fmod = Fgen / [2*FGEN_DIV * MCLK_DIV].**
Values shown are nominal. Adjustment resolution of the internal Rate-A generator is constrained by the ratio of two integers (3.6.4). (Fmod shown for reference only).

Table 3.6.4-1. Rate-A Generator Control Register

Offset: 0004h **Default: 0028 0037h**

Bit Field	Mode	Designation	Function *
D[11..00]	R/W	VCO FACTOR **(Nvco)**	Rate-A VCO factor; 20-300.
D[15..12]	R/W	(Reserved)	---
D[27..16]	R/W	REF FACTOR **(Nref)**	Rate-A REF factor; 20-300.
D[31..28]	R/W	(Reserved)	---

* For optimum performance, select the lowest possible values for Nvco and Nref.

Table 3.6.4-2. Rate-A Generator Control Parameters

Parameter	Notation	Valid Range or Value
VCO Frequency Range	**Fgen**	34 - 68 MHz
Reference Frequency	**Fref**	Standard value = 32.768 MHz
VCO Factor	**Nvco**	20-300; Optimum at 25-100.
Reference Factor	**Nref**	20-300; Optimum at 25-100.
Nvco/Nref Factor Ratio	**Nvco/Nref**	1.04- 2.08

Table 3.6.4-3. Rate-A Generator Control Examples

Sample Rate (KSPS)	Nvco	Nref	Fgen (Mhz)
250.00	125	64	64.000
44.000	55	40	45.056
9.375	75	64	38.400
1.000	50	25	65.536

Fref = 32.768MHz. All values shown in decimal format.

Table 3.8.1-1. Interrupt Event Selection

Interrupt A[2:0]	Interrupt Event Condition
0	Initialization completed. Default state.
1	Autocal completed
2	Channels Ready; LOW-to-HIGH transition
3	Data Buffer threshold flag, LOW-to-HIGH transition
4	Data Buffer threshold flag, HIGH-to-LOW transition
5	Triggered Burst Completed
6	Channels Ready; HIGH-to-LOW transition
7	(Reserved)

Table 3.10-1. Board Configuration Register

Offset: 0000 0024h **Default: 0000 XXXXh**

Bit Field	Description
D00-D11	Firmware Revision
D12-D15	(Reserved status flags).
D16-D17	Number of input channels: 0 => 64 Channels 1 => 48 Channels 2 => 32 Channels 3 => (Reserved)
D18-D19	Range Set: 0 => ±10V 1-3 => (Reserved)
D20-D21	Image Filter Frequency: 0 => 500kHz 1 => 100kHz 2-3 => (Reserved)
D22-D23	Master Clock Frequency: 0 => 49.152MHz 1-3 => (Reserved)
D24-D31	(Reserved; all-zero)

Table 3.11.1-1. Burst Block Size Control Register

Offset: 0018h **Default: 0000 0001h**

Bit Field	Mode	Designation	Function *
D00-D23	R/W	BURST BLOCK SIZE [23..0]	Number of samples acquired per channel in a triggered burst.
D24-D31	RO	(Reserved)	---

Table 3.11.2-1. Burst Trigger Timer Register

Offset: 0000 001Ch **Default: 0000 C000h**

Bit Field:	Designation	Function
D00-D23	TRIGGER RATE DIVISOR	Rate divisor for internally timed triggered bursts.
D24-D31	(Reserved)	---

Table 3.12-1 Digital Port Register

Offset: 0008h **Default: 0000 000Xh**

Data Bit	Mode	Designation	Default	Description
D00	RW	DIG IO 00 DATA	X	Digital I/O Data; Bits 00-03
D01	RW	DIG IO 01 DATA	X	
D02	RW	DIG IO 02 DATA	X	
D03	RW	DIG IO 03 DATA	X	
D04-D07	RW	(Reserved)	0h	---
D08	RW	DIG IO 00 OUTPUT SELECT	0	DIO direction control; High for output.
D09	RW	DIG IO 01 OUTPUT SELECT	0	
D10	RW	DIG IO 02 OUTPUT SELECT	0	
D11	RW	DIG IO 03 OUTPUT SELECT	0	
D12-D31	RO	(Reserved)	0h	---

Table 3.14-1. Auxiliary Sync I/O Control Register

Offset: 0000 0034h **Default: 0000 0000h**

Data Bit	Mode	Designation	Default	Description
D00-D01	R/W	AUX CLOCK Control Mode	0	AUX CLOCK I/O Control Mode: 0 => Inactive 1 => Active Input * 2, 3 => Active Output
D02-D03	R/W	AUX SYNC Control Mode	0	AUX SYNC I/O Control Mode 0 => Inactive 1 => Active Input * 2, 3 => Active Output
D04-D31	RO	(Reserved)	0	Read-back as all-zero.

* The Clock and Sync Source fields in the Analog Input Configuration register apply to these functions.

APPENDIX B

MIGRATION FROM PCI-24DSI32

Appendix B

Migration From PCI-24DSI32

Operation of the PCIe-24DSI64C200K is very similar to that of the PCI-24DSI32. This appendix summarizes the principal similarities and differences between the two products, and is provided as a general guide rather than a definitive list of requirements.

B.1. Comparison of Features

Table B.1 provides a brief comparison of PCIe-24DSI64C200K and PCI-24DSI32 features. The two products differ principally with respect to the number of input channels and the host bus architecture.

Table B.1. PCIe-24DSI64C200K, PCI-24DSI32 Features Comparison

Feature	PCIe-24DSI64C200K	PCI-24DSI32
Number of Channels	**64**	**32**
Host Bus Architecture	**PCI Express**	**PCI 2.3**
Maximum sample rate	**250KSPS**	**200KSPS**
Group Delay	**34/Fsamp, 3/Fsamp, Selectable**	**12/Fsamp**
Input Range	**Single range at ±0.5V to ±10V**	**3 ranges: ±2.5, ±5, ±10V**
Triggered bursts	**Supported with timer and block size**	**Trigger-only; No autotermination.**
Digital I/O Port	**Bidirectional TTL; 4-bit**	**None**
Local Clock	**49.152 MHz**	**30 MHz**
Conversion Resolution	24 Bits	24 Bits
Data Buffer	256K-Sample FIFO	256K-Sample FIFO

B.2. Migration Issues

- Control of sampling parameters (Sect 3.6) has been simplified, and allows utilization of advanced ADC features.
- 'Scan Synchronization' (orig Sect 3.10) is not required, and this section has been eliminated.
- The triggered burst feature (new Sect 3.11) has been upgraded to accept fixed-count burst acquisition and timed repetition.
- DMA control (Sect 3.9) has been modified to accommodate the PCI Express host interface.
- A 4-bit bidirectional digital I/O port has been added (Sect 3.12).

Section 2:

I/O connections have been increased from 100 pins to 160 pins.

Table 3.1-1**:**

- **Nref PLL**, **Nvco PLL** control registers: Replaced by **Rate-A Generator** control register.
- **Rate Assignments, Rate Divisor** control registers: Replaced by **Analog Input Configuration** control register.
- Three new control registers have been added: **Burst Block Size, Burst Trigger Timer, and Digital I/O Port**.
- The PLL Reference Frequency register has been eliminated.

Table 3.2-1 (BCR)**:**

- The **Range-select field** has been eliminated, as have also the '**Synchronize Scan',** **'Select Low Image Filter', 'Arm External Trigger'** and **'Threshold Flag Out'** control bits**.**
- Three new control bits have been added: **'Enable Input Burst'**, **'S/W Burst Trigger'** and **'Initialize ADCs'.**
- D18 has been renamed as **'Rate-A Clock Out'**

B.2. Migration Issues (Cont):

Sect 3.3:

- Initialization duration has been decreased from 5 seconds to 500ms.
- The input buffer initializes to the **disabled** state, to avoid extraneous data acquisition after initialization.
- Default sample rate and rate generator frequencies have been modified.

Sect 3.6 (Input Sampling Control)**:** Entire section has been updated.

Sect 3.9 (DMA Operation)**:** Referred to the PEX-8311 manual.

Orig Sect 3.6.2.2: (Legacy Rate Generator): This section and function have been eliminated.

Table 3.5.2-1**:** The channel-tag field width has been increased to 6 bits.

Table 3.5.3-1**:** The 'Threshold' field has been expanded to 19 bits.

Bits D18-D21 have moved up (left) one position.

The 'Disable Buffer Input' control bit has been redesignated as "Enable Buffer Input'. (This change prevents the buffer from filling immediately after initialization).

Table 3.8.1-1: Added event; 'Channels Ready' High-to-Low transition..

Table 3.10-1: (Orig Table 3.11.1): (Board Configuration)**:** Modified to reflect new options.

Orig Table 3.4.3**: (**Input Range) This table has been eliminated; the input range is now fixed.

Orig Tables 3.6.1.1, 3.6.1.2-1, 3.6.1.2-2, 3.6.1.3: Replaced by Table 3.6.-1.

Orig Tables 3.6.2.1-1 and 3.6.2.1-2: Replaced by Table 3.6.4-1.

Orig Table 3.6.2.1-3: Replaced by Table 3.6.4-2.

Orig Tables 3.6.2.2-1, 3.6.3**:** These tables have been eliminated.

New Tables added: 3.5.4-1 (Buffer Size), 3.11.1-1 (Burst Block Size), 3.11.2-1 (Burst Trigger Timer).

New Tables added: 3.6.3-1, 3.6.3-2, 3.6.3-3. Sampling parameters application examples.

New Table added: 3.12. Bidirectional Digital I/O Port control.

Revision History:

12-16-2015:	Origination.
05-27-2017:	General editorial markups.
06-27-2017:	Para 2.2.2: Updated System I/O pin assignments.
06-07-2018:	Figure 2.2.2-1: Reversed P3, P4 locations. Table 3.2-1. Revised D17 description. Removed 'Preliminary' status.
06-08-2019:	Cover sheet: Corrected sample rate in title.
08-16-2020:	Table 3.10-1: Added 100kHz listing.

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