PCIe-OPTO32C-12V-CONTACT

User's Manual

24 Input Bits

8 Output Bits

Optional -12V-CONTACT-8X28V

Opto-Isolator Board

General Standards Corporation
8302A Whitesburg Drive
Huntsville, AL 35802
Phone: (256) 880-8787
Fax: (256) 880-8788
URL: www.generalstandards.com
E-mail: support@generalstandards.com

Preliminary

PREFACE

Additional copies of this manual or other literature may be obtained from:

General Standards Corporation
8302A Whitesburg Dr.
Huntsville, Alabama 35802
Tele: (256) 880-8787
FAX: (256) 880-8788
E-mail: support@generalstandards.com

The information in this document is subject to change without notice.

General Standards Corp. makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. Although extensive editing and reviews are performed before release to ECO control, **General Standards Corp.** assumes no responsibility for any errors that may exist in this document. No commitment is made to update or keep current the information contained in this document.

General Standards Corp. does not assume any liability arising out of the application or use of any product or circuit described herein, nor is any license conveyed under any patent rights or any rights of others.

General Standards Corp. assumes no responsibility for any consequences resulting from omissions or errors in this manual, or from the use of information contained herein.

General Standards Corp. reserves the right to make any changes, without notice, to this product to improve reliability, performance, function, or design.

This user's manual provides information on the specifications, theory of operation, register level programming, installation of the board and information required for customized hardware/software development.

RELATED PUBLICATIONS

The following manuals and specifications provide the necessary information for in depth understanding of the specialized parts used on this board.

EIA Standard for the RS-422A Interface (EIA order number EIA-RS-422A)

PCI Local Bus Specification Revision 2.1 June 1, 1995. Questions regarding the PCI specification be forwarded to:

PCI Special Interest Group
P.O. Box 14070
Portland, OR 97214
(800) 433- 5177 (U.S.)
(503) 797-4207 (International)
(503) 234-6762 (FAX)

PCIe-OPTO32C-12V-CONTACT Documentation History

1. Alterations for PCIe-OPTO32C-12V-CONTACT Board Assembly. Created from PCIe-OPTO16x16 baseline manual. Added Jumpers descriptions. Added LED's descriptions. Explained -CONTACT configurations better. Explained Resistor Values used in the -CONTACT Configurations. Formatting alterations. Clarify system configuration notes.

Table Of Contents

Table Of Figures

Table Of Tables

SECTION 1

1. Introduction

The PCIe-OPTO32C board is a high performance Single Lane PCI Express card offering 24 Opto-Isolated inputs and 8 Opto-Isolated outputs. It is based on the PCI-OPTO32B and Offers the same cable interface options and the same cable pin outs as the PCI-OPTO32B.

The PCIe-OPTO32C is available in the same 3 configurations as the PCI-OPTO32B with the same cable pin outs.

- As a Standard OPTO32 Board with 24 input Channels. See the PCIe-OPTO32C Manual
- As a OPTO32C-12V-CONTACT which is designed to sense contact closures on all 24 inputs. The high side of the Opto-Isolator is connected to +12V through a Current Limiting Resistor.
- As a OPTO32C-12V-CONTACT-8x28V which has channels 0 through 7 configured as normal OPTO Inputs but channels 8 through 23 are configured to sense contact closures.

1.1 Differences From OPTO32 Family

The PCIe-OPTO32C is based on the PCI-OPTO32B family. It was designed to provide a migration path for the OPTO32 family to the PCIe Bus. It uses the same cable connector and the same cable Pin out as other members of the OPTO32 Family.

- Output Bits 0-7 are the same as the OPTO32 Family.
- Input Bits 0-22 are the same as the OPTO32 Family.

The following differences exist between the OPTO32 Family and the PCIe-OPTO32C.

- Special Schmidt Trigger Input has been removed from Input Channel 23. All Inputs are the same.
- Input 23 is now the same as Input Channels 00-22
- True PCIe Form factor.
- Uses the PLX PEX 83111 PCIe Bus Interface.
- Card is mapped into PCIe Memory Space.

1.2 Card Features

- 24 optically isolated inputs
  - Selectable input voltage range thru use of field replaceable bias resistors.
  - Industry Standard 8 Pin Sip Resistors – 770-83-Rxx Series.
- 8 optically isolated outputs - 4 normal, 4 Diode Clamped
- Software Programmable clock debounce rate
- Software Programmable Change of State detection. Rising edge or falling edge per input channel
- Software Programmable Interrupts on any or all Change of State bit(s)
- Software Pre-loadable Event counter on Input Bit 23
- Programmable Interrupt on Event Counter Overflow
- Built in Self-Test Features.
  - Registers are Read / Write.
  - Ability to monitor the Debounce Clock.

The board uses the PEX 8311 PCIe single lane interface chip to provide the advanced features of the PCIe interface environment. These features include:

- Programmable Little Endian / Big Endian swapping
- PCIe cycles Asynchronous to local bus cycles
- Software Programmable board base address

The PCIe-OPTO32C offers the same operating modes as the PCI-OPTO32B. These include:

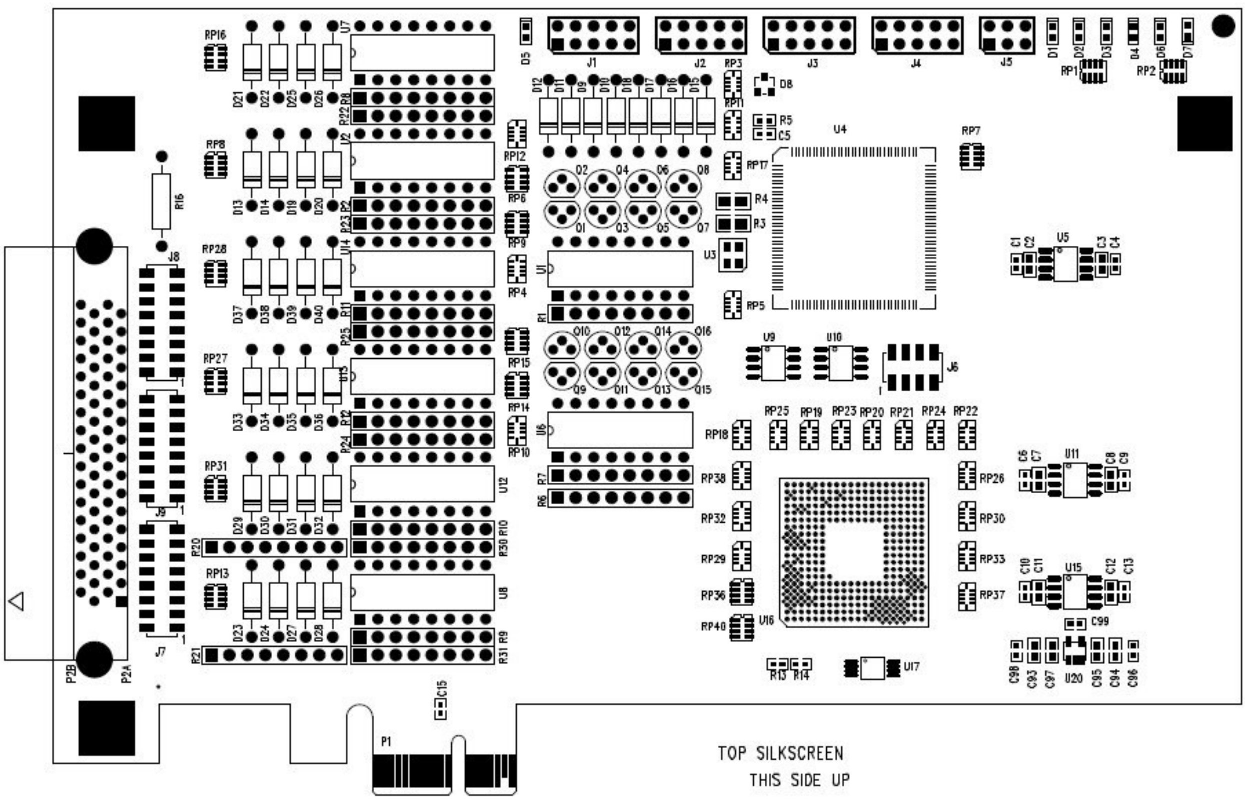
- Standard OPTO32 Operation, same as the PCI-OPTO32B and the PMC-OPTO32A
- -12V-Contact and -12V-CONTACT-8x28V Operation, same at the PCI-OPTO32B .
- Same Cable Pin-out as the PCI-OPTO32B.
- Optional Higher current resistors on channels 0-7
- Jumpers for Grounding connector pins in the –CONTACT configuration.

SECTION 2

2. INSTALLATION AND MAINTENANCE

2.1 Card Configuration

Figure 1 Board Layout



2.2 Installation

2.2.1 Physical Installation

Selectable input voltage range thru use of field replaceable bias resistors using standard 8 pin SIP isolation resistors. These bias resistor packages are socketed for easy replacement One bias resistor package will affect the input channels on nibble boundaries.

2.2.2 Input / Output Cable Connectors -12V-CONTACT

The PCIe-OPTO32C has the Same Cable Connector and the Same Cable Pinout as the PCI-OPTO32B. The following table lists the cable pin out for the 24 contact input option boards.

Table 2-1 Input / Output Cable Pin Assignments -12V-CONTACT

PIN NUMBER	SIGNAL	PIN NUMBER	SIGNAL
1	GND	35	GND
2	IN CH00	36	IN CH17
3	GND	37	GND
4	IN CH01	38	IN CH18
5	GND	39	GND
6	IN CH02	40	IN CH19
7	GND	41	GND
8	IN CH03	42	IN CH20
9	GND	43	GND
10	IN CH04	44	IN CH21
11	GND	45	GND
12	IN CH05	46	IN CH22
13	GND	47	GND
14	IN CH06	48	IN CH23
15	GND	49	LOG OUT CH0 HI
16	IN CH07	50	LOG OUT CH0 LO
17	GND	51	LOG OUT CH1 HI
18	IN CH08	52	LOG OUT CH1 LO
19	GND	53	LOG OUT CH2 HI
20	IN CH09	54	LOG OUT CH2 LO
21	GND	55	LOG OUT CH3 HI
22	IN CH10	56	LOG OUT CH3 LO
23	GND	57	PWR OUT CH4 HI
24	IN CH11	58	PWR OUT CH4 LO
25	GND	59	PWR OUT CLAMP 4
26	IN CH12	60	PWR OUT CH5 HI
27	GND	61	PWR OUT CH5 LO
28	IN CH13	62	PWR OUT CLAMP 5
29	GND	63	PWR OUT CLAMP 6
30	IN CH14	64	PWR OUT CH6 HI
31	GND	65	PWR OUT CH6 LO
32	IN CH15	66	PWR OUT CLAMP 7
33	GND	67	PWR OUT CH7 HI
34	IN CH16	68	PWR OUT CH7 LO

2.2.3 Input / Output Cable Connectors –12V-CONTACT-8x28V

The PCIe-OPTO32C has the Same Cable Connector and the Same Cable Pinout as the PCI-OPTO32B. The following table lists the cable pinout for the 8 input 16 contact input option boards.

Table 2-2 Input / Output Cable Pin Assignments –12V-CONTACT-8x28V

PIN NUMBER	SIGNAL	PIN NUMBER	SIGNAL
1	IN CH00 HI	35	GND
2	IN CH00 LO	36	IN CH17
3	IN CH01 HI	37	GND
4	IN CH01 LO	38	IN CH18
5	IN CH02 HI	39	GND
6	IN CH02 LO	40	IN CH19
7	IN CH03 HI	41	GND
8	IN CH03 LO	42	IN CH20
9	IN CH04 HI	43	GND
10	IN CH04 LO	44	IN CH21
11	IN CH05 HI	45	GND
12	IN CH05 LO	46	IN CH22
13	IN CH06 HI	47	GND
14	IN CH06 LO	48	IN CH23
15	IN CH07 HI	49	LOG OUT CH0 HI
16	IN CH07 LO	50	LOG OUT CH0 LO
17	GND	51	LOG OUT CH1 HI
18	IN CH08	52	LOG OUT CH1 LO
19	GND	53	LOG OUT CH2 HI
20	IN CH09	54	LOG OUT CH2 LO
21	GND	55	LOG OUT CH3 HI
22	IN CH10	56	LOG OUT CH3 LO
23	GND	57	PWR OUT CH4 HI
24	IN CH11	58	PWR OUT CH4 LO
25	GND	59	PWR OUT CLAMP 4
26	IN CH12	60	PWR OUT CH5 HI
27	GND	61	PWR OUT CH5 LO
28	IN CH13	62	PWR OUT CLAMP 5
29	GND	63	PWR OUT CLAMP 6
30	IN CH14	64	PWR OUT CH6 HI
31	GND	65	PWR OUT CH6 LO
32	IN CH15	66	PWR OUT CLAMP 7
33	GND	67	PWR OUT CH7 HI
34	IN CH16	68	PWR OUT CH7 LO

2.3 System Configuration

The PCIe-OPTO32C is available in 3 different configurations.

- As a Standard OPTO32 Board with 24 input Channels. See the PCIe-OPTO32C Manual
- As a OPTO32C-12V-CONTACT which is designed to sense contact closures on all 24 inputs. The high side of the Opto-Isolator is connected to +12V through a Current Limiting Resistor.
- As a OPTO32C-12V-CONTACT-8x28V which has channels 0 through 7 configured as standard OPTO Inputs and channels 8 through 23 are configured to sense contact closures.

2.3.1 Standard OPTO32 Input Configuration

Selectable input voltage range thru use of field replaceable bias resistors, labeled RIN, using standard 8 pin SIP isolation resistors. These bias resistor packages are socketed for easy replacement One bias resistor package will affect the input channels on nibble boundaries as follows:

Table 2-3 Input Channels Bias Resistors Locations.

Resistor Location	Input Channels	Configuration
R10	IN CH00 thru IN CH03	Standard
R9	IN CH04 thru IN CH07	Standard
R8	IN CH08 thru IN CH11	Standard
R2	IN CH12 thru IN CH15	Standard
R12	IN CH16 thru IN CH19	Standard
R11	IN CH20 thru IN CH23	Standard

Current Limiting Resistor Values should be chosen to provide a Minimum input current of 2.3 mA. Typical resistor values for input voltage levels are as follows:

Table 2-4 Input Channels Bias Resistor Values

Input Voltage Range	Bias Resistor Values
5 V	2200 ohms
12 V	5100 ohms
28 V	12000 ohms
48 V	20000 ohms

The PCIe-OPTO32C also has the Option of an additional input resistor in parallel with the Standard Resistor for channels IN00 through IN07 ONLY. This additional resistor is provided for higher current applications. Maximum rated Input Current is 80ma.

Table 2-5 Additional Input Channels Bias Resistors Locations.

Resistor Location	Input Channels
R30	IN CH00 thru IN CH03
R31	IN CH04 thru IN CH07

2.3.2 -12V-CONTACT Configurations

When the PCIe-OPTO32C is configured as a –12V-CONTACT then the resistors listed in Tables 2-2 and 2-4 will not be installed and the resistor locations listed in the following table will be used to pull the high side of the OPTO-Isolator to +12V from the PCI bus on all 24 Input Channels. The Standard -CONTACT uses 1.2K 200mw Resistor Packages.

Table 2-6 -12V-CONTACT Current Limiting Resistor Locations.

Resistor Location	Input Channels	Configuration	Value
R20	IN CH00 thru IN CH03	CONTACT	1.2K Ohms 200mw
R21	IN CH04 thru IN CH07	CONTACT	1.2K Ohms 200mw
R22	IN CH08 thru IN CH11	CONTACT	1.2K Ohms 200mw
R23	IN CH12 thru IN CH15	CONTACT	1.2K Ohms 200mw
R24	IN CH16 thru IN CH19	CONTACT	1.2K Ohms 200mw
R25	IN CH20 thru IN CH23	CONTACT	1.2K Ohms 200mw

2.3.3 -12V-CONTACT-8x28V Configurations

When the PCIe-OPTO32C is configured as a –12V-CONTACT-8x28V then the board will be configured as a mixture of inputs with Channels 0-7 configured as Normal Inputs using custom resistors and Channels 8-23 will be configured as -CONTACT Inputs where the high side of the OPTO-Isolator is connected to +12V from the PCI bus through a 1.2K 200mw Resistor Package.

Table 2-7 -12V-CONTACT-8x28V Current Limiting Resistors

Resistor Location	Input Channels	Configuration	Value
R10	IN CH00 thru IN CH03	Standard	2.7K Ohms 400mw
R9	IN CH04 thru IN CH07	Standard	2.7K Ohms 400mw
R22	IN CH08 thru IN CH11	CONTACT	1.2K Ohms 200mw
R23	IN CH12 thru IN CH15	CONTACT	1.2K Ohms 200mw
R24	IN CH16 thru IN CH19	CONTACT	1.2K Ohms 200mw
R25	IN CH20 thru IN CH23	CONTACT	1.2K Ohms 200mw

If the 2.7K 400mw higher power resistor is not available, then 2 x 5.6K 200mw resistors will be used in Parallel using the Additional Input Resistor Locations. The Configuration will be as shown below.

Table 2-8 -12V-CONTACT-8x28V Current Limiting Resistors - Alternate

Resistor Location	Input Channels	Configuration	Value
R10	IN CH00 thru IN CH03	Standard	5.6K Ohms 200mw
R30	IN CH00 thru IN CH03	Standard	5.6K Ohms 200mw
R9	IN CH04 thru IN CH07	Standard	5.6K Ohms 200mw
R31	IN CH04 thru IN CH07	Standard	5.6K Ohms 200mw
R22	IN CH08 thru IN CH11	CONTACT	1.2K Ohms 200mw
R23	IN CH12 thru IN CH15	CONTACT	1.2K Ohms 200mw
R24	IN CH16 thru IN CH19	CONTACT	1.2K Ohms 200mw
R25	IN CH20 thru IN CH23	CONTACT	1.2K Ohms 200mw

2.3.3.1 Channels 0-7

Isolation Voltage – 5000 V
Current Transfer Ratio – 80-600%
Min Input Current – 2.3 mA.
Max Input Current – 80 mA.
Typical Ton/Toff – 3/5 uSec.

Input channels 00-07 can be configured in 3 different ways through the use of optional resistors.
RIN is used for standard OPTO32C configurations.

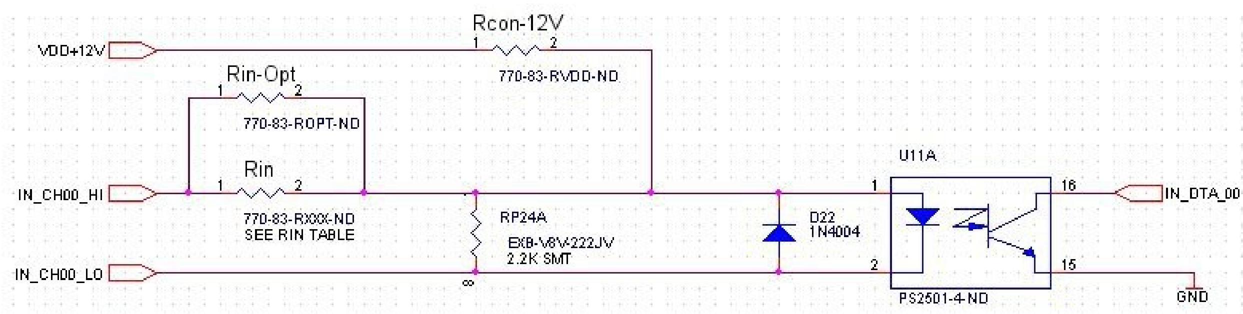
RIN-OPT is used along with RIN for higher current applications.

Rcon-12V is only used for –CONTACT applications. It is NEVER used with RIN or RIN-OPT. It is NEVER used in -12V-CONTACT-8x28V applications.

When configured as a -12V-CONTACT-8x28V Board, RIN Only is used and is a 2.7K 400mw Resistor. If the 2.7K 400mw is not available, then 2 x 5.6K 200mw resistors will be used in parallel and will be installed in RIN and RIN-OPT.

When configured as a -12V-CONTACT Board, Rcon-12V is used and is a 1.2K Ohms 200 mw Resistor Package.

Figure 2 Input Channels 0-7, Typical



2.3.3.2 Channels 8-23

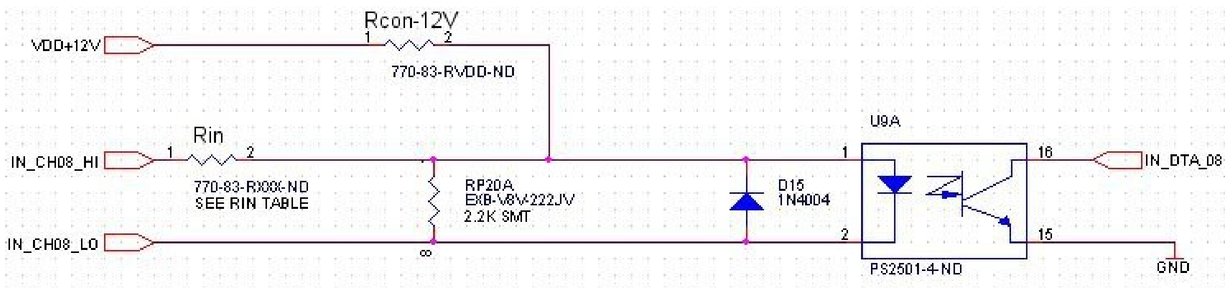
Isolation Voltage – 5000 V
Current Transfer Ratio – 80-600%
Min Input Current – 2.3 mA.
Max Input Current – 80 mA.
Typical Ton/Toff – 3/5 uSec.

Input channels 08-23 can be configured in 2 different ways through the use of optional resistors.
RIN is used for standard OPTO32C configurations.

Rcon-12V is only used for –CONTACT applications. It is NEVER used with RIN.

When configured as a -12V-CONTACT Board, Rcon-12V is used and is a 1.2K Ohms 200 mw Resistor Package.

Figure 3 Input Channels 8-22 Typical



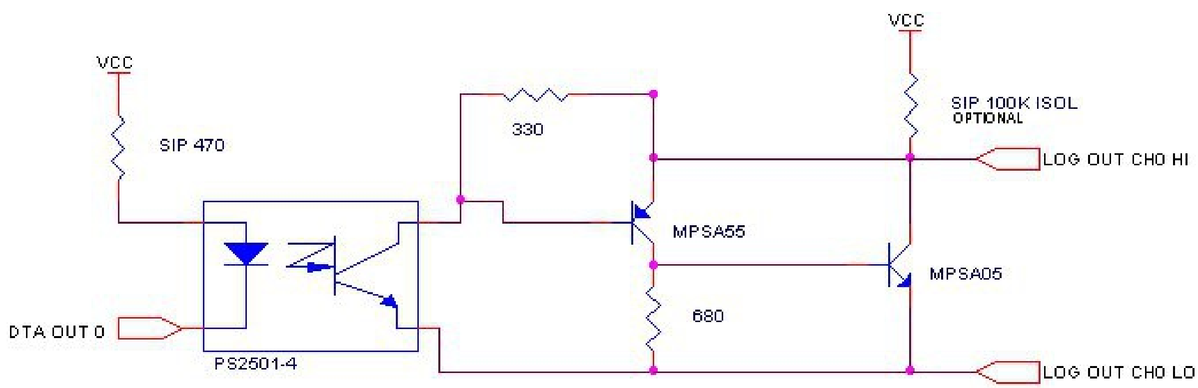
2.3.4 Opto-Isolated Outputs

2.3.4.1 Normal Outputs Bits 0-3

Output Bits 0-3 contain an Optional Pullup resistor to VCC that is not normally installed.

Isolation Voltage – 5000 V
VCEO (Max) – 60 V
Maximum Current – 100 ma.
Typical Ton/Toff – 3/5 uSec.

Figure 4 Normal Outputs, Bits 0-3

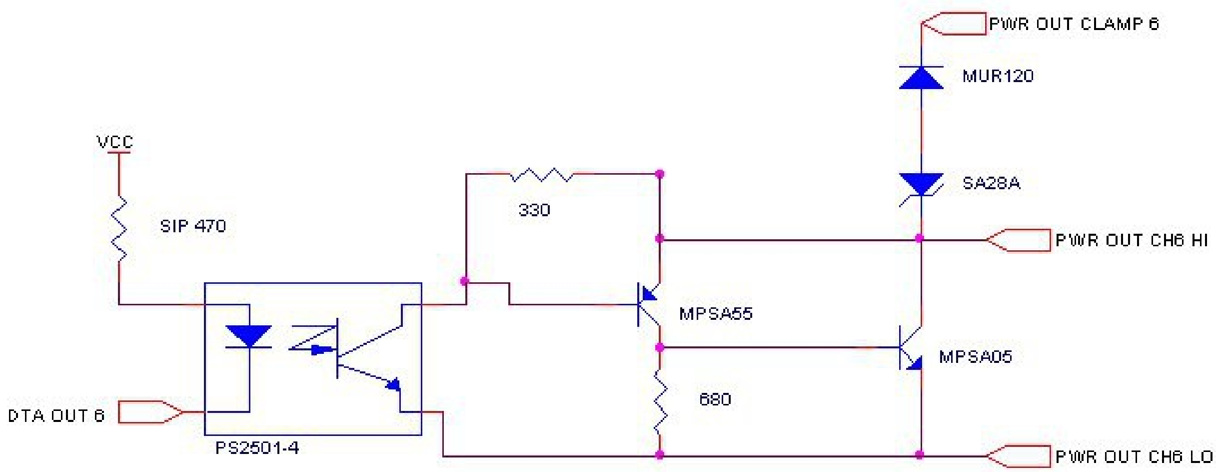


100 K isolation Resistor is Optional and is not normally installed.

2.3.4.2 Diode Clamped Outputs Bits 4-7

Isolation Voltage – 5000 V
VCEO (Max) – 60 V
Maximum Current – 100 ma.
Typical Ton/Toff – 3/5 uSec.

Figure 5 Diode Clamped Outputs, Bits 4-7



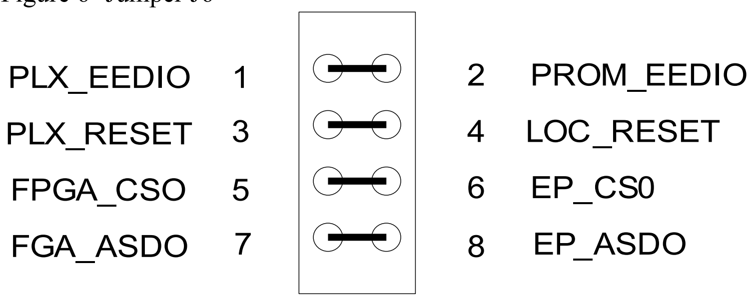
2.3.5 Jumpers

The PCIe-OPTO32C-12V-CONTACT board contains jumpers to support System Configuration and Troubleshooting. The PCIe-OPTO32C also contains jumpers to provide Ground pins to the connector as the return path for the +12V when the board is used in the PCIe-OPTO32C-12V-CONTACT configuration. These jumpers will NEVER be installed for operation as Standard Opto-Isolated inputs. Rin and Rin-OPT MUST ALWAYS be removed for the jumpers and Rcon-12V are installed.

2.3.5.1 J6 – PLX and FPGA Support

Jumper J6 is provided for Factory Troubleshooting and Support of the PLX Interface Chip and the FPGA on the board. All 4 Jumpers should always be installed for proper board operation.

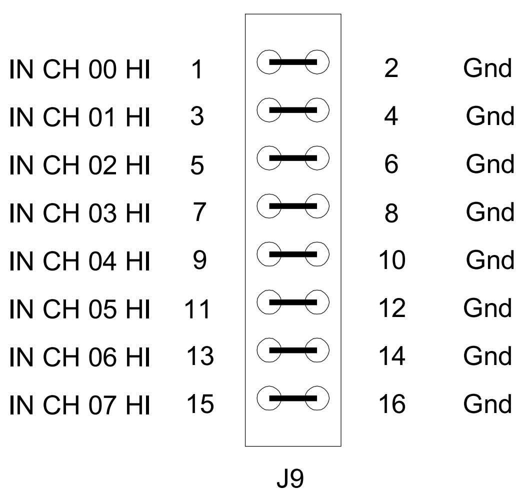
Figure 6- Jumper J6



2.3.5.2 J9 – Channels 00 – 07 - GND

Jumper J9 controls grounding of the Channel HI Pins for input Channels 00 through 07.
Jumper Absent is for normal OPTO-Isolator Operation.
Jumper Present is for –12V-CONTACT operation ONLY. Rin and Rin-OPT MUST be removed before the jumper is installed. :

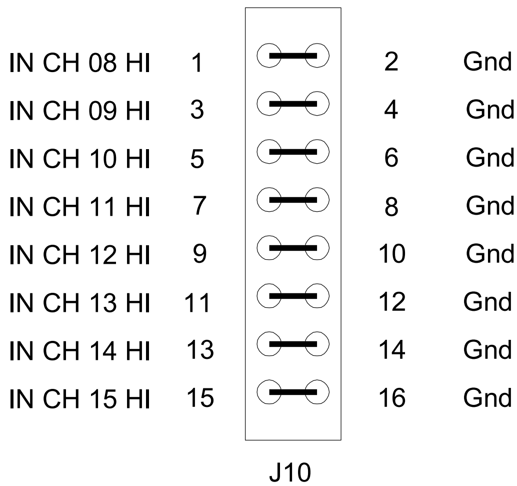
Figure 7- Jumper J9



2.3.5.3 J10 – Channels 08 – 15 - GND

Jumper J10 controls grounding of the Channel HI Pins for input Channels 08 through 15.
Jumper Absent is for normal OPTO-Isolator Operation.
Jumper Present is for –12V-CONTACT operation ONLY. Rin MUST be removed before the jumper is installed. :

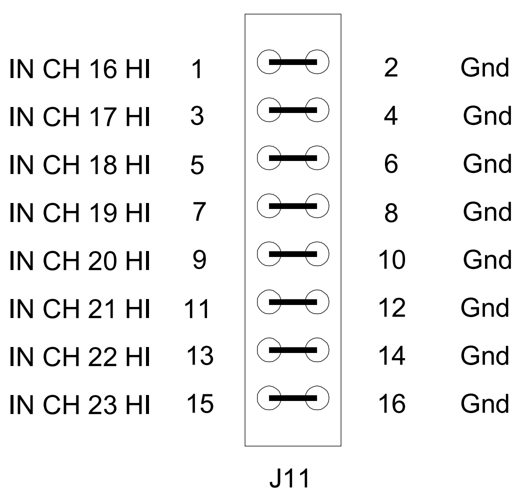
Figure 8 - Jumper J10



2.3.5.4 J11 – Channels 16 – 23 - GND

Jumper J11 controls grounding of the Channel HI Pins for input Channels 16 through 23.
Jumper Absent is for normal OPTO-Isolator Operation.
Jumper Present is for –12V-CONTACT operation ONLY. Rin MUST be removed before the jumper is installed. :

Figure 9 - Jumper J11



2.3.6 Board LED's

The PCIe-OPTO32C-12V-CONTACT Board provides several LED's for monitoring Board Status. The LED's are not required for normal board operation. All LED's are located along the Top edge of the board.

2.3.6.1 D1 – PLX PCIe Link Status – Green.

LED D1 is connected to the GPIO0 line from the PLX PCIe Interface Chip. The Default Power Up function of this line is to Indicate that the PCIe bus link is Good. It can also be placed under Software Control through the PLX 8311 control registers. Default is that this LED is Installed and that GREEN, 'ON', indicates that the PCIe Link is Good. This LED will always be ON during normal board operations.

2.3.6.2 D6 – FPGA Configuration – Red

LED D6 will be ON when the FPGA is NOT Configured. After a successful Configuration this LED will Turn OFF. In Normal Operation this LED will be OFF. This LED is located along the top near the back edge of the board, farthest from the cable connector. At Board Reset, This LED will flicker ON and then turn OFF during normal board operations.

2.3.6.3 D5 – Board Fail LED – Red

LED D5 is under software control through the Board Control Register, Section 3.2.2, Bit 7. The default is that this LED will Reset to the ON State. Writing a '1' to Board Control Register Bit 7 will turn this LED OFF. This LED is located along the top near the middle of the board, between the back edge and the cable connector. At Board Reset, This LED will flicker OFF and then turn ON after the FPGA is configured. After configuration, this LED is under Software Control and may be either ON or OFF .

SECTION 3

3. CONTROL SOFTWARE

3.1 Introduction

3.2 Board Register Descriptions

Table 3-9 Register Address Map

Board Offset	Size	Register Name
0x00	32 Bits Read Only	Board Status Register
0x00	8 Bits Write Only	Board Control Register
0x04	24 bits Read ONLY	Received Data Register
0x08	24 bits Read / Write	Change of State Register
0x0c	16 bits Read / Write	Receive Event Counter
0x010	24 bits Read / Write	COS Interrupt Enable Register
0x014	24 bits Read / Write	COS Polarity Register
0x018	24 bits Read / Write	Clock Division Register
0x01c	8 bits Read / Write	Output Data Register
0x020	32 Bits Read / Write	Test Register 1
0x024	32 Bits Read / Write	Test Register 2

3.2.1 Board Status Register - Board Offset 0x00

32 Bits read only. New with the PCIe-OPTO32C this Register expanded to 32 Bits with Fields to Identify the Firmware Revision Level, and the Board ID. Bits 0-7 are the same as the PCI and PMC OPTO32's.

Table 3-10 Board Status Register

Field	Description
Bit[0]	Int Byte LO Out H = bits 7 - 0 COS interrupt status
Bit[1]	Int Byte MD Out H = bits 15 - 8 COS interrupt status
Bit[2]	Int Byte HI Out H = bits 23 - 16 COS interrupt status
Bit[3]	Rx Event Overflow H = Event Overflow status
Bit[4]	Master Int Out = Master Interrupt Status – 1=Interrupt into the PLX
Bit[5]	Slow Debounce Clock ;
Bit[6]	Enable Rx Event Overflow H = Interrupt Enable for Event Overflow Read Back
Bit[7]	Fail LED ON L – Read Back
	New for the PCIe-OPTO32C.
Bit[15..8]	Reserved – Set to 0x00.
Bit[23..16]	Current Firmware Rev Level - Set to 0x00 for Rev NR.
Bit[31..24]	Board Identifier. Set to 0x02 to Identify the OPTO32C Board Family.

3.2.2 Board Control Register - Board Offset 0x00 -

8 Bits write only. -

Table 3-11 Board Control Register

Field	Description
Bit[0]	Clear Int Byte LO H = clear COS bits 7 - 0
Bit[1]	Clear Int Byte MD H = clear COS bits 15 - 8
Bit[2]	Clear Int Byte HI H = clear COS bits 23 - 16
Bit[3]	Clear Rx Event Overflow H =Clear Event Counter Overflow Status
Bit[4]	Master Clear = - Clear All COS bits and Event Counter Overflow Status bit.
Bit[5]	Reserved
Bit [6]	Enable Rx Event Overflow H - 1 = Interrupt enable.
Bit [7]	Fail LED ON L - 0=LED On / 1 = LED Off

NOTE: Bits 0-4 are self-clearing pulses that are written as a 1 to clear the interrupt source. The bits will then self clear so that another host operation is not required.

NOTE: The Clear COS Bytes, or the Master Clear (bit[4]), will clear ANY COS register bit that is set regardless of the bits Interrupt Enable Status. For Individual COS bit clearing, Write a 1 to the COS bit you wish to clear.

Event Overflow status will only be cleared by Clear Event Overflow or by Master Clear, Bit[4]. Loading the Event Counter WILL NOT clear out the event overflow status.

3.2.3 Received Data Register - Board Offset 0x04

24 bits. Debounced Receive data bits 0 - 23. Read ONLY.

The Input Data Bits, After they have been Debounced

Table 3-12 Received Data Register

Field	Description
23..00	Debounced Receive Data bits 0 - 23. Read ONLY The Debounced Input Data Bits.
31..24	Reserved – Undefined

3.2.4 Change of State Register - Board Offset 0x08

24 bits - Change of State Detected. Polarity programmed thru COS Polarity register, 0x014.

If a COS bit is set, then it will stay set until cleared by the host. A COS bit can be cleared by writing a 1 to a COS bit that is set. Writing a zero will have no effect. Writing a 1to a bit that is 0 will do nothing. COS bits may also be cleared by using the board control register Byte clears or using the board control master clear.

Table 3-13 Change of State register

Field	Description
23..00	Change of State Data bits 0 - 23. Writing a 1 will clear a bit that is set.
31..24	Reserved – Undefined

3.2.5 Receive Event Counter - Board Offset 0x0c

16 bits Read / Write. Reset to Zero.

This counter may be read at any time by the host. Counter will increment once for every Debounced Rising edge detected on input data bit 23. When the counter is 0x0ffff and increments the Rx event overflow status bit will be set and can be used to generate an interrupt.

Table 3-14 Receive Event Counter

Field	Description
15..00	Receive Event Counter
31..16	Reserved – Undefined

3.2.6 COS Interrupt Enable Register - Board Offset 0x010

24 bits. Read / Write. Reset to Zero.

Each bit will be bitwise ANDED with the COS register and all of the results OR'ed together to generate an Interrupt. A 1 will enable the corresponding interrupt. A 0 will disable that bit from generating an interrupt.

Table 3-15 COS Interrupt Enable Register

Field	Description
23..00	COS Interrupt Enable Register 1=Enable Interrupt for that corresponding COS bit.
31..24	Reserved – Undefined

3.2.7 COS Polarity Register - Board Offset 0x014

24 bits. Read / Write. Reset to Zero.

When the corresponding bit is zero, the COS detection for that bit will be set by a detected High to Low transition. When Set to a 1 the COS detection for that bit will look for Low to High transitions. Reset to all zeros.

Table 3-16 COS Polarity Register

Field	Description
23..00	COS Polarity Register - 1=Low to Hi will set COS Bit. 0=Hi to Low will set COS, Per Bit. .
31..24	Reserved – Undefined

3.2.8 Clock Division Register - Board Offset 0x018

24 bits. Read / Write. Reset to Zero.

Table 3-17 Clock Division Register

Field	Description
23..00	Clock Division Register - Sets the Clock Division Rate.
31..24	Reserved – Undefined

NOTE >>>> when altering this register, disable all interrupts and expect unusual results in the COS Detection register.

A 24 Bit clock divider is provided for programmable Debounce delays. The debounce circuit registers the incoming data 3 times in a daisy chain. When ALL 3 registers are high, the incoming data is a high. When the debounced data register contains a 1, then ALL three registers must contain zero for the debounced data to transition back to a zero. The clock for these holding registers is programmable thru the clock divider.

The Basic clock of the board is 20 MHz, 50 Ns. The Basic Clock Counter will always divide by 4, 200 Ns. Values of 0x0000 or 0x0001 will not alter this. When the clock divider is loaded with a larger value then the clock division will be (count * 2) + 2. The Total debounce time will be 3 X (clock division time).

For Example: for a 15ms. debounce time. Clock period should be 5ms.

5ms / 50 Ns = 100000. -2 = 99998.

99998 / 2 = 49999 = 0x0c34f Hex.

3.2.9 Output Data Register - Board Offset 0x01c.

8 bits - Read / Write. Reset to Zero.

The 8 bit output data register. Reset to All Zero's. Writing a 1 to a bit will make that opto output conductive and current will flow from 'HI' to 'LO'. Writing a 0 will turn the opto off and the output will be Non -Conductive from 'HI' to 'LO'

Table 3-18 Output Data Register

Field	Description
07..00	Output Data Register - Controls the Opto-Isolated Outputs. .
31..8	Reserved – Undefined

3.2.10 Test Register 1

32 Bits – Read / Write. Reset to Zero.

32 bit Register does not do anything. It was added to test 8, 16, and 32 Bit Reads and Writes.

Table 3-19 Test Register 1

Field	Description
31:0	Test Register 1 - Can be used for anything.

3.2.11 Test Register 2

32 Bits – Read / Write. Reset to Zero.

32 bit Register does not do anything. It was added to test 8, 16, and 32 Bit Reads and Writes.

Table 3-20 Test Register 2

Field	Description
31:0	Test Register 2 - Can be used for anything.

4. PEX 8311 Notes

The PCIe-OPTO32C uses the PLX Technologies PEX8311AA Interface chip. In the System Devices list this chip will show up as 2 devices, a 8311 PCIe to PCI bridge and a 9056 PCI to local bus adapter.

4.1 Initialization

When the PEX8311 is reset, the 9056 part of the chip will initialize itself from an on board serial EEPROM that is programmed at General Standards. A brief description of some of the Registers follows.

Table 4-21 EEPROM Register Initialization

Eeprom Addr	**PCI Addr**	**Description**	**Value After Reset**
0x00	0x00	Device ID / Vendor ID	0x905610B5
0x44	0x2c	Sub-System ID / Vendor ID	0x347110b5
0x04	0x08	Class Code / Revision	0x078000ba
0x0c	0x78	Mailbox 0	0x00010001
0x10	0x7c	Mailbox 1	0x80010000 – Standard 0x80010001 – Contact 0x80010002 – 8x28v
0x14		Space 0 range PCI to Local	0xffffff80
0x18		Space 0 Base Address (remap)	0x00000001

A list of the full EEPROM contents is located in Appendix B.

4.1.1 Device ID / Vendor ID

Device ID and Vendor ID are used to identify the PLX Device during configuration cycles.

Table 4-22 Device ID / Vendor ID Register Description

Field	Description	Value After Reset
15..00	Vendor ID - Identifies the manufacturer of the device. Defaults to the PCI SIG issued vendor ID of PLX	0x10B5
31..16	Device ID - Identifies the particular device. Defaults to the PLX part number for PCI interface chip.	0x9056

4.1.2 Sub-System ID / Vendor ID

Sub-System ID and Vendor ID are used to identify the PCIe-OPTO32C during configuration cycles.

Table 4-23 Sub-System ID and Vendor ID Register Description

Field	Description	Value After Reset
15..00	Vendor ID - Identifies the manufacturer of the device. Defaults to the PCI SIG issued vendor ID of PLX.	0x10B5
31..16	Sub-System ID - Identifies the particular device. Sub-System ID Assigned to the OPTO32C by PLX.	0x3471

4.1.3 Class Code / Revision

When loaded from the EE Prom this register will identify the device Base Class Code, Sub-Class Code and Revision of the PLX Device. PLX Revision is hard coded in the device.

Table 4-24 Class Code / Revision Register

Field	Description	Value After Reset
07..00	Revision Level of the PLX – currently	0xba
15..00	Register Level Programming Interface - 0x00 - None Defined	0x00
23..16	Sub-Class Code - 0x80 – Other Communications Device	0x08
31..24	Base Class Code 0x07 – Simple Communications Controller	0x07

4.1.4 Mailbox 0

When loaded from the EE Prom, this mailbox is used to contain values to identify the PLD revision, and EE Prom Revision levels of this board.

Table 4-25 Mailbox 0

Field	Description	Value After Reset
15..00	PLD Revision Level – Revision Level of the FPGA on the OPTO32C. Currently 0x0001 = Rev 0-NR .	0x0001
31..16	EE Prom Revision Level – Revision Level of the PLX EEPROM contents. Currently 0x0001 = Rev 0-NR .	0x0001

4.1.5 Mailbox 1

When loaded from the EE Prom, this mailbox register is used to identify the overall Board assembly level, and to Identify this Assembly.

Table 4-26 Mailbox 1

Field	Description	Value After Reset
15..00	Assembly Identifier – 0x0000 Identifies the OPTO32C base board 0x0001 Identifies the OPTO32C-12V-CONTACT 0x0002 Identifies the OPTO32C-12V-CONTACT-8x28V For Legacy Reasons the Assembly Identifier must be 0x0000 for the base OPTO32C Board.	0x0000 – Standard 0x0001 – Contact 0x0002 – 8x28V
31..16	Board Assembly Revision Level Currently 0x8001 = Rev NR of the PCIe-OPTO32C .	0x8001

4.1.6 Address Space 0 Range PCI to Local

Size of the Address Space required for the OPTO32C. The OPTO32C uses 128 Bytes of Memory Space.

Table 4-27 Space 0 Range PCI to Local

Field	Description	Value After Reset
31..00	Address Space 0 Range – Zero's indicate the size in Bytes of the Address Space to be reserved for the Board. Bit 0 Indicates the Board is mapped into Memory Space. The OPTO32C uses 128 Bytes of Memory Space.	0xffffff80

4.1.7 Address Space 0 Base Address (Remap)

There is no address space Remap for the Board. Bit Zero indicates that Address Space 0 is Active for writing to Local Registers on the Board.

Table 4-28 Address Space 0 Base Address (Remap)

Field	Description	Value After Reset
31..00	Address Space 0 Base Address (Remap) 0x01 Bit 0 Indicates that Address Space 0 is Active.	0x00000001

Appendix A

INTERRUPTS:

For Interrupt Operation, the Desired Interrupts are Enabled on the Opto isolator board AND Interrupts MUST be enabled At / Thru the PLX Interface chip. To enable Event Counter Overflow Interrupts, Bit[6] of the Board Control Register must be set to a 1.

```
outportb(Opto_register_base_address + 0x00, 0xc0 );
        // Byte write, Turn LED off, Enable Event Overflow Interrupt.
outportl(Opto_register_base_address + 0x0c, 0x0fffe );
        // Long word write, Event Counter, -2.
        // The Second Rising Edge detected will generate the Interrupt
```

To Enable COS Interrupts, Any / All Desired COS Interrupt bit's are enabled thru the COS Interrupt Enable Register.

```
outportl(Opto_register_base_address + 0x010, 0x08421 ) ;
        // Long word write, Offset 0x010, Enable Interrupts on
        // COS Bit's 0, 5, 10, and 15.
```

All other Machine dependent actions should be taken before the final steps in the process. Make ABSOLUTELY sure that there is NO Pending status laying around that is already setting an interrupt action. Either use the master clear's

```
outportb(Opto_register_base_address + 0x00, 0xdf );
        // Byte write, Turn LED off, Enable Event Overflow Interrupt.
        // Master Clear All COS and Clear the Event Counter overflow .
        // NOTE NOTE NOTE NOTE
        // The Master Clear will Clear ALL COS Bits.
        // The Byte Clear's will ALSO Clear ALL COS Bits in that Byte.
        // To Only Clear the Bit generating the Interrupt,
        // you must use the individual Clear's as
        // Described below.
```

Or, Individual Clears for the COS and Event Overflow.

```
Outportl(Opto_register_base_address + 0x08, 0x08421 ) ;
        // Long word write, Offset 0x08, COS register, Clear
        // COS Bit's 0, 5, 10, and 15. If they are set.

Outportb(Opto_register_base_address + 0x00, 0xc8 );
        // Byte write, Turn LED off, Enable Event Overflow Interrupt.
        // Clear Event Overflow
```

The final step is the write to the PLX interface that will enable it to generate Interrupts onto the PCI bus.

```
Outportl(PLX_io_base_address + 0x068, 0x00900 );
        // Long word write, PLX interrupt control register,
        // Bit's 8 and 11, Enable Local input to generate PCI interrupts
```

In the Interrupt Handler, there is NO action required to / with the PLX Interface chip. The only requirement to remove the Asserted interrupt is to remove the Local source of the interrupt. Which would be the COS bit or the event overflow.

```
temp = inportb(Opto_register_base_address + 0x00 ) ;
        // Read the OPTO Board Status register
if ( (temp & 0x010) == 0x010 )
        {
                // Master Interrupt bit will be set in the Board Status
                // Register if this board generated the Interrupt.
                // Status Bits 0 thru 3 could also be examined to
                // Determine Which Byte generated the Interrupt
                // Or if the Event Counter Overflow generated
                // The Interrupt.
                .
                .
                .
                .
                // Finished processing, Now It's time to clear the
                // Pending Interrupt.

        Outportl(Opto_register_base_address + 0x08, 0x08421 ) ;
                // Long word write, Offset 0x08, COS register, Clear
                // COS Bit's 0, 5, 10, and 15. If they are set.

        Outportb(Opto_register_base_address + 0x00, 0xc8 );
                // Byte write, Turn LED off, Enable Event Overflow Interrupt.
                // Clear Event Overflow
        }
```

To Disable All Interrupt's From the OPTO board, write to the PLX interface Chip.

```
Outportl(PLX_io_base_address + 0x068, 0x0000 );
        // Long word write, PLX interrupt control register,
        // Clear Bit's 8 and 11, disable All PCI interrupts
```

Appendix B

PLX EEPROM Contents:

The Full contents of the OPTO32C EEPROM for the 9056 portion of the interface chip are as follows.

Table B-29 PLX EEPROM Contents

Eeprom Addr	**Description**	**Value After Reset**
0x00	Device ID / Vendor ID	0x905610B5
0x04	Class Code / Revision	0x07800002
0x08	Max / Min Latency / Int. Pin / Int. Line Routing Value	0x00000100
0x0c	Mailbox 0 User defined	0x00010001
0x10	Mailbox 1 User defined	0x80010000 – Standard 0x80010001 – Contact 0x80010002 – 8x28v
0x14	Space 0 range PCI to Local	0xffffff80
0x18	Space 0 Base Address (remap)	0x00000001
0x1c	Mode / DMA Arbitration register	0x01200000
0x20	VPD Boundary -Big / Little Endian descriptor	0x00300500
0x24	Expansion ROM Range – Not Used	0x00000000
0x28	Expansion ROM Re-Map – Not Used	0x00000000
0x2c	Space 0 / Expansion ROM Descriptor	0x42000140
0x30	Direct Master to PCI Range – Not Used	0x00000000
0x34	Direct Master to PCI Local Base Address – Not Used	0x00000000
0x38	Direct Master to PCI IO/CFG Base Address -Not Used	0x00000000
0x3c	Direct Master to PCI Memory Re-Map – Not Used	0x00000000
0x40	Direct Master to PCI IO/CFG PCI – Not Used	0x00000000
0x44	Sub-System ID / Vendor ID	0x347110b5
0x48	Space 1 range PCI to Local – Not Used	0x00000000
0x4c	Space 1 Base Address (remap) – Not Used	0x00000000
0x50	Space 1 Descriptor – Not Used	0x00000000
0x54	Hot Swap Control	0x00004c06
0x58	PCI Arbiter Control	0x00000000
0x5c	PM Capabilities	0x00024801
0x60	PM Control / Status	0x00000000