General Standards Corporation
High Performance Bus Interface Solutions

PCIe-24DSI64C200K

24-Bit, 64-Channel, 250KSPS, PCI-Express Module

With 64 Differential Delta-Sigma Input Channels

Available also in PCI and Compact PCI form factors as:

PCI64-24DSI64C:	**PCI**, full length
cPCI6U64-24DSI64C:	**cPCI**, 6U

Features Include:

- 64 differential 24-Bit simultaneously-sampled analog input channels. Optional 48 and 32 channel versions also available.
- Input sample rates from 1KSPS to 250KSPS per channel.
- Fixed input range available from ±1V to ±10V. Call for availability of a specific range.
- Delta-Sigma input conversion minimizes or eliminates the need for antialias filtering.
- Precision DC characteristics as well as wide dynamic range AC performance.
- 256K-sample analog input FIFO buffer.
- Typical dynamic range of 103dB; 112dB with 10kHz host-software postfilter.
- Continuous and Burst (one-shot) sampling modes.
- Sample clock source selected as internal or external.
- Supports multiboard synchronization of analog inputs. Low channel skew.
- On-demand internal offset and gain autocalibration of all analog inputs.
- 4-Bit bi-directional digital TTL port.
- High-density Front-Panel system I/O connections.
- PCI Express control interface, single-lane.
- Available in PMC or XMC form factors with reduced channel-count.

Applications:

- ✓ Sonar Arrays
- ✓ Analog Inputs
- ✓ Voltage Acquisition
- ✓ Acoustic Research
- ✓ Phase Comparison
- ✓ Audio Waveform Analysis

--- PRELIMINARY ---

REV: 071918

Overview:

The 64-channel PCIe-24DSI64C200K analog input module provides high-density 24-bit analog input resources on a standard PCI Express module. Optimized for flexibility and performance, the board is ideal for a wide variety of applications, ranging from precision voltage measurements, to the analysis of complex acoustic signals and waveforms.

Functional Description:

Each of 64 analog input channels contains a delta-sigma A/D converter that provides inherent antialias suppression and sharp-cutoff digital lowpass filtering. The digital filter can be software-configured either as a fast low-latency filter, or as a wideband low-ripple sharp-cutoff filter for maximum antialiasing.

An internal voltage reference can be applied through all channels to support selftest operations and autocalibration. Gain and offset trimming is performed by applying correction values that are determined during on-demand autocalibration. A linear-phase digital antialiasing filter rejects out-of-band signals, and a simple lowpass analog filter reject those interference signals that fall within the harmonic images of the digital filter.

ADC clocking is obtained either from an external hardware source, or from an internal sample-rate generator. The internal generator is adjustable over a 2:1 frequency range, and is divided down within the local controller to provide sample rates from 1.0 KSPS to 250 KSPS. Conversion data is transferred to the PCI Express bus through a 256 K-sample data buffer that is supported by two DMA channels. Multiple boards can be synchronized to perform simultaneous sampling with external sync and clock connections. Burst acquisition is supported.
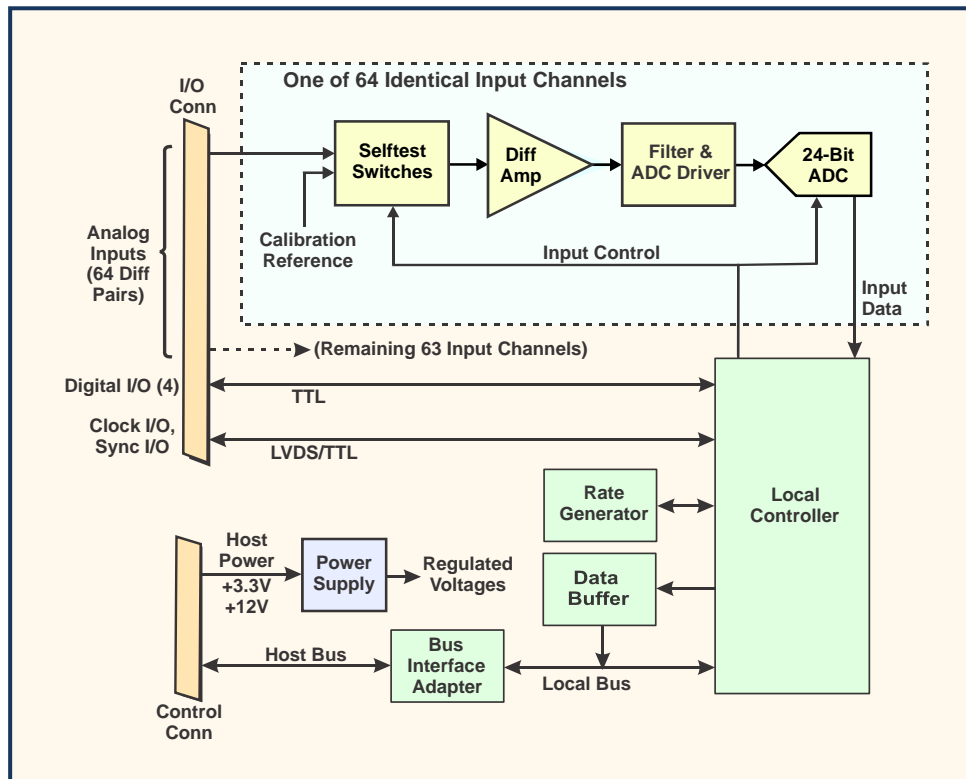

Figure 1. PCIe-24DSI64C200K; Functional Organization

This product is functionally compatible with the PCI Express Specification revision 1.0a. System input/output connections are made at the front panel through a high-density I/O connector. Power requirements consist of +3.3 VDC and +12 VDC, in compliance with the PCI Express specification, and operation over the specified temperature range is achieved with conventional air cooling.

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FUNCTIONAL SPECIFICATIONS

Typical at +25 ^{O}C, with specified operating conditions.

Input Characteristics:

Configuration:	64 differential input channels; 48-channel and 32-channel configurations also available.
Voltage Range:	Factory-Configurable as ±1.5V or ±10V; Contact Sales for availability of custom ranges from ±1V to ±10V.
Input Impedance:	Signal to analog ground: 1.0 Megohm in parallel with 40 pF, typical. Signal HI to Signal_LO: 2.0 Megohms in parallel with 40pF, typical.
Common Mode Rejection:	62dB to 15kHz on the ±10V range; typical.
Common Mode Range:	Fullscale range ±1.0V with zero normal-mode signal. e.g.: ±11V for the ±10V range.
Overvoltage Protection, Line to Ground:	±5V to ±10V ranges: ±24-Volts with power applied; ±10 Volts with power removed. Ranges less than ±5V: ±18-Volts with power applied; ±10 Volts with power removed

Transfer Characteristics:

Conversion Architecture:	24-Bit Delta-Sigma.
Sample Rate:	1-250 kilosamples per second per channel
Oversampling Factor:	Software-selectable as x32, x64, x128, x1024

DC Accuracy:
(Mean composite error after autocalibration)

Input Range	Midrange (Zero) Accuracy	Gain Accuracy
±10V	±0.9 mV	±4.0 mV
±1.5V	±0.4 mV	±1.4 mV
±1.0V	±0.3 mV	±1.0 mV

Wideband Filter [1]: Typical Characteristics:

-3dB bandwidth:	0.43 * Fsamp [2]
Stopband Freq:	0.49 * Fsamp
Stopband Atten:	105 dB
Group Delay: [3]	34/Fsamp
Settling Time:	68/Fsamp, 1 LSB

Low-Latency (Sinc) Filter [1]: Typical Characteristics:

-3dB bandwidth:	0.2 Fsamp [2]
Group Delay: [3]	3/Fsamp
Settling time:	7/FSamp, 1 LSB

Phase Skew:	Typically less than 55ns (0.1-Degree for Fsig = 5kHz), with Fsig/Fsamp <0.35; channel-channel (board-board for multiboard configurations), excluding noise, with high-frequency image filter.
No Missing Codes	24 Bits.
Integral Nonlinearity (INL)	0.001 percent of fullscale range.
Dynamic Range:	Wideband Filter (Typ): 103dB. Low-Latency Filter (Typ): 105dB.
SINAD:	Wideband Filter (Typ): 102dB. Low-Latency Filter (Typ): 103dB.
Interchannel Crosstalk:	-96 dB typical to 50 kHz
Antialias Filtering:	Each ADC provides digital lowpass filtering as indicated above for "Wideband" and "Low Latency" filters. In addition to the digital filter, a 1st-order lowpass analog image filter in each channel provides a -3 dB cutoff frequency of approximately 500kHz to suppress images from the digital filter. Optional alternative image filter frequencies are available.

[1] Software-selectable.
[2] Fsamp equals the output data rate (ODR).
[3] Group delay is equivalent to Latency.

Operating Modes and Controls:

Organization:	All active input channels operate at the same sample rate, controlled by division of an internal or external rate generator frequency.
Sampling Clock I/O:	The sampling clock can be derived either from an internal rate generator, or from a LVDS or TTL external hardware input. Multiple boards can be locked to a common clock by multidropping ('star' configuration) the output clock from an external source to the input clocks of all active boards.
Internal Rate Generator:	An internal PLL rate generator and a frequency divider provide sample rates from 1.0 KSPS to 250 KSPS. The frequency of the generator is controlled by the ratio of two 10-Bit integers, and by a **reference frequency** of 32.768 MHz. Setting accuracy is 25 PPM; Frequency alternatives are available optionally.
Synchronization:	'Star-configuration' hardware sync inputs can be used to synchronize sampling among multiple boards.
Channel Grouping:	Input channels are partitioned into 8-channel groups. Each group can be independently selected as active or inactive. Inactive channel data does not appear in the input buffer. All active groups share the same sample rate.
Burst Timing:	Triggered-burst sampling can be initiated either internally from an internal rate generator, or externally using the Sync input.
Data Format:	Software-selectable as either offset binary or two's complement. Width of the data field is selectable as 16, 18, 20 or 24 bits.
Channel Tags:	A 6-bit channel tag is appended to each input data value.
Buffer Access:	The input buffer FIFO is accessed through either of two DMA channels, with both block-mode and demand-mode transfers supported.
Auxiliary External Sync I/O:	A 6-pin 'AUX' connector provides external clock and sync I/O capability within the enclosure.

PCIe Compatibility:

Conforms to PCI Express Specification revision 1.0a.
DMA transfers as bus master with two DMA channels.

Power Requirements:

+3.3VDC ±0.2 VDC from the PCIe bus, 1.5 Amps typical, 2.0 Amps maximum.
+12VDC ±0.4 VDC from the PCIe bus, 1.7 Amps typical, 2.1 Amps maximum.
Total power consumption: 23 Watts typical, 27 Watts maximum.

Physical Dimensions:

Height: 106.7 mm (4.20 in)
Depth: 312.0 mm (12.28 in)
Width: 21.6 mm (0.85 in)

Environmental Specifications:

Ambient Temperature Range:

Standard Temperature:	Operating: 0 to +70 Degrees Celsius * Storage: -40 to +85 Degrees Celsius
Extended Temperature:	Operating: -40 to +80 Degrees Celsius * Storage: -40 to +85 Degrees Celsius
	* Air temperature at board surface.
Relative Humidity:	0 to 95%, non-condensing
Altitude:	Operation to 10,000 ft.
Cooling:	Conventional air cooling; 150 LFPM

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Ordering Information:

Specify the basic product model number followed by an option suffix "-A-B-C-D-E", as indicated below. For example, model number **PCIe-24DSI64C200K-64-10V-500K-SRF-0** describes a PCI Express module with 64 input channels, ±10V input range, standard 500 kHz low-pass image filter, standard 32.768 MHz reference frequency, and no custom features. For industrial (extended) temperature operation, add "-I" at the end of the model number.

Optional Parameter	Value	Specify Option As:
Number of Input Channels	**64 Channels**	**A = 64**
	48 Channels	**A = 48**
	32 Channels	**A = 32**
Input Range:	**±1.5V**	**B = 1.5V**
	±10V	**B = 10V**
	Custom Ranges (±1V to ±10V)	**B=xxV (xx= ± range)**
Image Filter Frequency: [1]	**500 kHz**	**C = 500K**
	Custom frequency (kHz)	**C = xxxK**
Reference Frequency: [2]	**32.768 MHz (Standard reference frequency)**	**D = 32.768M or SRF**
	Custom frequency (MHz)	**D = xx.xxxM**
Custom Feature: [3]	**---**	**E = 0**

[1] Image filter frequency. 20-2000 kHz; ±20% frequency accuracy.
[2] Rate generator reference frequency. 30-40MHz MHz; ±0.01% frequency accuracy.
[3] Contact Sales for availability of custom features.

SYSTEM I/O CONNECTIONS

Table 2. System I/O Connector Pin Functions.

| P4			P4		P3			P3	
Pin	Signal		Pin	Signal	Pin	Signal		Pin	Signal
43	DGND		---	---	43	DGND		---	---
42	DGND		85	DGND	42	DGND		85	DIO_00
41	CLK_INP_LO		84	CLK_INP_HI	41	DGND		84	DIO_01
40	CLK_OUT_LO		83	CLK_OUT_HI	40	DGND		83	DIO_02
39	SYNC_INP_LO		82	SYNC_INP_HI	39	DGND		82	DIO_03
38	SYNC_OUT_LO		81	SYNC_OUT_HI	38	DGND		81	DGND
37	AGND		80	AGND	37	AGND		80	AGND
36	IN_LO_00		79	IN_HI_00	36	IN_LO_32		79	IN_HI_32
35	IN_LO_01		78	IN_HI_01	35	IN_LO_33		78	IN_HI_33
34	IN_LO_02		77	IN_HI_02	34	IN_LO_34		77	IN_HI_34
33	IN_LO_03		76	IN_HI_03	33	IN_LO_35		76	IN_HI_35
32	IN_LO_04		75	IN_HI_04	32	IN_LO_36		75	IN_HI_36
31	IN_LO_05		74	IN_HI_05	31	IN_LO_37		74	IN_HI_37
30	IN_LO_06		73	IN_HI_06	30	IN_LO_38		73	IN_HI_38
29	IN_LO_07		72	IN_HI_07	29	IN_LO_39		72	IN_HI_39
28	AGND		71	AGND	28	AGND		71	AGND
27	IN_LO_08		70	IN_HI_08	27	IN_LO_40		70	IN_HI_40
26	IN_LO_09		69	IN_HI_09	26	IN_LO_41		69	IN_HI_41
25	IN_LO_10		68	IN_HI_10	25	IN_LO_42		68	IN_HI_42
24	IN_LO_11		67	IN_HI_11	24	IN_LO_43		67	IN_HI_43
23	IN_LO_12		66	IN_HI_12	23	IN_LO_44		66	IN_HI_44
22	IN_LO_13		65	IN_HI_13	22	IN_LO_45		65	IN_HI_45
21	IN_LO_14		64	IN_HI_14	21	IN_LO_46		64	IN_HI_46
20	IN_LO_15		63	IN_HI_15	20	IN_LO_47		63	IN_HI_47
19	AGND		62	AGND	19	AGND		62	AGND
18	IN_LO_16		61	IN_HI_16	18	IN_LO_48		61	IN_HI_48
17	IN_LO_17		60	IN_HI_17	17	IN_LO_49		60	IN_HI_49
16	IN_LO_18		59	IN_HI_18	16	IN_LO_50		59	IN_HI_50
15	IN_LO_19		58	IN_HI_19	15	IN_LO_51		58	IN_HI_51
14	IN_LO_20		57	IN_HI_20	14	IN_LO_52		57	IN_HI_52
13	IN_LO_21		56	IN_HI_21	13	IN_LO_53		56	IN_HI_53
12	IN_LO_22		55	IN_HI_22	12	IN_LO_54		55	IN_HI_54
11	IN_LO_23		54	IN_HI_23	11	IN_LO_55		54	IN_HI_55
10	AGND		53	AGND	10	AGND		53	AGND
9	IN_LO_24		52	IN_HI_24	9	IN_LO_56		52	IN_HI_56
8	IN_LO_25		51	IN_HI_25	8	IN_LO_57		51	IN_HI_57
7	IN_LO_26		50	IN_HI_26	7	IN_LO_58		50	IN_HI_58
6	IN_LO_27		49	IN_HI_27	6	IN_LO_59		49	IN_HI_59
5	IN_LO_28		48	IN_HI_28	5	IN_LO_60		48	IN_HI_60
4	IN_LO_29		47	IN_HI_29	4	IN_LO_61		47	IN_HI_61
3	IN_LO_30		46	IN_HI_30	3	IN_LO_62		46	IN_HI_62
2	IN_LO_31		45	IN_HI_31	2	IN_LO_63		45	IN_HI_63
1	AGND		44	AGND	1	AGND		44	AGND
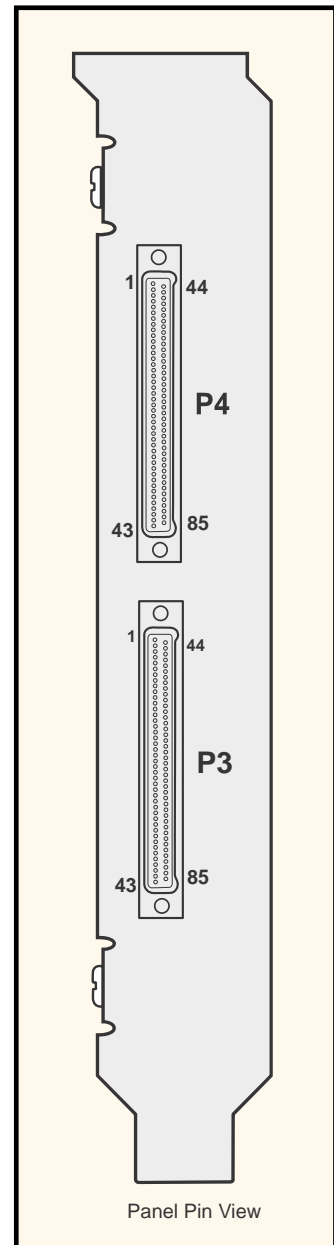
Figure 2. Panel Bracket

System I/O Mating Connector:
Omnetics # MNPO-85-DD-N-EJS-C,
dual-row, straight tail.
(Assembled cables available)

SYSTEM I/O CONNECTIONS (Continued)

Table 2. Sync-I/O Pin Functions

SYNC-I/O Conn Pin	Signal
1	DIG RTN
2	AUX CLOCK
3	DIG RTN
4	AUX SYNC
5	DIG RTN
6	Reserved. Connect to INPUT RTN or leave disconnected.

Recommended Sync-I/O mating
connector: Molex# 51146-0600.