General Standards Corporation

High Performance Bus Interface Solutions

Rev: 031521

PMC66-24DSI16WRC

24-BIT, SIXTEEN-CHANNEL, WIDE-RANGE, 105 KSPS DELTA-SIGMA ANALOG INPUT PMC MODULE

REFERENCE MANUAL

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

LIST OF ILLUSTRATIONS

LIST OF TABLES

SECTION 1.0

INTRODUCTION

1.1 General Description

The PMC66-24DSI16WRC module provides wide-range 24-bit analog input capability in the single-width PMC form factor at sample rates up to 105 KSPS per channel. In addition to providing sixteen analog input channels, this product supports multiboard clocking and synchronization. Input ranges are software-selectable from ±100mV to ±10V. The module is functionally and electrically compatible with the IEEE PCI local bus specification Revision 2.3. Power requirements consist of +5 VDC in accordance with the PCI specification, and operation over the specified temperature range is achieved with nominal air cooling. Specific details pertaining to performance are contained in the PMC66-24DSI16WRC product specification.

This product is designed for minimum off-line maintenance. Internal selftest switches permit the calibration and signal integrity of each channel to be verified by the host. An on-demand autocalibration function calibrates all input channels to a single precision internal voltage reference. System input and output connections are made through an 80-Pin dual-ribbon cable connector. Figure 1.1 represents the physical configuration of the module.

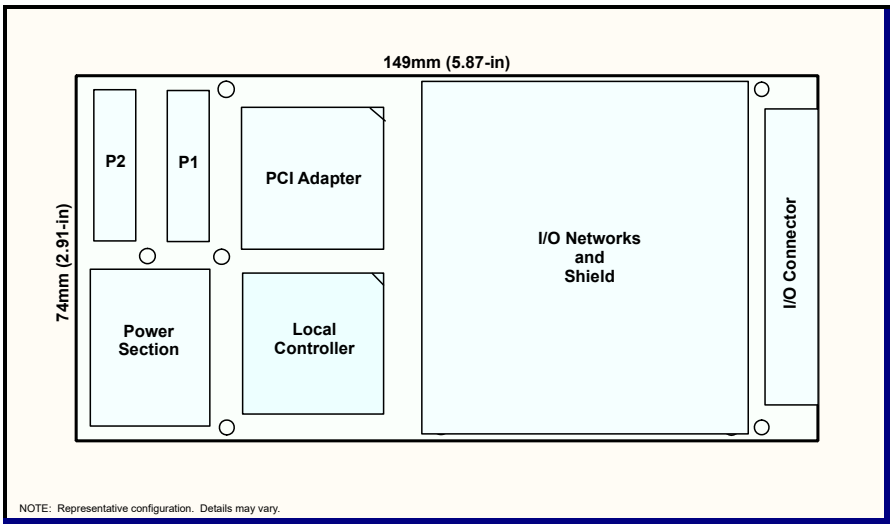

Figure 1.1. Physical Configuration

1.2 Functional Overview

A PCI interface adapter provides the interface between the controlling PCI bus and the internal local controller through a 32-bit local bus (Figure 1.2). Each input channel contains a dedicated scaling instrumentation amplifier and a 24-Bit delta-sigma A/D converter (ADC) that support high-resolution data acquisition over a wide range of input levels.

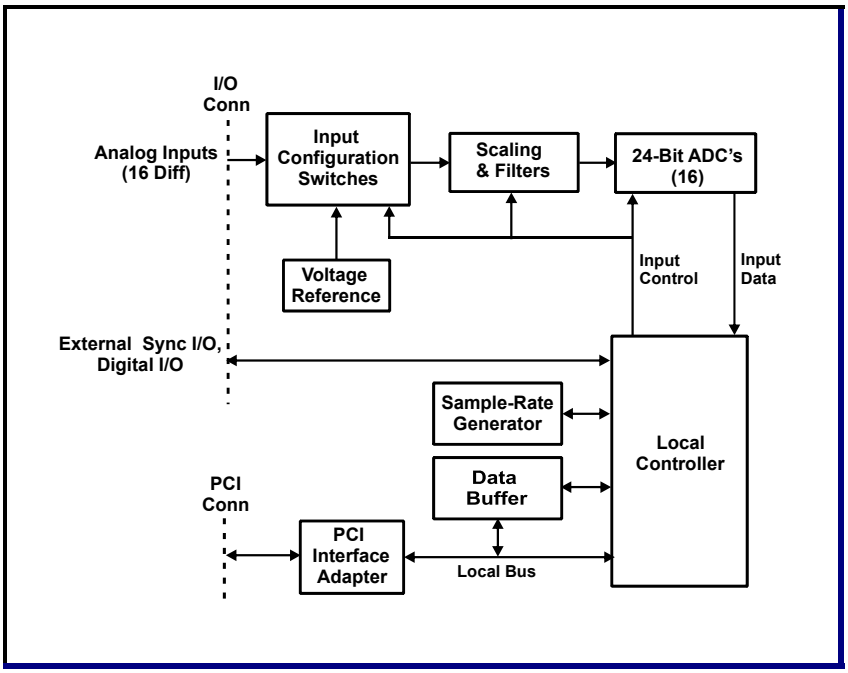

Figure 1.2. Functional Organization

An internal sample-rate clock generator uses the master-clock oscillator to provide sample rates from 0.2 KSPS to 105 KSPS, or an external clock source can control the sample rate over the same range. The input bandwidth extends down to DC. Conversion data from all active channels is transferred to the PCI bus through a 256K-sample FIFO data buffer.

Multiple boards can be synchronized to perform sampling in "lockstep", either by a software command, or by external hardware sync and clock input signals. Hardware sync and clock input/output signals permit multiple boards to be connected together for phase-locked operation from a common clock. The master clock frequency can be software-adjusted approximately 80PPM to either side of the nominal value.

SECTION 2.0
INSTALLATION AND MAINTENANCE

2.1 Board Configuration

This product has no field-alterable electrical or mechanical features, and is completely configured at the factory.

2.2 Installation

2.2.1 Physical Installation

To minimize the opportunity for accidental damage before installation, the module should be stored in the original protective shipping envelope. System power must be turned OFF before proceeding with the installation.

CAUTION: This product is susceptible to damage from electrostatic discharge (ESD). Before removing the module from the conductive shipping envelope, ensure that the work surface, the installer and the host equipment have been properly discharged to ground.

After removing the board from the shipping envelope, position the board with the two mezzanine connectors P1 and P2 facing the mating connectors J1 and J2 on the host board (Figure 2.2-1). Then carefully press the board into position on the host. Verify that the mezzanine connectors have mated completely and that the board is seated firmly against the host board. Attach the board to the host with 2.5 x 6.5mm panhead screws. Pass the screws through the host board into the corresponding mounting holes in the standoffs and front-panel bezel. Tighten the screws carefully to complete the installation. Do not overtighten.

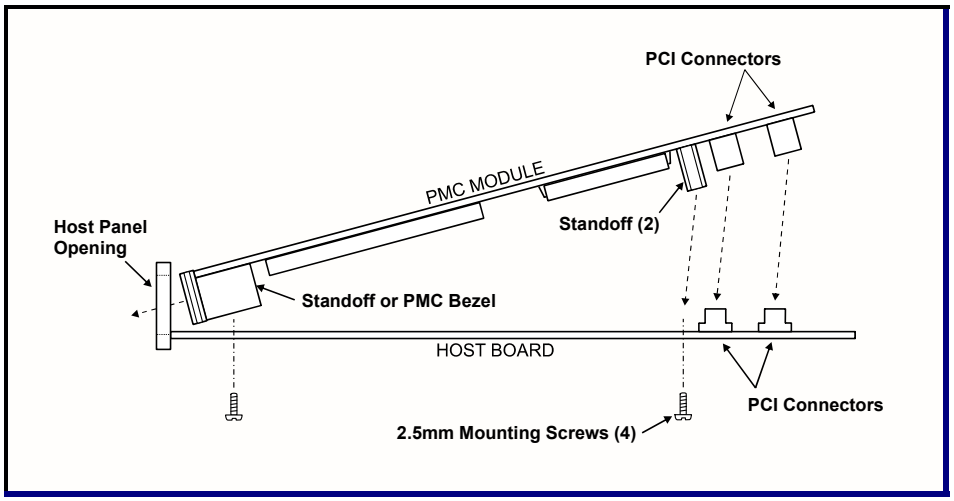

Figure 2.1. Physical Installation

NOTE: The 16-Channel version of this product requires forced-air cooling at the rate of 150 linear feet per minute (LFPM).

2.2.2 Input/Output Cable Connections

System cable signal pin assignments are listed in Table 2.2.2-1. Unused input pins may be left disconnected in most applications. However, if very long cables are used or if excessive cable noise is anticipated, the unused analog inputs should be grounded to the input return to minimize the injection of noise into the board.

The system I/O connector is designed to mate with an 80-pin dual-ribbon connector, equivalent to Robinson Nugent Model P50E-80S-TG, or equivalent. This insulation displacement (IDC) cable connector accepts two 40-wire 0.050-inch ribbon cables, with the pin numbering convention shown in Table 2.2.2-1 and in Figure 2.2.2. Contact the factory if prewired cables are required.

Table 2.2.2-1. System Connector Pin Assignments

ROW-A			ROW-B	
PIN	SIGNAL		PIN	SIGNAL
1	INP00 LO		1	INP09 LO
2	INP00 HI		2	INP09 HI
3	INPUT RTN		3	INPUT RTN
4	INPUT RTN		4	INPUT RTN
5	INP01 LO		5	INP10 LO
6	INP01 HI		6	INP10 HI
7	INPUT RTN		7	INPUT RTN
8	INPUT RTN		8	INPUT RTN
9	INP02 LO		9	INP11 LO
10	INP02 HI		10	INP11 HI
11	INPUT RTN		11	INPUT RTN
12	INPUT RTN		12	INPUT RTN
13	INP03 LO		13	INP12 LO
14	INP03 HI		14	INP12 HI
15	INPUT RTN		15	INPUT RTN
16	INPUT RTN		16	INPUT RTN
17	INP04 LO		17	INP13 LO
18	INP04 HI		18	INP13 HI
19	INPUT RTN		19	INPUT RTN
20	INPUT RTN		20	INPUT RTN
21	INP05 LO		21	INP14 LO
22	INP05 HI		22	INP14 HI
23	INPUT RTN		23	INPUT RTN
24	INPUT RTN		24	INPUT RTN
25	INP06 LO		25	INP15 LO
26	INP06 HI		26	INP15 HI
27	INPUT RTN		27	INPUT RTN
28	INPUT RTN		28	INPUT RTN
29	INP07 LO		29	DIG IO 00
30	INP07 HI		30	DIGITAL RTN
31	INPUT RTN		31	DIG IO 01
32	INPUT RTN		32	DIGITAL RTN
33	INP08 LO		33	DIG IO 02
34	INP08 HI		34	DIGITAL RTN
35	INPUT RTN		35	DIG IO 03
36	DIGITAL RTN		36	DIGITAL RTN
37	EXT CLK INP LO		37	EXT CLK OUT LO
38	EXT CLK INP HI *		38	EXT CLK OUT HI *
39	EXT SYNC INP LO		39	EXT SYNC OUT LO
40	EXT SYNC INP HI *		40	EXT SYNC OUT HI *

* TTL signal levels when TTL sync I/O is selected. Otherwise LVDS.

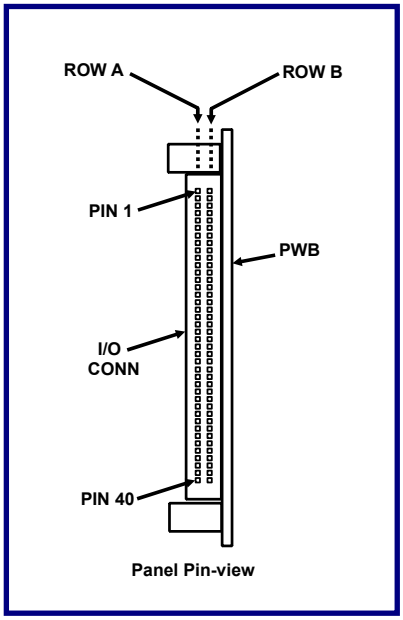

Figure 2.2.2. System I/O Connector

System Mating Connector:

Standard 80-pin 0.050" dual-ribbon socket connector:

Robinson Nugent **P50E-080S-TG**
or equivalent.

A second I/O connector is located on the back of the module (Side-2), and provides an external TTL clock and sync interface for implementation within the equipment enclosure. Table 2.2.2-2 identifies the pin assignments for this Auxiliary Sync I/O connector

Table 2.2.2-2. Auxiliary Sync Connector Pin Assignments

PIN	SIGNAL
1	DIGITAL RTN
2	AUX CLOCK
3	DIGITAL RTN
4	AUX SYNC
5	DIGITAL RTN
6	Reserved. Ground or leave disconnected.

Recommended mating cable connector is Molex# 51146-0600.

2.3 Analog Input Configuration

The analog inputs are configured as sixteen differential input pairs. Differential operation provides the highest noise immunity, and is recommended for the majority of applications. Pull-down resistors are provided on all analog inputs. Although the input configuration is differential, single-ended signal sources can be accommodated as described in Paragraph 2.3.2.

2.3.1 Differential Inputs

Differential operation is essential when the input source returns are at different potentials. This operating mode also offers the highest rejection of the common mode noise that is characteristic of long unshielded cables. When operating in the differential mode, shown in Figure 2.3.1a, the wire pair from each signal source is connected between the HI(+) and LO(-) inputs of a single input channel. The input return should be connected to system ground (remote common) as closely as possible to the input sources. The average HI/LO signal level relative to the input return is the common mode voltage **Vcm** which, for optimum performance, must not exceed the maximum value indicated in the product specification. (**Vcm** actually is the *mean value* of the HI and LO inputs relative to INPUT RTN, but is shown here for simplicity as the potential between the LO input and INPUT RTN.)

2.3.2 Single-Ended Input Sources

Single-ended signal sources can be accommodated as shown in Figure 2.3.1b, with the signal line connected to INP XX HI, and the associated INP XX LO input connected to INPUT RTN at the source. The single-ended operating connection provides suitable performance only when the input signal sources either are isolated from each other, or are common to a single isolated signal return.

CAUTION: If a significant potential difference exists between the remote signal return and INPUT RTN, a low impedance between the two returns can cause excessive current to flow, which in turn can cause erroneous measurements or possible damage to the board. Return-current should be controlled to less than a few milliamps for best performance, and to less than 100 milliamps to avoid damage.

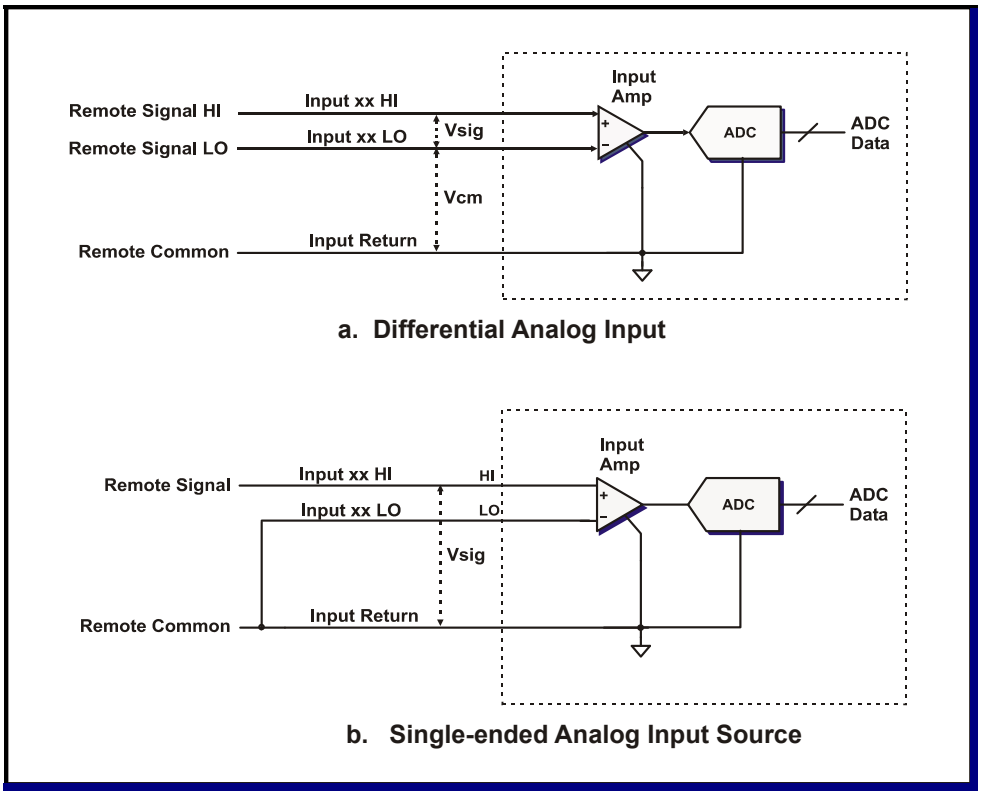

Figure 2.3.1. Input Configurations

2.4 Multiboard Clocking and Synchronization

Analog input converters on multiple boards can be:

a. Clocked from a single clock source (Multiboard clocking), and/or:

b. Synchronized to a common time reference (Multiboard synchronization).

Clocking multiple converters from a single source prevents the *sampling drift* that occurs when converters are clocked from different sources. *Synchronizing* the converters on multiple boards causes the converters to initiate conversions simultaneously, and can be used to eliminate *sampling skew* between channels.

2.4.1 Interboard Connections

Figure 2.4.1 illustrates how multiple PMC66-24DSI16WRC boards can be daisy-chained together in an initiator-target sequence to provide common clocking between boards. The CLK OUT HI/LO lines from an initiator are connected to the CLK INP HI/LO lines on a target board, and the SYNC output and input pairs are connected similarly. Each target board can serve as an initiator for another target board, and multiple boards can be daisy-chained together for synchronous operation.

NOTE: The external sync input should be driven LOW if external clocking is implemented.

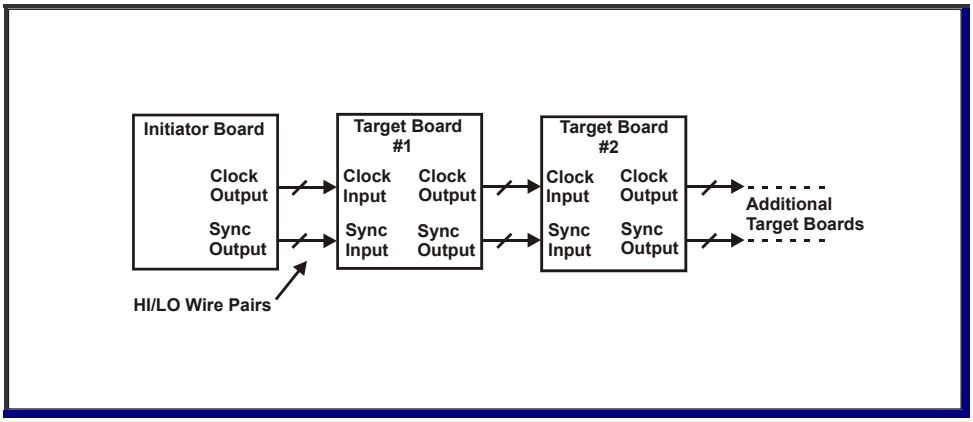

Figure 2.4.1. Multiboard Clock/Sync Connections

By using an external clock and sync distribution module, multiple boards can be interconnected in a 'star' configuration to eliminate the clock and sync propagation delay introduced by each board in a daisy chain configuration.

The clock output signal is generated internally on an initiator board, or is a duplicate of the clock input signal on a target board. Similarly, the sync output is the software-generated sync signal on an initiator board, or a duplicate of the sync input signal on a target board.

Note: External clock and sync inputs can be provided from external sources other than an initiator board, and can be software-configured for either single-ended TTL or differential LVDS logic levels. As a general rule, LVDS levels should be used in applications requiring I/O cable lengths that exceed 20-30 centimeters (10 inches).

In the TTL configuration, clock and sync inputs and outputs are connected through the "HI" I/O pins. LO inputs must be left open or disconnected, and the LO outputs are inactive. TTL signals are referenced to DIGITAL RTN.

Because each board provides active clock and sync outputs for the next board in the chain, the number of boards in the chain is limited only if the propagation delay of approximately 10 nanoseconds introduced by each board becomes significant through multiple boards. For LVDS clock and sync I/O configurations, cable-length between boards should not exceed one meter for general-purpose ribbon cable, while high-quality 100-Ohm cable can extend the length to 10 meters or more.

Application software controls the designation of each board as an initiator or a target. For additional synchronization options, refer to Section 3.12.

NOTE: The EXT SYNC INP signal can also be software-configured to initiate a triggered acquisition burst.

2.4.2 Multiboard Synchronization

Boards that are interconnected for multiboard synchronization initiate internal *synchronization sequences* each time a sync pulse is generated by the initiator board. The Sync I/O can also be used to reset (clear) the data buffers on target boards.

2.5 Maintenance

This product requires no scheduled hardware maintenance other than periodic reference verification. The optimum adjustment interval will vary, depending upon the specific application, but in most instances an interval of one year is recommended. In the event of a suspected malfunction, all associated system parameters, such as I/O cabling, power voltages, and control bus integrity should be evaluated before a board is returned to the factory for problem analysis and repair.

2.6 Reference Verification and Adjustment

All input and output channels are software-calibrated to an internal voltage reference by an embedded autocalibration software utility. This procedure describes the adjustment of the internal reference.

2.6.1 Equipment Required

Table 2.6.1 lists the equipment requirements for calibrating the PMC-24DSI16WRC. Alternative equivalent equipment may be used.

Table 2.6.1. Reference Adjustment Equipment

EQUIPMENT DESCRIPTION	MANUFACTURER	MODEL
Digital Multimeter (DMM), 5-1/2 digit, 0.005% accuracy for DC voltage measurements at +10 Volts.	Hewlett Packard	34401A
Host system with PMC site	---	---
DMM test leads suitable for connecting to 2mm header pins.	---	---

2.6.2 Adjustment Procedure

The following procedure describes the single adjustment that is necessary to ensure conformance to the product specification. Adjustment of the internal reference (Vtest) is performed with an internal trimmer that is accessible at one edge of the module, as shown in Figure 2.6.1. This procedure assumes that the board is installed in an operating system.

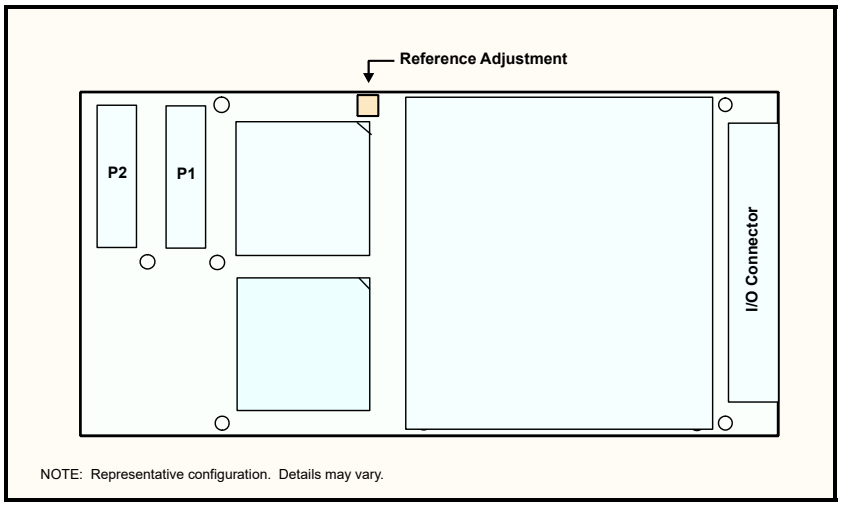

Figure 2.6.1: Reference Adjustment Location

1. Connect the digital multimeter between VTEST (+) Pin-3, and REF RTN (-) Pin-4 in the J4 test connector adjacent to the reference adjustment trimmer.
2. If power has been removed from the board, apply power now. Wait at least 10 minutes after power is applied before proceeding..
3. Select the ±10V input voltage range.
4. Verify that the digital multimeter indication is +9.9000 VDC ±0.0008 VDC. If the indication is not within this range, adjust the INTERNAL REFERENCE trimmer accordingly.
5. Verification and adjustment is completed. Remove all test connections.

SECTION 3.0

CONTROL SOFTWARE

3.1 Introduction

The PMC66-24DSI16WRC board is compatible with the PCI Local Bus specification, and is controlled through a PLX™ PCI-9056 PCI adapter that supports both 33MHz and 66MHz bus speeds as well as universal signaling. Configuration-space registers are initialized internally to support the location of the board on any 32-longword boundary in memory space.

After initialization, communication between the PCI bus and the board takes place through the control and data registers shown in Table 3.1. All data transfers are long-word D32. The input data buffer supports both block-mode and demand-mode DMA transfers, as well as single-reads. To ensure compatibility of applications with subsequent product upgrades, reserved bits should be written as LOW.

Table 3.1. Control and Data Registers

Local Addr [1]	Designation	Access Mode [2]	Default	Primary Function	Ref
00	**Board Control (BCR)**	R/W	0000 383Ch	Board Control Register (BCR)	3.2
04	**Rate Control-A**	R/W	0003 2040h	PLL reference oscillator control integer.	3.6.2
08	**Digital I/O Port**	R/W	0000 000Xh	Bidirectional digital I/O port control	3.15
0C	**Clock-Source Assignments**	R/W	0000 0000h	ADC Clock source; Group disables.	3.6.1.2
10	**Rate Divisor**	R/W	0000 0005h	Sample rate divisor.	3.6.1.3
14	(Reserved)	R/W	0000 0000h	---	---
18	(Reserved)	RO	0000 0000h	---	---
1C	**Burst Block Size**	R/W	0000 0001h	Specifies the number of sample sets to be acquired in a triggered burst	3.14
20	**Buffer Control**	R/W	0003 FFFEh	Input buffer control and status	3.5.3
24	**Board Configuration**	RO	00XX XXXXh	Installed firmware and hardware options	3.10
28	**Buffer Size**	RO	000X XXXXh	Number of ADC values in the input buffer.	3.5.4
2C	Autocal Values [3]	R/W	---	---	---
30	**Input Data Buffer**	RO (DMA)	XXXX XXXXh	Input Data Buffer; Data and channel tag	3.5
34	**Auxiliary Sync I/O Control**	R/W	0000 0000h	Auxiliary external Clock and Sync control.	3.12
38	**Master Clock Adjust**	R/W	0000 8000h	Master clock frequency adjustment.	3.13
3C	**Burst Trigger Timer**	R/W	0000 9C40h	Internal trigger timer rate divisor	3.14
40-7C	(Reserved)	---	---	---	---

[1] Offsets from the PCI base address for local addressing.

[2] R/W = Read/Write; RO = Read-Only.

[3] Maintenance register; Shown for reference only

3.2 Board Control Register

The Board Control Register (BCR) controls primary board functions, including analog input mode and input range selections, and supports up to 32 control bits and status flags (Table 3.2). Control and monitoring functions of the BCR are described in detail throughout the remainder of this section.

Table 3.2. Board Control Register

Offset: 0000h **Default: 0000 383Ch**

Data Bit	Designation	Mode	Def	Function	Ref
D00	AIM0	R/W	0h	Analog input mode. Selects system inputs or selftest mode. Defaults to system inputs.	3.4
D01	AIM1				
D02	RANGE0	R/W	3h	Analog input range selection. Defaults to ±10V range.	3.4.2
D03	RANGE1				
D04	OFFSET BINARY	R/W	1	Selects offset binary or two's complement input data format. Defaults HIGH to offset binary.	3.5.2.2
D05	INITIATOR OUTPUT	R/W	1	Selects INITIATOR or TARGET mode for external clock and sync output signals. Defaults HIGH to Initiator mode.	3.6.5
D06	SOFTWARE SYNC [1]	R/W	0	Initiates a local ADC sync operation when asserted. Also generates an external sync output if INITIATOR mode is selected. Clears automatically.	3.5.3.2, 3.6.4
D07	AUTOCAL [1]	R/W	0	Initiates an autocalibration operation when asserted. Clears automatically upon autocal completion.	3.7
D08	INTERRUPT A0	R/W	0h	Interrupt event selection. Default is zero.	3.8
D09	INTERRUPT A1	R/W			
D10	INTERRUPT A2	R/W			
D11	INTERRUPT REQUEST FLAG	R/W	1	Set HIGH when the board requests an interrupt. Clears the request when cleared LOW by the bus.	
D12	AUTOCAL PASS	RO	1	Set HIGH at reset or autocal initialization. Cleared LOW if autocalibration terminates unsuccessfully.	3.7
D13	CHANNELS READY	RO	1	LOW during any change in channel parameters. Asserted HIGH when inputs are ready to acquire data.	3.4.3
D14	BUFFER THRESHOLD FLAG	RO	0	Asserted HIGH when buffer contents exceed the assigned threshold.	3.5.3.1
D15	INITIALIZE [1]	R/W	0	Initializes the board when asserted. Sets all defaults.	3.3.2
D16	ENABLE TRIGGER TIMER	R/W	0	Enables the internal burst trigger timer.	3.14
D17	CLEAR BUFFER ON SYNC	R/W	0	Changes the context of the SOFTWARE SYNC to CLEAR BUFFER.	3.5.3.2
D18	RATE GEN EXT CLOCK OUT (Initiator Mode only)	R/W	0	When HIGH: Selects the internal rate generator as the external clock output source. When LOW: Selects the Group-00 sample clock. (If Group-00 external clocking is selected, the output is driven by the internal rate generator and the Group-00 divisor).	3.6.5.1
D19	HIGH SPEED ADC MODE	R/W	0	Selects the ADC High-Speed mode when HIGH, or the High-Resolution Mode when LOW.	3.6.1.3
D20	TTL EXTERNAL SYNC I/O	R/W	0	Selects TTL external sync I/O configuration.	3.6.1.2
D21	ENABLE INPUT BURST	R/W	0	Selects triggered-burst acquisition when HIGH.	3.14
D22	S/W BURST TRIGGER	R/W	0	Initiates a triggered burst when asserted. Forced HIGH during any triggered burst.	
D23	ENABLE EXT SYNC INPUT	R/W	0	The EXT SYNC INP external input is accepted, independent of the clocking mode.	
D24-31	(Reserved)	RW	0h	---	---

[1] Clears automatically.

3.3 Configuration and Initialization

3.3.1 Configuration

Board configuration is initiated by a PCI bus RESET, which should be required only once after the initial application of power. During configuration, initial values for both the PCI configuration registers and the internal control logic are extracted from internal nonvolatile read-only memory. While the PCI configuration registers are being loaded, the response to PCI target accesses is RETRY's. Configuration operations are executed in the sequence shown in Table 3.3.1.

Table 3.3.1. Configuration Operations

Operation	Maximum Duration
PCI configuration registers are loaded from internal EEPROM	3 ms
Internal control logic is configured from internal ROM	300 ms
Internal control logic is initialized	3 ms
A/D converters and clocks are initialized	20 ms

Configuration terminates with the PCI interrupts disabled.

3.3.2 Initialization

Internal control logic can be initialized without invoking configuration by setting the INITIALIZE control bit in the BCR. This action causes the internal logic to be initialized, but does not affect the PCI configuration registers and does not reconfigure the internal control logic. Initialization has a maximum duration of 20 milliseconds, and produces the following conditions:

- The Initiator mode is selected, (3.6.5.1),
- The width of the buffer data field is adjusted to 16 bits (3.5.2),
- The input buffer is disabled; Acquisition is suspended (3.5.3.2),
- The internal rate generator is the ADC clock source for all input channels (3.6.1),
- Internal rate generator frequency is 51.200 MHz (3.6.2),
- Rate divisor is preset to 5, and High-Resolution sampling is selected (3.2, 3.6.1.3),
- Sample rate is 10.0 KSPS (3.6.1),
- The internal burst-trigger timer is adjusted to 1.00 kHz (3.14.2),
- The analog input buffer is reset to empty; buffer threshold equals 0003 FFFEh (3.5.3),
- Analog inputs are configured for ±10 Volt operation (3.4.2),
- All control registers are initialized; all defaults are invoked (3.3.2),
- The local interrupt request is asserted as an initialization-completed event (3.8).

Upon completion of initialization, the INITIALIZE control bit is cleared automatically.

3.4 Analog Input Configuration

Configuration of the analog input networks is controlled by the BCR control bits designated as AIM[1..0], the effects of which are summarized in Table 3.4. The analog input selection arranges all input channels in differential configuration during normal operation, or invokes one of two selftest modes.

Table 3.4. Analog Input Function Selection

AIM[..0]	Function or Mode
0	Differential analog input mode.
1	(Reserved).
2	ZERO test. Internal ground reference is connected to all analog input channels.
3	+VREF test. Internal voltage reference is connected to all analog input channels.

3.4.1 Selftest Modes

Two selftest modes provide the ability to verify the accuracy of any or all input channels by replacing the system input connections with either a precision internal reference voltage (+VREF) or a zero reference (ZERO). ***The +VREF test applies a precision test voltage of +9.900V to all input channels only on the ±10V input range, and Zero (0.0000V) on all other ranges.*** The ZERO test applies a value of 0.0000 Volts on all ranges. The accuracy of selftest measurements should correspond to the product accuracy specification.

NOTE: For maximum test accuracy, the internal reference voltage must be allowed to settle completely when the test mode is changed. After selecting either of these test modes, insert a minimum settling delay of 100 milliseconds before acquiring test values:

3.4.2 Input Range Selection

Any one of four input voltage ranges can be selected for all input channels. RANGE[1..0] control bits in the BCR select the input range, as shown in Table 3.4.3. The specific set of available input ranges is identified in Table 3.10.1.

Table 3.4.3. Analog Input Range Selection

RANGE[1..0]	Standard Input Range	Optional Alternate Input Range
0	±10mV	±1.25V
1	±100mV	±2.5V
2	±1.0V	±5V
3	±10V	±10V

NOTE: Overdriving the inputs by more than 20-percent beyond the selected input range can cause increased input leakage current. Overdriving beyond 50-percent will increase internal power supply loading and possibly cause corrupted data.

3.4.3 Settling Delays and the Channels-Ready Flag

When a critical parameter such as input mode or sample rate is changed, a settling transition occurs during which input measurements are unpredictable. A settling delay is inserted automatically when any or all of these parameters are changed, and the CHANNELS READY status flag in the BCR goes LOW during the delay. A LOW-to-HIGH transition of this flag is selectable as an interrupt request "channels ready" event (Section 3.8.1). The CHANNELS READY flag goes low during the following operations for the approximate intervals indicated:

20 ms:	Board initialization (3.3),
10 us-20 ms:	Buffer reset; Sample-rate dependent (3.5.3.2).
20 ms:	Modified sample rate parameter ; i.e.: Nrate, Ndiv, Clock source.
2-700 ms:	ADC synchronization (3.6.5.2), or Speed-mode change (3.6.1.3).

3.5 Input Data Buffer

3.5.1 General Characteristics

Analog input samples accumulate in the analog input data FIFO buffer, which has a capacity of 256K (262,144) data values. Data accumulates in the buffer until extracted by the PCI bus from a single register location, indicated as 'Input Data Buffer' in Table 3.1. Reading an empty buffer returns an indeterminate value. For each input sample set, data is arranged with Channel-00 appearing first, and the highest-numbered active channel appearing last.

3.5.2 Data Organization

Each value in the data buffer consists of a 4-bit channel tag field, a zero-pad field, and a data field, as shown in Table 3.5.2. The width of the right-justified data field is adjustable from 16 bits to 24 bits by the DATA WIDTH control field in the buffer control register (Table 3.5.3), and the width of the zero-pad field is adjusted accordingly. The zero-pad field becomes a sign-extension field if two's complement data coding is selected.

Table 3.5.2. Input Data Buffer Organization

Offset: 0000 0030h **Default: XXXX XXXXh**

Selected Data Width	Reserved (Zero)	Channel Tag	Zero-Pad	Channel Data Value
16 Bits	D[31..28]	D[27..24]	D[23..16]	D[15..0]
18 Bits	D[31..28]	D[27..24]	D[23..18]	D[17..0]
20 Bits	D[31..28]	D[27..24]	D[23..20]	D[19..0]
24 Bits	D[31..28]	D[27..24]	---	D[23..0]

3.5.2.1 Channel Tags

A channel tag that identifies each input channel is attached to each data value in the buffer. This tag value equals the associated input channel number. The channel tag can be eliminated by setting the DISABLE CHANNEL TAG control bit in the Buffer Control Register.

.

3.5.2.2 Input Data Format

Input data values can be represented either in offset binary format by asserting the OFFSET BINARY control bit HIGH (default state) in the BCR, or in two's complement format by clearing the control bit LOW. Both coding conventions are illustrated for 16-Bit data in Table 3.5.2.2.

Table 3.5.2.2. Analog Input Data Coding; 16-Bit Data Field

	DIGITAL VALUE (Hex)	
ANALOG INPUT LEVEL	**OFFSET BINARY**	**TWO'S COMPLEMENT**
Positive Full Scale minus 1 LSB	FFFFh	7FFFh
Zero plus 1 LSB	8001h	0001h
Zero	8000h	0000h
Zero minus 1 LSB	7FFFh	FFFFh
Negative Full Scale plus 1 LSB	0001h	8001h
Negative Full Scale	0000h	8000h

Positive Full Scale is a positive level that equals the selected input voltage range for the board (e.g.: +10.000 Volts for the ±10V range). *Negative Full Scale* is the negative equivalent of positive full-scale. *Full-scale Range* (FSR) is the total input voltage range. For 16-Bit data, one LSB equals the full-scale range divided by 65,536. (e.g.: 305.175 microvolts for the ±10V range).

3.5.3 Buffer Control Register

The buffer control register (Table 3.5.3) contains the threshold value for the buffer threshold flag in the BCR, and also provides control bits for clearing the buffer and for disabling the buffer input.

Table 3.5.3. Buffer Control Register

Offset: 0000 0020h **Default: 0003 FFFEh**

Bit Field	Mode	Designation	Def	Function
D[18..00]	R/W	BUFFER THRESHOLD	0003 FFFEh	Buffer Flag Threshold
D[19]	R/W	ENABLE BUFFER INPUT	0	Enables ADC inputs to the buffer.
D[20]	R/W	CLEAR BUFFER [1]	0	Clears (empties) the buffer. Asserted HIGH while the buffer is cleared, either locally or externally.
D[22..21]	R/W	DATA WIDTH	0	Controls the width of the buffer data field: 0 => 16 bits 1 => 18 bits 2 => 20 bits 3 => 24 bits.
D[23]	R/W	DISABLE CHANNEL TAG	0	Replaces the channel tag with a zero-field.
D[24]	R/W	BUFFER OVERFLOW [2]	0	Reports buffer overflow (Write on full)
D[25]	R/W	BUFFER UNDERFLOW [2]	0	Reports buffer underflow (Read on empty)
D[31..26]	RO	(Reserved)	0h	---

[1] Clears automatically. [2] Cleared by writing LOW, or by Initialization.

NOTE: Since delta-sigma ADC's perform conversions continuously, the initiation and termination of acquisition sequences is controlled by the buffer's 'Clear' and 'Enable' controls.

3.5.3.1 Status Flag and Threshold

The amount of data contained in the input buffer can be used to control the BCR status bit BUFFER THRESHOLD FLAG, which can be selected as an interrupt request event. The interrupt request event can be selected to occur on either the rising or falling edge of the flag (Table 3.8.1).

The threshold flag is asserted HIGH when the number of samples in the buffer ***exceeds*** the BUFFER THRESHOLD value in the buffer control register. A buffer-empty event is produced when the threshold value is adjusted to equal 0000 0000h and the threshold flag undergoes a HIGH-to-LOW transition.

3.5.3.2 Buffer Clearing and Enabling/Disabling

Asserting the CLEAR BUFFER control bit in the buffer control register resets (empties) the buffer, and holds the buffer in reset until the internal data pipeline clears. This delay can vary from approximately 10 microseconds to 20 milliseconds, depending upon the selected sample rate (See also 3.4.3). This bit clears automatically, but is held HIGH while the buffer is being cleared.

Asserting the ENABLE BUFFER INPUT control bit enables inputs to the buffer from the ADC input channels, and initiates the accumulation of input data. Clearing this control bit disables the buffer and suspends sample acquisition. Input data already present in the buffer when this bit is deasserted remains in the buffer.

Buffer enabling and disabling operations both are synchronous with the input data stream. That is, regardless of when the enabling control bit is set or cleared, actual enabling of the buffer always occurs immediately prior to a complete sample set arriving, and disabling always occurs immediately after the last active channel in a sample set is loaded into the buffer.

NOTE: Global Buffer Clear:

The buffer also can be cleared by writing a "one" to the SOFTWARE SYNC control bit in the BCR when the CLEAR BUFFER ON SYNC control bit is HIGH. For multiple synchronized boards:

1. On all boards: Set the CLEAR BUFFER ON SYNC bit,
2. On the Initiator: Set SOFTWARE SYNC;
   Wait for Channels Ready LOW-to-HIGH on the initiator.
   (All ADC's and buffers are now scan-synchronized).
3. On all boards: Clear the CLEAR BUFFER ON SYNC bit.

3.5.4 Buffer Size Register

This read-only register listed in Table 3.1 contains the number of analog input values currently stored in the input data buffer, from zero to 262144 (40000h).

3.5.5 Buffer Underflow and Overflow Flags

BUFFER OVERFLOW and BUFFER UNDERFLOW status bits in the buffer control register report overflow (write on full) or underflow (read on empty) events. Once set, these status bits remain HIGH until cleared either by writing LOW directly, or by Initialization.

3.6 Input Sampling Control

The local controller establishes the following input sampling parameters:

a. Sample rate,
b. Phase, or skew,
c. Channel synchronization.

The effective input bandwidth is determined by the sample rate, while phase and synchronization control the relative timing of sampling between multiple channels. Phase and synchronization are considerations in applications that require consistent relative timing of sampling among multiple channels or multiple boards.

Clocking multiple converters from a single sample rate clock prevents the *sampling drift* that occurs when converters are clocked from different sources. *Synchronization* causes the converters in all channels to initiate conversions simultaneously, and can be used to eliminate *sampling skew* between channels.

NOTE: It is critically important that the inputs always be synchronized (3.6.4) after changing any parameter that affects the sample rate. Failure to do so can cause the general corruption of input data. Any change to the Rate-A control, Clock Source Assignments, Rate Divisor or the High Speed/Resolution mode will initiate an automatic synchronization sequence. However any sample-rate change, especially from an external source, should still be followed by synchronization through the BCR.

3.6.1 Sample Rate Control

3.6.1.1 Sample Clock Organization

Sample rates are derived either from an adjustable internal rate generator, or from a single external hardware clock, as shown in Figure 3.6.1.1. The input channels are divided into two equal groups (Table 3.6.1.1), and all active input channels operate from the same clocking source. Group-1 can be independently designated as either active (enabled) or inactive (disabled). The sample rate for both channel groups is controlled by the following operations:

a. Assignment of both groups to the internal rate generator or to an external clock,
b. Rate generator frequency selection, if the internal rate source is selected,
c. Rate divisor selection, unless the Direct External Sample Clock is selected.

The number of channels per group is reduced to four channels for 8-channel boards, or to two channels for 4-Channel boards. This scheme ensures that the board is partitioned into two equal channel groups, regardless of the number of channels present on a board.

3.6.1.2 Clock Source Assignment

A 4-bit code CLOCK SOURCE in the Clock Source Assignments register (Table 3.6.1.2-1) selects either the internal rate generator or the external sample rate clock as sample rate source. Group selection codes are arranged in the register as shown in the table, and use the assignment codes listed in Table 3.6.1.2-2. ***The Group-0 assignment selects the sample rate source for both groups***, while the Group-1 assignment simply enables or disables the group. A disabled group does not provide data to the input data buffer.

NOTE: External I/O signals EXT CLK INP/OUT and EXT SYNC INP/OUT are configured as LVDS HI/LO pairs if the TTL EXTERNAL SYNC I/O control bit is LOW in the BCR, or for TTL signals on the HI lines if the bit is HIGH.

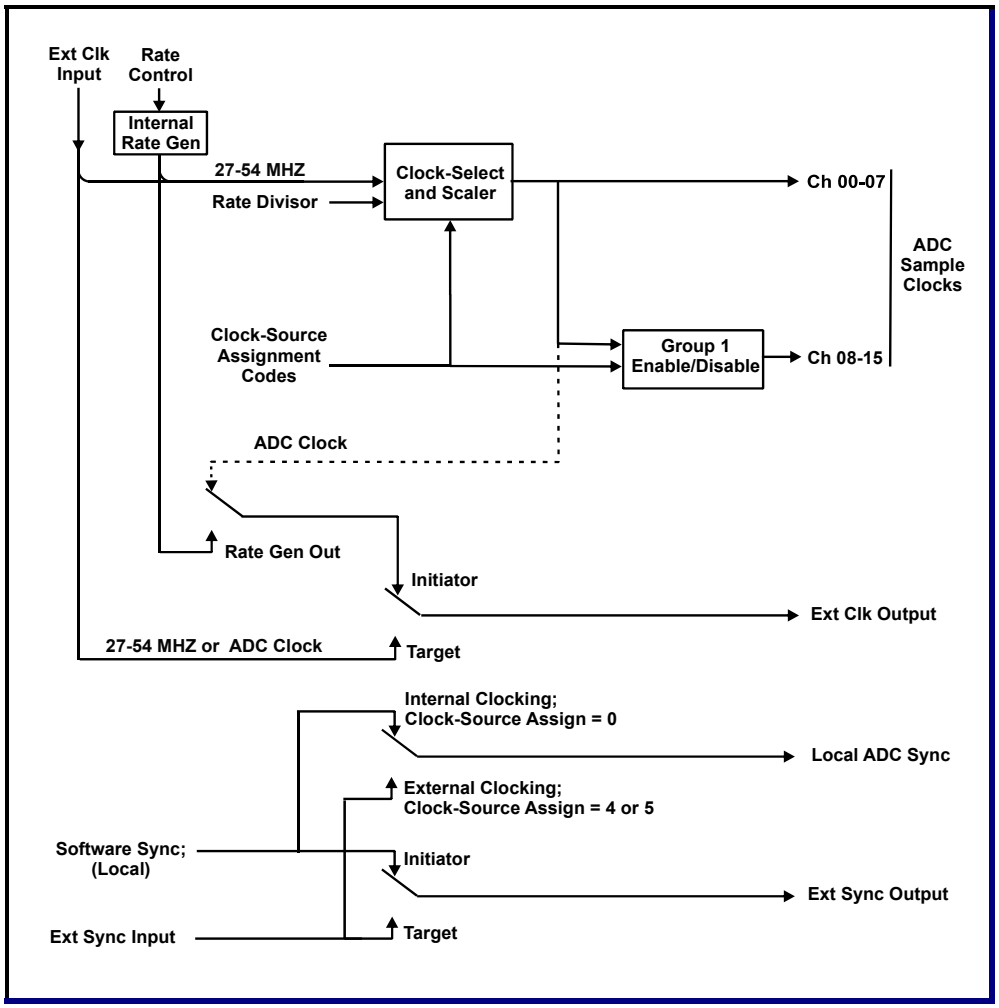

Figure 3.6.1.1. ADC Clock and Sync Organization, 16 Channels

Table 3.6.1.1. Channel Groups

CHANNEL GROUP	16-CHAN BOARD	8-CHAN BOARD	4-CHAN BOARD
0	Channels 00-07	00-03	00, 01
1	Channels 08-15	04-07	02, 03

Table 3.6.1.2-1. Clock-Source Assignments Register

Offset: 0000 000Ch **Default: 0000 0000h**

BIT FIELD	DESIGNATION	CHANNEL GROUP
D[03..00]	GROUP 0 CLOCK SOURCE	0
D[07..04]	GROUP 1 CLOCK SOURCE	1
D[31..08]	(Reserved)	---

Table 3.6.1.2-2. Clock-Source Assignment Codes

ASSIGNMENT CODE	GROUP 0 ASSIGNMENT	GROUP 1 ASSIGNMENT
0	Internal Rate Generator *	No effect. (Same as Group-0)
1-3	(Reserved)	
4	External Sample Clock (as rate generator input)	
5	Direct External Sample Clock (routed directly to ADC)	
6	**Disabled**	**Disabled**
7-15	(Reserved)	(Reserved)

* Applies to both channel groups. Disabling Group-0 disables both groups.

3.6.1.3 Sample Clock Generation

The ADC's operate in one of two sampling modes, the High-Resolution mode or the High-Speed mode, selected by the HIGH SPEED ADC MODE control bit in the BCR. The sample rate range is 0.4-105KSPS in the High-speed mode, or 0.2-52.5KSPS in the High-Resolution mode. The signal-to-noise ratio (SNR) is approximately 3dB higher in the High-Resolution mode, when compared with High-Speed mode performance.

A rate divisor integer **Ndiv** (Table 3.6.1.3-1) controls a *rate divisor* for the rate generator or external clock input.

Table 3.6.1.3-1. Rate Divisor Register

Offset: 0000 0010h **Default: 0000 0005h**

BIT FIELD:	DESIGNATION	FUNCTION
D[08..00]	RATE DIVISOR (**Ndiv)**	Prescales the rate generator input frequency.
D[31..9]	(Reserved)	---

NOTE: Changing the state of the HIGH SPEED ADC MODE control bit forces a buffer reset and deasserts the CHANNELS READY status flag (3.4.3) for approximately 140 ADC sample periods.

The ADC sample rate **Fsamp** is determined by a rate generator frequency **Fgen** and rate divisor **Ndiv** as: (all values shown in decimal)

$$\textbf{Fsamp (High-Speed)} = \frac{\textbf{Fgen}}{\textbf{Ndiv} * \textbf{512}}, \qquad \textbf{(3-1a)}$$

$$\textbf{Fsamp (High-Resolution)} = \frac{\textbf{Fgen}}{\textbf{Ndiv} * \textbf{1024}}, \qquad \textbf{(3-1b)}$$

where **Fsamp** and **Fgen** are in kilohertz, and **Ndiv** is an integer. **Fgen** has a nominal range of 27-54 MHz, and **Ndiv** can have any integer value from 1-300.

Table 3.6.1.3-2. Sample-Rate Control Parameters

PARAMETER	NOTATION	RANGE
VCO Frequency Range	**Fgen**	27 - 54 MHz nominal range
Rate Divisor	**Ndiv**	1-300
Sample Rate Range	**High-Speed Mode**	0.4 - 105 KSPS
	High-Resolution Mode	0.2 - 52.5 KSPS

3.6.2 Rate Generator Control

The internal rate generator is a PLL-controlled oscillator that is phase-locked to a stable reference frequency. The frequency of the generator is controlled by the Rate Control-A register listed in Table 3.1, and shown in Table 3.6.2-1.

Fgen can be obtained either externally through the system I/O connector (3.6.5) or from the internal phase-locked loop (PLL) oscillator, and has a nominal frequency range of 27-54 MHz. The frequency **Fgen** of the internal oscillator is related to a reference frequency **Fref** by integers **Nref** and **Nvco** as:

$$\textbf{Fgen} = \textbf{Fref} * \frac{\textbf{Nvco}}{\textbf{Nref}}, \qquad \textbf{(3-2)}$$

where **Nvco** and **Nref** each has a valid range from 25 to 300, and **Fref** is the frequency of the reference oscillator, which has a standard frequency of **40.000MHz**. Table 3.6.2-2 summarizes the rate generator control parameters. *(**Fref** is referred to in Paragraph 3.13 as **FcIk**, and is adjustable as described in that paragraph).*

NOTE: The nominal range of Fgen (27-54 MHz) and an Fref value of 40.000MHz imply a valid range of 0.67-1.35 for the ratio Nvco/Nref.

Table 3.6.2-1. Rate Generator Control Register

Offset: 0004h **Default: 0003 2040h**

BIT FIELD	MODE	DESIGNATION	FUNCTION *
D[11..00]	R/W	VCO FACTOR **(Nvco)**	PLL VCO factor; 25-300.
D[23..12]	R/W	REF FACTOR **(Nref)**	PLL Reference factor; 25-300.
D[31..24]	R/W	(Reserved)	---

* For maximum phase stability, select the lowest possible values for Nvco and Nref.

NOTE: Nvco and Nref each has a maximum range from 25 to 300. For optimum performance (lowest noise), select the *lowest* possible values for Nvco and Nref.

By combining Equation 3-2 with 3-1a and 3.1b:

$$\textbf{Fsamp (High-Speed)} = \frac{\textbf{Fref}}{\textbf{Ndiv * 512}} * \frac{\textbf{Nvco}}{\textbf{Nref}} \quad , \qquad \textbf{(3-3a)}$$

$$\textbf{Fsamp (High-Resolution)} = \frac{\textbf{Fref}}{\textbf{Ndiv * 1024}} * \frac{\textbf{Nvco}}{\textbf{Nref}} \quad , \qquad \textbf{(3-3b)}$$

where **Fsamp** and **Fref** are in kilohertz, and **Ndiv, Nvco** and **Nref** are integers. Table 3.6.2-2 summarizes the acceptable ranges for these control parameters.

Table 3.6.2-2. Rate-Generator Control Parameters

PARAMETER	NOTATION	NOMINAL RANGE
VCO Frequency Range	**Fgen**	27 - 54 MHz
Reference Frequency	**Fref**	Standard value = 40,000 kHz
VCO Factor	**Nvco**	25-300
Reference Factor	**Nref**	25-300
Nvco/Nref Factor Ratio	**Nvco/Nref**	0.67 - 1.35

To establish a specific sample rate Fsamp, determine the in-range values of **Ndiv**, **Nvco** and **Nref** that produce the closest available rate. For the best SNR performance, use the High-Resolution sampling mode if possible.

Table 3.6.2-3. Sample Rate Examples

Sample Rate (KSPS)	Nvco	Nref	Fgen (Mhz)	Ndiv	MODE (BCR)
0.200	128	125	40.9600	200	High-Resolution
1.000	64	50	51.2000	50	
10.000	64	50	51.2000	5	
20.000	128	125	40.9600	2	
100.000	64	50	51.2000	1	High-Speed
105.000	168	125	53.7600	1	

Fref = 40.000MHz. All values shown in decimal format.

3.6.3 Direct External Clocking

If the rate assignment selection (Table 3.6.1.2-2) is "Direct External Sample Clock," the signal at the external clock input is routed directly to the ADC's without modification. This configuration eliminates the effect of the **Ndiv**, **Nvco** and **Nref** control variables, and gives the external clock source direct control of the ADC's. Although the variables **Ndiv**, **Nvco** and **Nref** have no effect in this configuration, the sampling mode of the ADC's still must be controlled by the HIGH SPEED ADC MODE control bit in the BCR.

NOTE: The ratio of Fext (External Clock) to Fsamp (Sample Rate) is the Oversamping Factor (OSF) for the ADC's, and equals 256 in the High-Speed mode, or 512 in the High-Resolution mode.

3.6.4 Channel Synchronization

Due to the oversampling nature of delta-sigma conversion, each conversion represents a sampling interval consisting of multiple clock cycles, and simply operating all converters from a common clock does not ensure simultaneous, or skew-free, sampling. To ensure simultaneous sampling, the converters must be synchronized to perform conversions simultaneously relative to a common point in time. Thereafter, the converters will continue to sample simultaneously while operating from a common clock.

Synchronization is invoked by setting the SOFTWARE SYNC control bit HIGH in the BCR. Completion of the synchronization sequence is indicated by the CHANNELS READY flag in the BCR undergoing a Low-to-High transition (Paragraph 3.4.3). The CHANNELS READY transition can be selected as a condition for an interrupt request event.

NOTE: It is critically important that the inputs always be synchronized after changing any parameter that affects the sample rate. Failure to do so can cause the general corruption of input data. Any change to the Rate-A control, Clock Source Assignments, Rate Divisor or the High Speed/Resolution mode will initiate an automatic synchronization sequence. However any sample-rate change, especially from an external source, should still be followed by synchronization through the BCR.

3.6.5 Multiboard Operation

Multiple PMC66-24DSI16WRC boards can be connected together to share a common sampling clock and synchronization command. One of the boards is designated as the *initiator*, and the remaining boards are designated as *targets*. A board is designated as an initiator by setting the INITIATOR control bit HIGH in the BCR, or as a target when the control bit is LOW.

The INITIATOR control bit controls only the source of the external clock and sync outputs, and has no other effect.

External clock and sync inputs can be provided from LVDS or TTL sources other than an initiator board.

3.6.5.1 External Sample Clock

Target boards receive an external clock from the external clock input connection, and duplicate the input clock at the external clock output connection (Figure 3.6.1.1). The external clock input is designated as the clocking source by writing either the "External Sample Clock" or "Direct External Sample Clock" assignment code to the target boards' Clock-Source Assignments register (Table 3.6.1.2-2). For calculation of target board sample rates, the external sample clock corresponds to the rate generator frequency **Fgen** described in Section 3.6.1 if "External Sample Clock" is selected, or provides the ADC sample clock directly if "Direct External Sample Clock" is selected.

NOTE: The external sync input should be driven LOW if external clocking is implemented.

An ***initiator*** provides an external clock output from either of two sources. If the RATE GEN EXT CLOCK OUT control bit in the BCR is LOW (default), the external clock output frequency equals twice the Group 00 ADC sample clock frequency, and is the internal rate generator output divided by the rate divisor. If the control bit is HIGH, the internal rate generator's unmodified output provides the external clock.

Multiple boards can all be configured as targets and operated in a "star" configuration to operate from a single rate generator. To avoid overloading the LVDS source driver, an LVDS distribution module usually is required in this configuration.

3.6.5.2 External Sync

Boards that are hardware-configured for multiboard synchronization initiate a *synchronization sequence* each time a sync pulse is generated by the initiator board. During synchronization, all ADC's are reset and initialized in a sequence that requires approximately 140 sample intervals for completion. The data buffers also are reset during the sequence, at the end of which, all channels on all boards are synchronized to within one sample clock interval, and all data buffers commence acquiring data simultaneously.

The "CHANNELS READY flag is deasserted on all boards during the synchronization sequence, and returns HIGH when all boards are synchronized and commence acquiring data.

NOTE: A "sample clock interval" is the period of the ADC sample clock (1/Fgen) while the "sample interval" is the interval between data samples (1/Fsamp) and is 256-512 times the sample clock interval (3.6.1).

The SOFTWARE SYNC control bit in the BCR can be used also to clear the buffers on the initiator and target boards simultaneously without executing a full synchronization sequence, by first setting the CLEAR BUFFER ON SYNC control bit HIGH in the BCR. This process requires 4-5 sample intervals for completion. ***If implemented, the CLEAR BUFFER-ON-SYNC control bit must be asserted on the initiator and all targets.***

NOTE: The external sync input signal should be driven LOW if external clocking is implemented. External clocking is disabled when this input is High.

For very low-frequency sample clocks, the synchronization interval can approach one second. Notice that In the absence of an ADC clock, the synchronization or buffer-clear interval will be indefinitely long.

Refer to Paragraph 3.14 if burst-triggering is to be implemented.

3.7 Autocalibration

Autocalibration is an embedded utility that calibrates all input channels to a single internal voltage reference. Offset and gain error corrections for each channel are determined and stored during autocalibration, and then are applied to each channel in real-time during data acquisition. The correction values are retained until either: (a) power is removed, (b) a PCI reset occurs, or (c) autocalibration is invoked again. Autocalibration is invoked by setting the AUTOCAL control bit HIGH in the BCR. Completion of autocalibration is indicated by the AUTOCAL flag clearing automatically to the LOW state. The end of autocalibration is selectable as an interrupt request event (3.8.1).

NOTE: Autocalibration calibrates all channels on all ranges in a single sequence.

An autocalibration sequence can have a duration from 1 to 35 seconds, depending upon the selected sample rate and the number of active channels. For 16 active channels, the ***approximate*** autocal duration is

$$\mathbf{T_{autocal}\ (seconds) = 1 + (6500/Fsamp),}$$

where Fsamp is the selected sample rate in samples-per-second. For example:

$T_{autocal}$ @ 10ksps = 1 + (6,500/10,000) ~= 1.7 Seconds.
$T_{autocal}$ @ 400sps = 1 + (6,500/400) ~= 17 Seconds.

Read or write access from the PCI bus during autocalibration could disrupt the calibration process, and should be avoided. Either a suitable delay or the "Autocal Completed" interrupt should be used to detect the end of autocalibration.

If a board is defective, the autocalibration process may be unable to successfully calibrate all input channels. If this situation occurs, the AUTOCAL PASS status flag in the BCR will be LOW when the autocal sequence is completed. A HIGH state for AUTOCAL PASS indicates that autocalibration was successful for all channels.

To ensure full conformance to the product specification, autocalibration should always be invoked after:

(a). Power has been applied to the board,

(b). A PCI reset event has occurred,

(c). The clock source or sampling rate has been altered.

Autocalibration can be invoked at any time, but should not occur while the system is experiencing a major environmental transition such as that which usually occurs directly after power is applied. For optimum performance, a warmup delay of 15 minutes is recommended.

3.8 Interrupt Control

In order for the board to generate a PCI interrupt on INTA#, *both* of the following conditions must occur:

a. The internal controller must generate a Local Interrupt Request
b. The *PCI interrupt* must be enabled.

If the internal controller generates a local interrupt request, a PCI bus interrupt will not occur unless the PCI interrupt has been enabled as described below in Paragraph 3.8.2.

3.8.1 Local Interrupt Request

The single local interrupt request line is controlled by the INTERRUPT A[2:0] and INTERRUPT REQUEST FLAG control bits in the BCR. The condition for the interrupt request is selected as shown in Table 3.8.1. When the selected condition occurs, a local interrupt request is generated and the INTERRUPT REQUEST FLAG bit is set in the BCR. The request remains asserted until the PCI bus clears the BCR request flag. A local interrupt request is generated automatically at the end of initialization.

Detection of an interrupt condition or event is *edge-sensitive*. An interrupt request is generated if, and only if, a specific interrupt condition undergoes a *transition* from 'false' (not-true) to 'true' while that condition is selected.

Table 3.8.1. Interrupt Event Selection

INTERRUPT A[2:0]	INTERRUPT EVENT CONDITION
0	Initialization completed. Default state.
1	Autocal completed
2	Channels Ready; LOW-to-HIGH transition
3	Data Buffer threshold flag, LOW-to-HIGH transition
4	Data Buffer threshold flag, HIGH-to-LOW transition
5	Triggered Burst Completed
6	(Reserved)
7	(Reserved)

3.8.2 Enabling the PCI Interrupt

A local interrupt request will not produce an interrupt on the PCI bus unless the PCI interrupt is enabled. The PCI interrupt is enabled by setting the *PCI Interrupt Enable* and *PCI Local Interrupt Enable* control bits HIGH in the runtime *Interrupt Control/Status Register* described in the PLX™ PCI-9056 reference manual..

3.9 DMA Operation

DMA transfers from the analog input buffer are supported with the board operating as a bus master. Set Bit 02 in the PCI Command register HIGH to select the bus mastering mode. Refer to the PCI-9056 reference manual for a description of DMA configuration registers.

3.9.1 Block Mode

Table 3.9.1 illustrates a *typical* PCI register configuration that would control a non-chaining, non-incrementing ***block-mode*** DMA transfer in DMA Channel 00, in which a PCI interrupt is generated when the transfer has been completed. For most applications, the DMA Command Status Register would be initialized to 0000 0001h, and then changed to 0000 0003h to initiate a transfer.

Table 3.9.1. Typical DMA Register Configuration; Block Mode

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial (constant) local address of buffer	0000 0030h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

* Determined by specific transfer requirements.

3.9.2 Demand Mode

Demand mode transfers are controlled in a manner similar to block mode transfers, with the addition of ***demand-mode*** operation selected in the DMA mode register (D[12] = HIGH). Demand mode operation also requires the ***slow terminate*** mode (D[15] = LOW), which is the default state for this control bit. Table 3.9.2 shows a *typical* PCI register configuration for DMA Channel 00 demand mode operation.

Table 3.9.2. Typical DMA Register Configuration; Demand Mode

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32)	0002 1943h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial (constant) local address of buffer	0000 0030h
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

* Determined by specific transfer requirements.

NOTE: The PCI-9056 adapter extracts data from the 32-Bit (Lword) local bus in 64-Bit (quad-word) increments. Consequently, *if the buffer runs empty or nearly empty*, the situation can arise in which the last one or two samples in an active channel group are retained until subsequent data is acquired. If this occurs, the next sample set flushes the retained data through the PCI-9056 adapter to the PCI bus, and no samples are lost.

3.10 Board Configuration Register

The read-only board configuration register (Table 3.10.1) contains the existing firmware revision, and a status field that indicates the availability of optional features.

Table 3.10.1. Board Configuration Register

Offset: 0000 0024h **Default: 0000 XXXXh**

BIT FIELD	DESCRIPTION
D00-D11	Firmware Revision
D12-D15	(Reserved status flags).
D16-D17	Number of input channels: 0 => 16 Channels 1 => 8 Channels 2 => 4 Channels 3 => (Reserved)
D18-D20	Image Filter Frequency: 0 => 150kHz 1 => No filter. 2-7 => (Reserved)
D21	Selectable Input Ranges: Low => ±10V, ±1V, ±100mV, ±10mV (Standard range set) High => ±10V, ±5V, ±2.5V, ±1.25V (Optional range set)
D22-D31	(Reserved)

3.11 Settling Time Considerations

An abrupt change in the analog configuration generally is followed by a 'settling' interval during which the analog networks are transitioning to a new state, and during which specified performance might be suspended. Abrupt changes include:

- A change in voltage range or sample rate,
- A major input step-change,
- Transitioning into or out of a selftest mode, or out of autocalibration,
- A system or local reset,
- Power application.

The settling time required to reestablish specified performance depends upon the type of disruption, and can vary from tens of milliseconds for a change in voltage-range, to as long as 10-15 minutes after the initial application of power. For *most* configuration changes other than the application of power, specified performance should resume after a settling interval of 20-100 milliseconds. Low-frequency filters will extend the settling interval by an amount that depends upon the filter characteristics. In general, the longest settling delay consistent with application requirements should be implemented.

3.12 Auxiliary External Clock and Sync I/O

Two auxiliary external connections provide an alternate method of synchronizing sample clocking to external events. These bidirectional TTL connections are available as AUX CLOCK and AUX SYNC (Table 2.2.2-2), and when active *as inputs*, replace the corresponding external EXT CLK I/O and EXT SYNC I/O inputs in the system I/O connector. The AUX I/O signals are accessible through a 6-Pin connector on the back (Side-2) of the board.

AUX clock and sync signals are designated independently through the Auxiliary Sync I/O Control register as inputs, outputs, or inactive, as indicated in Table 3.12.1. When an AUX signal is designated as an ***input***, the signal replaces the corresponding EXT CLK INP or EXT SYNC INP input from the system connector. The AUX I/O pins are pulled up internally to +3.3VDC through 33K.

In order for Aux inputs to be acknowledged, in addition to making the appropriate 'active' selections in Table 3.12.1, "External Sample Clock" must be selected with the Clock-Source Assignment code (Table 3.6.1.2-2).

The AUX *CLOCK* and AUX SYNC ***as active outputs*** duplicate the EXT CLK OUT and EXT SYNC OUT signals respectively in the system I/O connector.

Table 3.12.1. Auxiliary Sync I/O Control

Offset: 0000 0034h **Default: 0000 0000h**

Data Bit	Mode	Designation	Default	Description
D00-01	R/W	AUX CLOCK Control Mode	0	AUX CLOCK I/O Control Mode: 0 => Inactive 1 => Active Input 2, 3 => Active Output
D02-03	R/W	AUX SYNC Control Mode	0	AUX SYNC I/O Control Mode 0 => Inactive 1 => Active Input 2, 3 => Active Output
D04-31	RO	(Reserved)	0	Read-back as all-zero.

3.13 Master Clock Frequency Adjustment

The master clock oscillator frequency **Fclk** (Fref in Paragraph 3.6.2) can be adjusted approximately 50-80PPM to either side of its nominal value. The control field for this adjustment is the lower 16 bits (D00-15) of the MASTER CLOCK ADJUST register listed in Table 3.1. This field defaults to 8000h after initialization, and is adjustable from 0000h to FFFFh. Lower values produce lower frequencies, with 0000h producing a negative frequency deviation approximately 50-80PPM below nominal, and FFFFh producing a positive deviation 50-80PPM above nominal.

Writing to this register automatically initiates a loading sequence in which the new contents of the register are transferred to the DAC that controls the master clock oscillator. The entire sequence has a duration of less than ten microseconds.

3.14 Triggered Burst Sampling

3.14.1 Burst Control

If burst sampling is enabled by setting the ENABLE INPUT BURST control bit HIGH in the BCR, a Burst Trigger initiates the acquisition of a specific number of samples for each active channel. During a burst, sampling proceeds at the selected input sample rate until the specified number of samples has been acquired. Sampling then terminates until a subsequent trigger occurs. The number of samples acquired during a triggered burst is specified by the 24-Bit Input Burst Block Size control register (Table 3.1-1). The number of samples acquired in a burst *for each active channe*l equals the value contained in this register. The total number of samples acquired equals this value *times* the number of active channels. If a BURST BLOCK SIZE of zero is selected, a trigger initiates a nonterminating burst that continues as long as bursting is enabled, the buffer is enabled, and a sample clock is present.

A trigger can be generated by (a) asserting the S/W BURST TRIGGER control bit in the BCR, or (b) by implementing the internal burst trigger timer (3.14.2), or (c) by injecting a positive pulse of 150 nanoseconds or greater width as the EXT SYNC INP input signal at the system I/O connector. Regardless of the source of the trigger, the S/W BURST TRIGGER bit in the BCR will always be HIGH during a triggered burst, and the trigger will appear also as a 200 nanosecond positive pulse at the EXT-SYNC OUT output in the I/O connecter for synchronously triggering other boards. *Input triggers are ignored when S/W BURST TRIGGER is HIGH, of if the buffer is disabled (3.5.3.2).*

A software trigger can be applied at any time by setting the INPUT S/W TRIGGER control bit HIGH in the BCR. This bit overrides the existing CLOCK TRIGGER selection, and clears automatically.

Note: While the ENABLE INPUT BURST control bit is HIGH in the BCR, an external SYNC input will be regarded as a burst trigger, and synchronization as described in Paragraph 3.6.5.2 will not occur. To burst-trigger multiple boards, synchronize the boards before asserting ENABLE INPUT BURST.

Note: Assert the ENABLE EXT-SYNC-INP control bit HIGH in the BCR to accept external sync or trigger inputs independently of the clocking mode (Firmware Revision-008 and higher).

3.14.2 Internal Burst Timer

When the ENABLE-TRIGGER TIMER control bit is HIGH in the BCR, the internal trigger timer generates a continuous series of burst triggers. The trigger rate is determined as:

TRIGGER RATE (Hz) = Fref / TRIGGER RATE DIVISOR,

where Fref is the master clock frequency in Hertz, and TRIGGER RATE DIVISOR is defined in the Trigger Rate Divisor register shown in Table 3.14.1. Fref has a standard value of 40.000MHz.

Table 3.14.1. Trigger Rate Divisor Register

Offset: 0000 003Ch **Default: 0000 9C40h**

BIT FIELD:	DESIGNATION	FUNCTION
D[23..00]	TRIGGER RATE DIVISOR	Rate divisor for internally timed triggered bursts.
D[31..24]	(Reserved)	---

3.15 Digital I/O Port

The bidirectional digital I/O port consists of four independently controlled data bits, as shown in Table 3.15.1. Each data bit DIG IO xx DATA is a hardware input if the corresponding direction control bit DIG IO xx OUTPUT SELECT is LOW, or is an output if the control bit is HIGH. Logic polarities are retained, with a HIGH level at a connector pin associated with a HIGH level for the corresponding bit in the Digital I/O Port register. All digital I/O lines default to inputs.

Table 3.15.1. Digital I/O Port Register

Offset: 0008h **Default: 0000 000Xh**

DATA BIT	MODE	DESIGNATION	DEFAULT	DESCRIPTION
D00	RW	DIG IO 00 DATA	X	Digital I/O Data; Bits 00-03
D01	RW	DIG IO 01 DATA	X	
D02	RW	DIG IO 02 DATA	X	
D03	RW	DIG IO 03 DATA	X	
D04-D07	RW	(Reserved)	0h	
D08	RW	DIG IO 00 OUTPUT SELECT	0	DIG IO direction control; High for output.
D09	RW	DIG IO 01 OUTPUT SELECT	0	
D10	RW	DIG IO 02 OUTPUT SELECT	0	
D11	RW	DIG IO 03 OUTPUT SELECT	0	
D12-D31	RO	(Reserved)	0h	

SECTION 4.0

PRINCIPLES OF OPERATION

4.1 General Description

The PMC66-24DSI16WRC contains sixteen delta-sigma 24-Bit A/D converters and all supporting functions necessary for controlling critical acquisition parameters in a 16-Channel analog input module. A PCI interface adapter (Figure 4.1) provides the interface between the controlling PCI bus and an internal local controller through a 32-bit local bus. The local controller performs all internal configuration and data manipulation functions, including autocalibration.

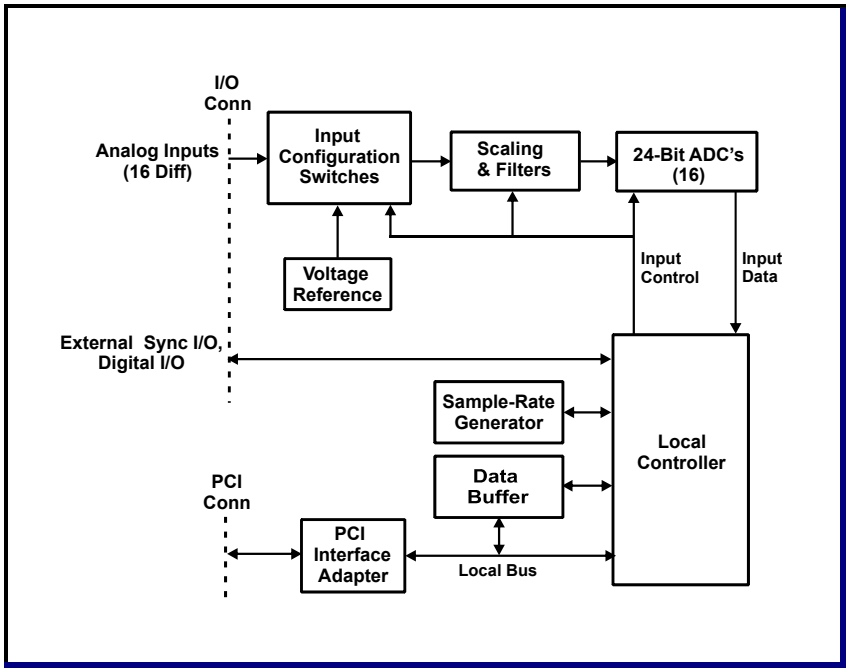

Figure 4.1. Functional Block Diagram

Input configuration switches allow the controller to select any of several signal sources as inputs to the ADC's. This feature is used to establish the internal connections necessary during autocalibration, and also permits verification from the PCI bus of the integrity of all analog input channels. All channels are calibrated against a single precision voltage reference. The offset and gain calibration of each input channel are adjusted with correction values that are determined during autocalibration.

4.2 Analog Inputs

The 16 analog input channels are arranged in two channel groups, with each group containing one-half of the channels present on the board. Either group can be designated as either active or inactive, with only active groups sending input data to the data buffer. Analog-to-digital conversions can be performed on signals from any of several sources, which are selected by the input configuration switches shown in Figure 4.1. During normal operation, the analog input signal passes through a scaling differential amplifier which controls the input range, and which suppresses any common mode voltage that might be present. During selftest and autocalibration operations, the input configuration switches can be used to replace the system input signal with either a precision zero (ground) or a positive full-scale reference voltage.

Each ADC implements a sharp-cutoff lowpass digital image filter that has a bandwidth slightly less than one-half the sampling frequency. A characteristic of this filter (and of most digital filters) is a loss of attenuation at multiples of the ADC clocking frequency. Consequently, 'images' of any out-of-band signal components present in the input signal can occur at these frequencies and can be aliased into the passband as interference. For this reason, each input signal passes through a lowpass 2nd-order Butterworth analog filter that is designed to suppress any image components that might be present in the input signals.

The final conditioned and scaled input signal is digitized by each ADC into a 24-BIt serial data word that is deserialized into parallel format by the local controller. The local controller then attaches a 4-bit channel tag to the data word, applies offset and gain correction factors, and finally transfers the corrected data to the input data buffer.

4.3 Autocalibration

Autocalibration is an embedded firmware utility that calibrates all input channels to a single internal voltage reference. The utility can be invoked at any time by the control software.

The offset error of each channel is determined first, by selecting a zero input reference level and storing the values reported from all channels. A precision internal voltage reference then is used to determine the necessary gain correction, which, like offset correction, is stored for use during normal acquisition

The internal voltage reference is adjusted to equal 99.000 percent of the selected input voltage range. This in-range value ensures that the ADC's will provide the nonsaturated, or in-range, responses that are necessary during the calibration adjustment process.

4.4 Sampling Clocks

An internal sample rate generator provides a frequency range of approximately 27-54 MHz, which is divided down by a software-specified integer to provide sample rates from 0.2-105 KSPS.

An external clock output can be assigned to replace the output of the internal rate generator, or can serve directly as the ADC sample clock. A board from which a rate generator or ADC sample clock originates is a *clock initiator*. Boards that receive and retransmit the external clock are *clock targets*. Multiple targets can be controlled from a single initiator.

4.5 Power Control

Regulated supply voltages of +5 Volts, +6 Volts and ±14 Volts are required by the analog networks. Multiple DC/DC converters in the power conditioner use +5V input power from the PCI bus to produce preregulated DC voltages that subsequently are postregulated with linear regulators to the required supply voltages. Linear regulators ensure that the final power voltages delivered to the analog networks are well-regulated and free of noise.

APPENDIX A

LOCAL REGISTER QUICK REFERENCE

APPENDIX A

LOCAL REGISTER QUICK REFERENCE

This appendix summarizes all local registers in the order in which they appear in Section 3.

Table 3.1. Control and Data Registers

Local Addr [1]	Designation	Access Mode [2]	Default	Primary Function	Ref
00	**Board Control (BCR)**	R/W	0000 383Ch	Board Control Register (BCR)	3.2
04	**Rate Control-A**	R/W	0003 2040h	PLL reference oscillator control integer.	3.6.2
08	**Digital I/O Port**	R/W	0000 000Xh	Bidirectional digital I/O port control	3.15
0C	**Clock-Source Assignments**	R/W	0000 0000h	ADC Clock source; Group disables.	3.6.1.2
10	**Rate Divisor**	R/W	0000 0005h	Sample rate divisor.	3.6.1.3
14	(Reserved)	R/W	0000 0000h	---	---
18	(Reserved)	RO	0000 0000h	---	---
1C	**Burst Block Size**	R/W	0000 0001h	Specifies the number of sample sets to be acquired in a triggered burst	3.14
20	**Buffer Control**	R/W	0003 FFFEh	Input buffer control and status	3.5.3
24	**Board Configuration**	RO	00XX XXXXh	Installed firmware and hardware options	3.10
28	**Buffer Size**	RO	000X XXXXh	Number of ADC values in the input buffer.	3.5.4
2C	Autocal Values [3]	R/W	---	---	---
30	**Input Data Buffer**	RO (DMA)	XXXX XXXXh	Input Data Buffer; Data and channel tag	3.5
34	**Auxiliary Sync I/O Control**	R/W	0000 0000h	Auxiliary external Clock and Sync control.	3.12
38	**Master Clock Adjust**	R/W	0000 8000h	Master clock frequency adjustment.	3.13
3C	**Burst Trigger Timer**	R/W	0000 9C40h	Internal trigger timer rate divisor	3.14
40-7C	(Reserved)	---	---	---	---

[1] Offsets from the PCI base address for local addressing.

[2] R/W = Read/Write; RO = Read-Only.

[3] Maintenance register; Shown for reference only

Table 3.2. Board Control Register

Offset: 0000h **Default: 0000 383Ch**

Data Bit	Designation	Mode	Def	Function	Ref
D00	AIM0	R/W	0h	Analog input mode. Selects system inputs or selftest mode. Defaults to system inputs.	3.4
D01	AIM1				
D02	RANGE0	R/W	3h	Analog input range selection. Defaults to ±10V range.	3.4.2
D03	RANGE1				
D04	OFFSET BINARY	R/W	1	Selects offset binary or two's complement input data format. Defaults HIGH to offset binary.	3.5.2.2
D05	INITIATOR OUTPUT	R/W	1	Selects INITIATOR or TARGET mode for external clock and sync output signals. Defaults HIGH to Initiator mode.	3.6.5
D06	SOFTWARE SYNC [1]	R/W	0	Initiates a local ADC sync operation when asserted. Also generates an external sync output if INITIATOR mode is selected. Clears automatically.	3.5.3.2, 3.6.4
D07	AUTOCAL [1]	R/W	0	Initiates an autocalibration operation when asserted. Clears automatically upon autocal completion.	3.7
D08	INTERRUPT A0	R/W	0h	Interrupt event selection. Default is zero.	3.8
D09	INTERRUPT A1	R/W			
D10	INTERRUPT A2	R/W			
D11	INTERRUPT REQUEST FLAG	R/W	1	Set HIGH when the board requests an interrupt. Clears the request when cleared LOW by the bus.	
D12	AUTOCAL PASS	RO	1	Set HIGH at reset or autocal initialization. Cleared LOW if autocalibration terminates unsuccessfully.	3.7
D13	CHANNELS READY	RO	1	LOW during any change in channel parameters. Asserted HIGH when inputs are ready to acquire data.	3.4.3
D14	BUFFER THRESHOLD FLAG	RO	0	Asserted HIGH when buffer contents exceed the assigned threshold.	3.5.3.1
D15	INITIALIZE [1]	R/W	0	Initializes the board when asserted. Sets all defaults.	3.3.2
D16	ENABLE TRIGGER TIMER	R/W	0	Enables the internal burst trigger timer.	3.14
D17	CLEAR BUFFER ON SYNC	R/W	0	Changes the context of the SOFTWARE SYNC to CLEAR BUFFER.	3.5.3.2
D18	RATE GEN EXT CLOCK OUT (Initiator Mode only)	R/W	0	When HIGH: Selects the internal rate generator as the external clock output source. When LOW: Selects the Group-00 sample clock. (If Group-00 external clocking is selected, the output is driven by the internal rate generator and the Group-00 divisor).	3.6.5.1
D19	HIGH SPEED ADC MODE	R/W	0	Selects the ADC High-Speed mode when HIGH, or the High-Resolution Mode when LOW.	3.6.1.3
D20	TTL EXTERNAL SYNC I/O	R/W	0	Selects TTL external sync I/O configuration.	3.6.1.2
D21	ENABLE INPUT BURST	R/W	0	Selects triggered-burst acquisition when HIGH.	3.14
D22	S/W BURST TRIGGER	R/W	0	Initiates a triggered burst when asserted. Forced HIGH during any triggered burst.	
D23	ENABLE EXT SYNC INPUT	R/W	0	The EXT SYNC INP external input is accepted, independent of the clocking mode.	
D24-31	(Reserved)	RW	0h	---	---

[1] Clears automatically.

Table 3.3.1. Configuration Operations

Operation	Maximum Duration
PCI configuration registers are loaded from internal EEPROM	3 ms
Internal control logic is configured from internal ROM	300 ms
Internal control logic is initialized	3 ms
A/D converters and clocks are initialized	20 ms

Table 3.4. Analog Input Function Selection

AIM[..0]	Function or Mode
0	Differential analog input mode.
1	(Reserved).
2	ZERO test. Internal ground reference is connected to all analog input channels.
3	+VREF test. Internal voltage reference is connected to all analog input channels.

Table 3.4.3. Analog Input Range Selection

RANGE[1..0]	Standard Input Range	Optional Alternate Input Range
0	±10mV	±1.25V
1	±100mV	±2.5V
2	±1.0V	±5V
3	±10V	±10V

Table 3.5.2. Input Data Buffer Organization

Offset: 0000 0030h **Default: XXXX XXXXh**

Selected Data Width	Reserved (Zero)	Channel Tag	Zero-Pad	Channel Data Value
16 Bits	D[31..28]	D[27..24]	D[23..16]	D[15..0]
18 Bits	D[31..28]	D[27..24]	D[23..18]	D[17..0]
20 Bits	D[31..28]	D[27..24]	D[23..20]	D[19..0]
24 Bits	D[31..28]	D[27..24]	---	D[23..0]

Table 3.5.2.2. Analog Input Data Coding; 16-Bit Data Field

	DIGITAL VALUE (Hex)	
ANALOG INPUT LEVEL	**OFFSET BINARY**	**TWO'S COMPLEMENT**
Positive Full Scale minus 1 LSB	FFFFh	7FFFh
Zero plus 1 LSB	8001h	0001h
Zero	8000h	0000h
Zero minus 1 LSB	7FFFh	FFFFh
Negative Full Scale plus 1 LSB	0001h	8001h
Negative Full Scale	0000h	8000h

Table 3.5.3. Buffer Control Register

Offset: 0000 0020h **Default: 0003 FFFEh**

Bit Field	Mode	Designation	Def	Function
D[18..00]	R/W	BUFFER THRESHOLD	0003 FFFEh	Buffer Flag Threshold
D[19]	R/W	ENABLE BUFFER INPUT	0	Enables ADC inputs to the buffer.
D[20]	R/W	CLEAR BUFFER [1]	0	Clears (empties) the buffer. Asserted HIGH while the buffer is cleared, either locally or externally.
D[22..21]	R/W	DATA WIDTH	0	Controls the width of the buffer data field: 0 => 16 bits 1 => 18 bits 2 => 20 bits 3 => 24 bits.
D[23]	R/W	DISABLE CHANNEL TAG	0	Replaces the channel tag with a zero-field.
D[24]	R/W	BUFFER OVERFLOW [2]	0	Reports buffer overflow (Write on full)
D[25]	R/W	BUFFER UNDERFLOW [2]	0	Reports buffer underflow (Read on empty)
D[31..26]	RO	(Reserved)	0h	---

[1] Clears automatically. [2] Cleared by writing LOW, or by Initialization.

Table 3.6.1.1. Channel Groups

CHANNEL GROUP	16-CHAN BOARD	8-CHAN BOARD	4-CHAN BOARD
0	Channels 00-07	00-03	00, 01
1	Channels 08-15	04-07	02, 03

Table 3.6.1.2-1. Clock-Source Assignments Register

Offset: 0000 000Ch **Default: 0000 0000h**

BIT FIELD	DESIGNATION	CHANNEL GROUP
D[03..00]	GROUP 0 CLOCK SOURCE	0
D[07..04]	GROUP 1 CLOCK SOURCE	1
D[31..08]	(Reserved)	---

Table 3.6.1.2-2. Clock-Source Assignment Codes

ASSIGNMENT CODE	GROUP 0 ASSIGNMENT	GROUP 1 ASSIGNMENT
0	Internal Rate Generator *	No effect. (Same as Group-0)
1-3	(Reserved)	
4	External Sample Clock (as rate generator input)	
5	Direct External Sample Clock (routed directly to ADC)	
6	**Disabled**	**Disabled**
7-15	(Reserved)	(Reserved)

* Applies to both channel groups. Disabling Group-0 disables both groups.

Table 3.6.1.3-1. Rate Divisor Register

Offset: 0000 0010h **Default: 0000 0005h**

BIT FIELD:	DESIGNATION	FUNCTION
D[08..00]	RATE DIVISOR (**Ndiv)**	Prescales the rate generator input frequency.
D[31..9]	(Reserved)	---

Table 3.6.1.3-2. Sample-Rate Control Parameters

PARAMETER	NOTATION	RANGE
VCO Frequency Range	**Fgen**	27 - 54 MHz nominal range
Rate Divisor	**Ndiv**	1-300
Sample Rate Range	**High-Speed Mode**	0.4 - 105 KSPS
	High-Resolution Mode	0.2 - 52.5 KSPS

Table 3.6.2-1. Rate Generator Control Register

Offset: 0004h **Default: 0003 2040h**

BIT FIELD	MODE	DESIGNATION	FUNCTION *
D[11..00]	R/W	VCO FACTOR **(Nvco)**	PLL VCO factor; 25-300.
D[23..12]	R/W	REF FACTOR **(Nref)**	PLL Reference factor; 25-300.
D[31..24]	R/W	(Reserved)	---

* For maximum phase stability, select the lowest possible values for Nvco and Nref.

Table 3.6.2-2. Rate-Generator Control Parameters

PARAMETER	NOTATION	NOMINAL RANGE
VCO Frequency Range	**Fgen**	27 - 54 MHz
Reference Frequency	**Fref**	Standard value = 40,000 kHz
VCO Factor	**Nvco**	25-300
Reference Factor	**Nref**	25-300
Nvco/Nref Factor Ratio	**Nvco/Nref**	0.67 - 1.35

Table 3.6.2-3. Sample Rate Examples

Sample Rate (KSPS)	Nvco	Vref	Fgen (Mhz)	Ndiv	MODE (BCR)
0.200	128	125	40.9600	200	High-Resolution
1.000	64	50	51.2000	50	
10.000	64	50	51.2000	5	
20.000	128	125	40.9600	2	
100.000	64	50	51.2000	1	High-Speed
105.000	168	125	53.7600	1	

Fref = 40.000MHz. All values shown in decimal format.

Table 3.8.1. Interrupt Event Selection

INTERRUPT A[2:0]	INTERRUPT EVENT CONDITION
0	Initialization completed. Default state.
1	Autocal completed
2	Channels Ready; LOW-to-HIGH transition
3	Data Buffer threshold flag, LOW-to-HIGH transition
4	Data Buffer threshold flag, HIGH-to-LOW transition
5	Triggered Burst Completed
6	(Reserved)
7	(Reserved)

Table 3.9.1. Typical DMA Register Configuration; Block Mode

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial (constant) local address of buffer	0000 0030h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

* Determined by specific transfer requirements.

Table 3.9.2. Typical DMA Register Configuration; Demand Mode

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32)	0002 1943h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial (constant) local address of buffer	0000 0030h
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

* Determined by specific transfer requirements.

Table 3.10.1. Board Configuration Register

Offset: 0000 0024h **Default: 0000 XXXXh**

BIT FIELD	DESCRIPTION
D00-D11	Firmware Revision
D12-D15	(Reserved status flags).
D16-D17	Number of input channels: 0 => 16 Channels 1 => 8 Channels 2 => 4 Channels 3 => (Reserved)
D18-D20	Image Filter Frequency: 0 => 150kHz 1 => No filter. 2-7 => (Reserved)
D21	Selectable Input Ranges: Low => ±10V, ±1V, ±100mV, ±10mV (Standard range set) High => ±10V, ±5V, ±2.5V, ±1.25V (Optional range set)
D22-D31	(Reserved)

Table 3.12.1. Auxiliary Sync I/O Control

Offset: 0000 0034h **Default: 0000 0000h**

Data Bit	Mode	Designation	Default	Description
D00-01	R/W	AUX CLOCK Control Mode	0	AUX CLOCK I/O Control Mode: 0 => Inactive 1 => Active Input 2, 3 => Active Output
D02-03	R/W	AUX SYNC Control Mode	0	AUX SYNC I/O Control Mode 0 => Inactive 1 => Active Input 2, 3 => Active Output
D04-31	RO	(Reserved)	0	Read-back as all-zero.

Table 3.14.1. Trigger Rate Divisor Register

Offset: 0000 003Ch **Default: 0000 9C40h**

BIT FIELD:	DESIGNATION	FUNCTION
D[23..00]	TRIGGER RATE DIVISOR	Rate divisor for internally timed triggered bursts.
D[31..24]	(Reserved)	---

Table 3.15.1. Digital I/O Port Register

Offset: 0008h **Default: 0000 000Xh**

DATA BIT	MODE	DESIGNATION	DEFAULT	DESCRIPTION
D00	RW	DIG IO 00 DATA	X	Digital I/O Data; Bits 00-03
D01	RW	DIG IO 01 DATA	X	
D02	RW	DIG IO 02 DATA	X	
D03	RW	DIG IO 03 DATA	X	
D04-D07	RW	(Reserved)	0h	
D08	RW	DIG IO 00 OUTPUT SELECT	0	DIG IO direction control; High for output.
D09	RW	DIG IO 01 OUTPUT SELECT	0	
D10	RW	DIG IO 02 OUTPUT SELECT	0	
D11	RW	DIG IO 03 OUTPUT SELECT	0	
D12-D31	RO	(Reserved)	0h	

APPENDIX B

Migration From PMC-24DSI12

Appendix B

Migration From PMC-24DSI12

Operation of the PMC66-24DSI16WRC is similar to that of the PMC-24DSI12. This appendix summarizes the principal similarities and differences between the two products, and is provided as a general guide rather than a definitive list of requirements or changes.

B.1. Comparison of Features

Table B.1 summarizes principal PMC-24DSI12 and PMC66-24DSI16WRC features.

Table B.1. PCI-24DSI32, PMC66-24DSI16WRC Features Comparison

Feature	PMC-24DSI12	PMC66-24DSI16WRC
Number of Input Channels	**12**	**16**
Input Ranges	**±10V, ±5V, ±2.5V**	**±10V, ±1.0V, ±100mV, ±10mV**
Sample Rate Range	**2 KSPS to 200 KSPS**	**0.2 KSPS to 105 KSPS**
Gain Stability; ±10V Range	**0.1-0.5%**	**0.06% Max**
Local Clock	**30 MHz**	**40 MHz**
GPS Synchronization	**Yes; 1PPS sync**	**No**
Burst Sampling	**No**	**Yes**
Adjustable Internal clocks	**2**	**1**
Master Clock Freq Fine-Adjust	**No**	**Yes**
External clock and sync I/O	**LVDS, TTL Front-panel only**	**LVDS, TTL, Front-panel and Internal**
Triggered-Burst Sampling	**No**	**Yes**
Digital I/O	**No**	**Yes**
Native Resolution	24 Bits	
Native Input Configuration	Differential	
Input Impedance	High (1-2 Megohms)	
Data Buffer	256 K-Sample FIFO	
Buffer DMA Access	Block and Demand Mode DMA	
Form Factor	Single-width PMC with front-panel I/O	
PCI Interface	PCI 2.3; D32; 33MHz/66MHz	
External clock and sync I/O	LVDS, TTL	
Autocalibration	On-demand	

B.2. Migration Issues

Section 2.0. Installation and Maintenance:

I/O pin assignments have changed.

Table 3.1. Control and Data Registers

The 'Rate Control B', PLL Reference Frequency' and 'GPS Synchronization' registers have been eliminated.

The 'Rate Assignments' register is redesignated as the 'Clock-Source Assignments' register.

Default values for the 'Rate Control A' and 'Rate Divisor' registers have changed.

'Burst Block Size', 'Master Clock Adjust' and 'Burst Trigger Timer' control registers have been added.

Table 3.2: Board Control Register:

The 'Asynchronous Scan' control bit has been redesignated as "Enable Trigger Timer" (3.14). All data is automatically scan-synchronized to ensure uniform ordering of input channels in the data buffer.

The ' Low Freq Filter' control bit has been deleted.

Table 3.3.2: Initialization:

The default sample rate has been reduced from 20KSPS to 10KSPS.

Table 3.5.2. Input Data Buffer Organization:

The width of the channel tag is reduced from five bits to four.

Table 3.5.3. Buffer Control Register:

A new 'Disable Channel Tag' control bit has been added, and the Lower bit field has been extended. The 'Disable Buffer Input' control bit has been redesignated as 'Enable Buffer Input' to avoid having data acquisition commence before setup operations have been completed.

Table 3.6.1. Sample Rate Control

The number of internal rate generators has been reduced from two to one. Sample-rate calculations have been modified to accommodate the ADS1271 converter.

Section 3.6.1.2. Active-Group Assignment Codes Registers

The 'Rate Assignments' and 'Rate-Generator Assignments Codes' registers have been redesignated as the 'Clock Source Assignments' and Clock-source Assignment Codes' registers.

Table 3.8.1. Interrupt Event Selection

A 'Triggered-burst termination' event has been added.

Section 3.6.3.2. External Sync

It is no longer necessary to execute a multiboard buffer reset to scan-synchronize multiple boards. The buffer reset is executed automatically now at the end of the synchronization sequence..

Section 3.6.4. Channel Synchronization

Channel synchronization is essential. See note in sections 3.6 and 3.6.4.

Section 3.9 DMA Operation

Demand-mode DMA capability has been updated to improve performance. Block mode DMA operations have been modified somewhat to conform to more recent conventions.

Section 3.10 Scan Synchronization

Section deleted. Scan synchronization is now automatic.

Section 3.12 Auxiliary External Clock and Sync

Replaces '**GPS Synchronization'.**

Section 3.13 Master Clock Adjustment

New feature.

Section 3.14 Burst Sampling

New feature.

Section 3.15 Digital I/O Port

New feature.

Revision History:

08-02-2010: Origination as preliminary draft.

09-17-2010: Updated tables 3.6.1.2-2, 3.6.2-1, 3.12.1; Paragraph 3.6.5.2.
Paragraphs 3.14, 3.15 Added burst sampling and digital I/O..

10-27-2010: General editorial updates. Notes regarding synchronization.

11-05-2010: Paragraph 2.2.1: Added note regarding forced-air cooling.
Paragraphs 3.4.1, 3.4.2: Added notes regarding the selftest voltage and overdriving the inputs.

12-22-2010: Paragraph 3.5.4: Added range of size-register contents.

06-05-2011: Paragraph 3.14.1: Revised sync-source description.
Miscellaneous editorial updates. Removed 'Preliminary' categorization.

06-19-2012: Paragraph 3.6.5.1, 3.6.5.2: Added note regarding ext-sync input implementation.

09-11-2014: Paragraph 2.4.1: Added note regarding the external sync input.

02-21-2018: Table 3-2: Added control bit D23. (Effective in Firmware Revision-008 and higher).
Para 3.14.1: Added note pertaining to the new Enable Ext Sync Input control bit.

03-15-2018: Para 3.6.3: Added note pertaining to direct external clocking.:

Additional copies of this manual or other General Standards Co. literature may be obtained from:

General Standards Corp.
8302A Whitesburg Dr.
Huntsville, Alabama 35802
Telephone: (256) 880-8787
FAX: (256) 880-8788

General Standards Corporation

High Performance Bus Interface Solutions