General Standards Corporation

High Performance Bus Interface Solutions

Rev: 063010

PMC66-16HSDI4AO4

8-Channel 16-Bit PMC Analog Input/Output Board

With Four Simultaneously-Sampled Delta-Sigma Inputs at 1.0 MSPS,

Four Analog Outputs at 1.0 MSPS,

And 16-Bit Digital I/O Port

REFERENCE MANUAL

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SECTION 1.0

INTRODUCTION

The single-width PCI mezzanine card PMC66-16HSDI4AO4 provides 16-bit analog input and output capability for PMC applications. Four sigma-delta analog input channels (Figure 1.1-1) are digitized simultaneously at rates up to 1,000,000 conversions per second per channel, with software-controlled voltage ranges of ±10V, ±5V or ±2.5V. Digitized input data is buffered through a 256K-sample FIFO.

Four 16-bit analog output channels provide software-selected output ranges of ±10V, ±5V or ±2.5V, and are accessed either directly through dedicated control registers, or through a 256K-sample FIFO buffer. The analog output buffer can be clocked at rates up to 1,000,000 output samples per second per channel. The inputs and outputs can be configured to operate at a common clocking rate.

A 16-Bit bidirectional digital port is configurable as two independent byte-wide ports.

The board is designed for minimum off-line maintenance. All functional parameters are under software control, thereby eliminating field-configuration jumpers. A selftest switching network routes output channels or calibration reference signals to the analog inputs, and permits board integrity to be verified by the host.

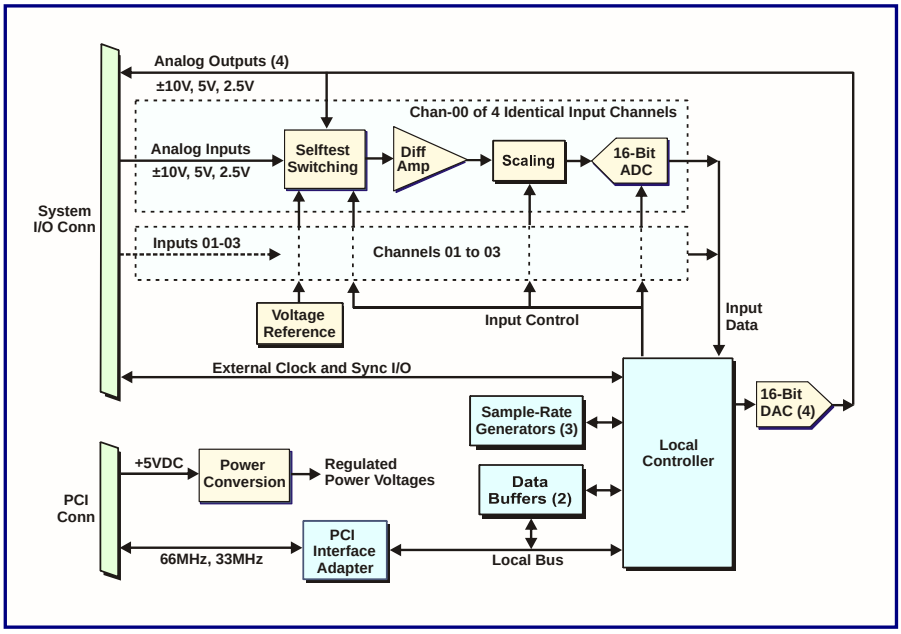

Figure 1.1-1. Functional Organization

This product is functionally compatible with the IEEE PCI local bus specification Revision 2.3, and supports the "plug-n-play" initialization concept. System connections are made at the front panel through a high-density dual-ribbon 80-pin connector. Electrical power is derived from +5VDC supplied by the PCI bus, and analog power voltages are generated internally. Universal signaling is supported, and all operational parameters are software configurable. Operation over the specified temperature range is achieved with conventional convection cooling.

SECTION 2.0

INSTALLATION AND MAINTENANCE

2.1 Board Configuration

This product has no field-alterable configuration features, and is completely configured at the factory for field use.

2.2 Installation

2.2.1 Physical Installation

To minimize the opportunity for accidental damage before installation, the board should be stored in the original protective shipping envelope. System power must be turned OFF before proceeding with the installation.

CAUTION: This product is susceptible to damage from electrostatic discharge (ESD). Before removing the board from the conductive shipping envelope, ensure that the work surface, the installer and the host board have been properly discharged to ground.

After removing the board from the shipping envelope, position the board with the shield and standoffs facing the host (carrier) board, and with the I/O connector oriented toward the front panel (Figure 2.2-1). Align the two PCI connectors located at the end of the board opposite the I/O connector, with the mating connectors on the host board. Then carefully press the board into position on the host. Verify that the PCI connectors have mated completely and that the standoffs are seated against the host board.

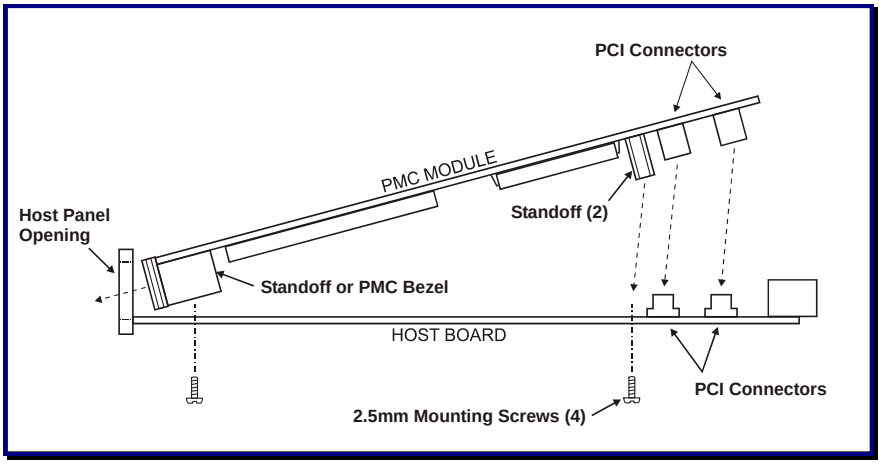

Figure 2.2-1: PMC Physical Installation

Attach the board to the host with four 2.5 x 6.5mm panhead screws. Pass the screws through the back of the host into the four mounting holes on the board. Tighten the screws carefully to complete the installation. Do not overtighten.

2.2.2 Input/Output Cable Connections

System cable signal pin assignments are listed in Table 2.2-1. The I/O connector is designed to mate with an 80-pin dual-ribbon connector, equivalent to Robinson Nugent #P50E-080S-TG. The Robinson Nugent insulation displacement connector accepts two 40-wire 0.050-inch ribbon cables, with the pin numbering convention shown in Table 2.2-1 and in Figure 2.2-2. Contact the factory if preassembled cables are required.

Table 2.2-1. System I/O Connector Pin Functions

PIN	ROW-A SIGNAL
1	OUTPUT RTN
2	ANA OUT 00
3	OUTPUT RTN
4	ANA OUT 01
5	OUTPUT RTN
6	ANA OUT 02
7	OUTPUT RTN
8	ANA OUT 03
9	INPUT RTN
10	INPUT RTN
11	INP00 LO
12	INP00 HI
13	INPUT RTN
14	INPUT RTN
15	INP01 LO
16	INP01 HI
17	INPUT RTN
18	INPUT RTN
19	INP02 LO
20	INP02 HI
21	INPUT RTN
22	INPUT RTN
23	INP03 LO
24	INP03 HI
25	INPUT RTN
26	INPUT RTN
27	INPUT RTN
28	INPUT RTN
29	INPUT RTN
30	INPUT RTN
31	INPUT RTN
32	INPUT RTN
33	INPUT RTN
34	INPUT RTN
35	INPUT RTN
36	INPUT RTN
37	INPUT RTN
38	INPUT RTN
39	INPUT RTN
40	INPUT RTN

PIN	ROW-B SIGNAL
1	DIGITAL RTN
2	DIO 00
3	DIGITAL RTN
4	DIO 01
5	DIGITAL RTN
6	DIO 02
7	DIGITAL RTN
8	DIO 03
9	DIGITAL RTN
10	DIO 04
11	DIGITAL RTN
12	DIO 05
13	DIGITAL RTN
14	DIO 06
15	DIGITAL RTN
16	DIO 07
17	DIGITAL RTN
18	DIO 08
19	DIGITAL RTN
20	DIO 09
21	DIGITAL RTN
22	DIO 10
23	DIGITAL RTN
24	DIO 11
25	DIGITAL RTN
26	DIO 12
27	DIGITAL RTN
28	DIO 13
29	DIGITAL RTN
30	DIO 14
31	DIGITAL RTN
32	DIO 15
33	VTEST RTN
34	VTEST
35	DIGITAL RTN
36	OUTPUT CLK I/O
37	DIGITAL RTN
38	TRIGGER I/O
39	DIGITAL RTN
40	INPUT CLK I/O

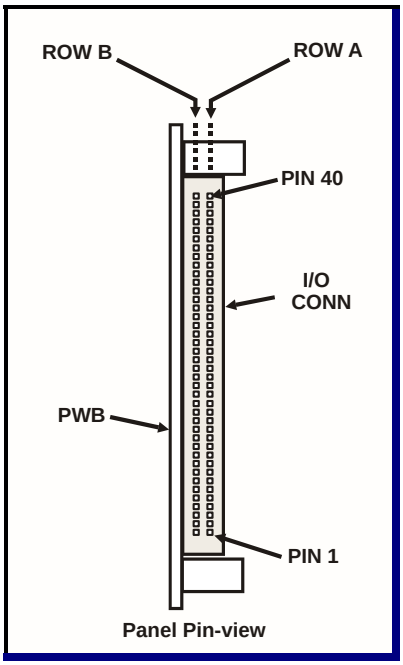

Figure 2.2-2. System I/O Connector

2.3 System Configuration

2.3.1 Analog Inputs

The four analog input channels can be software-configured for either differential or single-ended operation. The hardware input configuration must be acknowledged by the control software.

2.3.1.1 Differential Inputs

Differential input operation usually provides the best performance, and is essential when the input signal sources are not isolated from each other or have returns that are at significantly different potentials. A potential difference between grounds is significant if it is larger than the maximum tolerable measurement error.

This operating mode also offers the highest rejection of the common mode noise, which is a characteristic of long cables in typical instrumentation environments. When operating in the differential mode, shown in Figure 2.3-1a, the wire pair from each signal source is connected between the HI(+) and LO(-) inputs of a single input channel. The input return (INPUT RTN in Table 2.2-1) is connected to a ground point which ensures that the sum of the signal level **(Vsig)** and the common mode voltage **(Vcm)** remains within the range specified for the board. Ground current through the INPUT RTN pins must be limited in order to avoid damage to the cable or the input board.

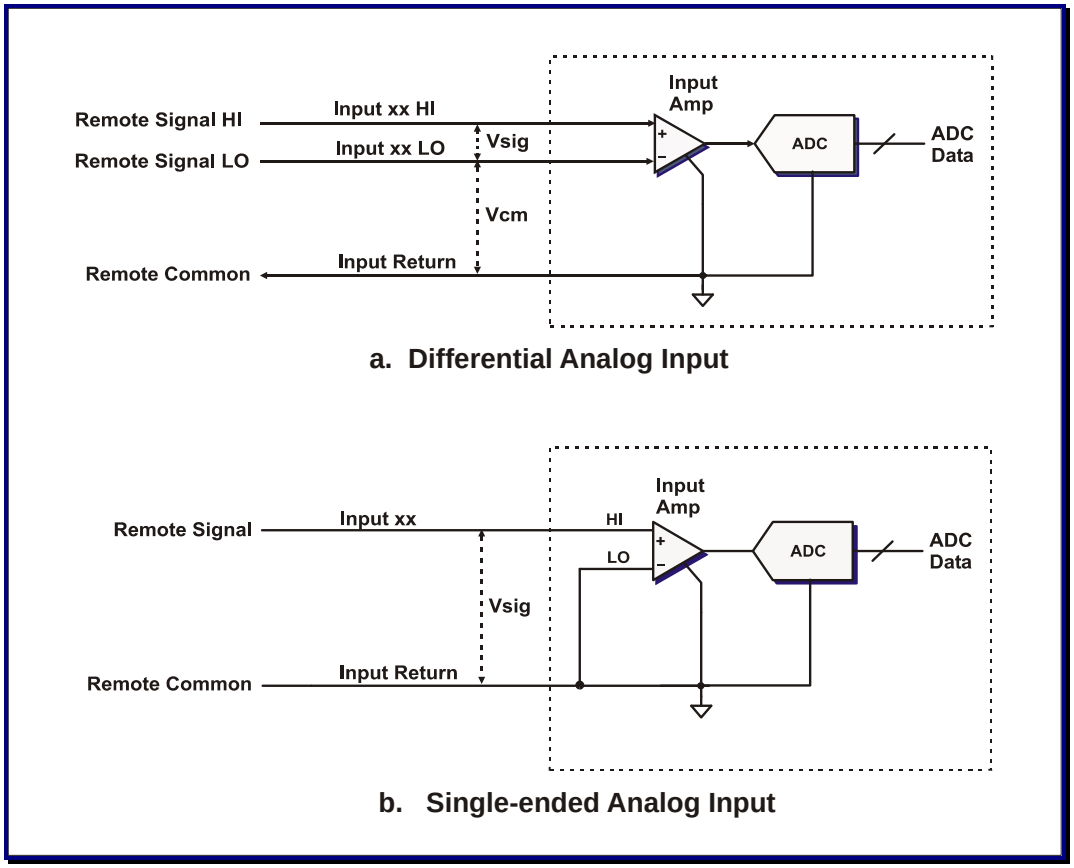

Figure 2.3-1. Analog Input Configurations

2.3.1.2 Single-Ended Inputs

Single-ended operation (Figure 2.3-1b) generally provides acceptable performance only when the input signal sources either are isolated from each other, or are common to a single isolated signal return. A single-ended configuration usually is more susceptible to system interference than a differential configuration.

Single-ended inputs share a common input return that provides a return path for all inputs, making isolation from other system grounds a critical issue. If the signal sources are returned externally to system ground when operating in this mode, a potential difference between the system ground and input return can cause erroneous measurements, or could generate potentially destructive ground current.

For applications in which multiple signal sources share a single ground, the differential configuration is recommended, with all "LO" inputs connected together at the common remote return.

2.3.2 Analog Outputs

2.3.2.1 Output Configurations

The four analog output channels are single-ended and have a common signal return that is referred to in Table 2.2-1 as OUTPUT RTN. Single-ended outputs should drive only loads that have high impedances to system ground. The best results are obtained when the loads are isolated also from each other.

Figure 2.3-2 shows the primary sources of error in both isolated and nonisolated system configurations. For loads that are isolated from each other (Figure 2.3-2a), the total line-loss error is twice the loss produced in a single line, assuming equal wire size and length for output and return lines. For loads with a common return that is isolated from system ground, line loss in the common return appears as crosstalk between channels.

If the load return is connected to a remote system ground (Figure 2.3-2b), the potential difference **Vgnd** between the remote ground and the internal signal return will introduce an error into the signal delivered to the load. The ground current **Ignd** developed in the return line is limited essentially only by **Rgnd**, and can damage the cable or the board if not controlled.

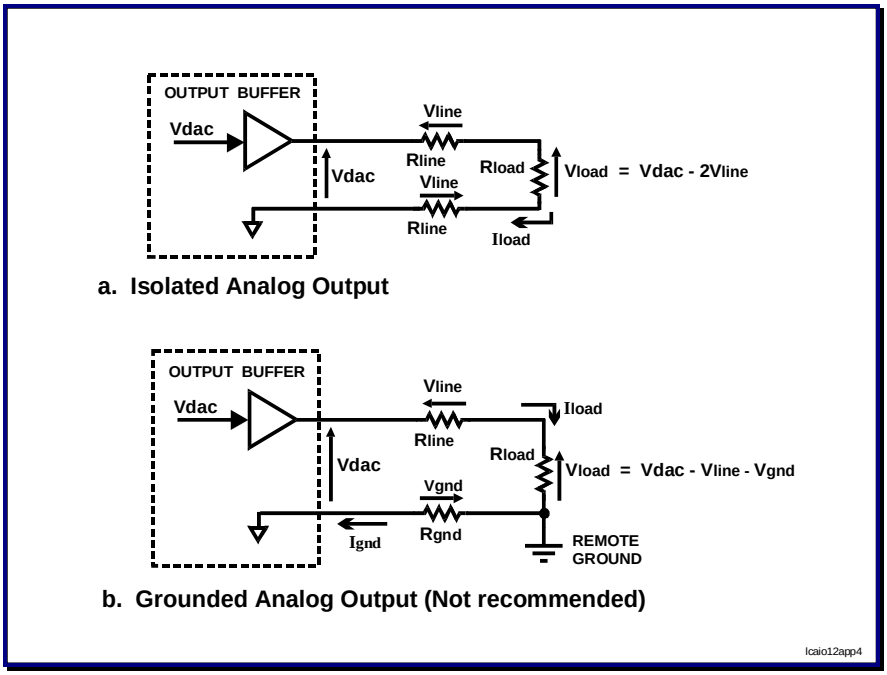

Figure 2.3-2. Output Configurations

2.3.2.2 Loading Considerations

The voltage drop in the system I/O cable can be a significant source of error, especially with relatively long cables driving moderate or heavy loads. Figure 2.3-3 shows the effect of load current on the voltage drop in copper wire of various sizes. A 4.0 milliamp load for example, inserts a voltage drop of more than 0.25 millivolt *per foot* in #28 AWG ribbon cable; twice that if the return line also is considered. Several feet of ribbon cable therefore can produce significant errors, especially in a 16-bit system, in which 1 LSB can represent

only 76 microvolts on a ±2.5 Volt range. High impedance loads generally do not produce significant DC errors.

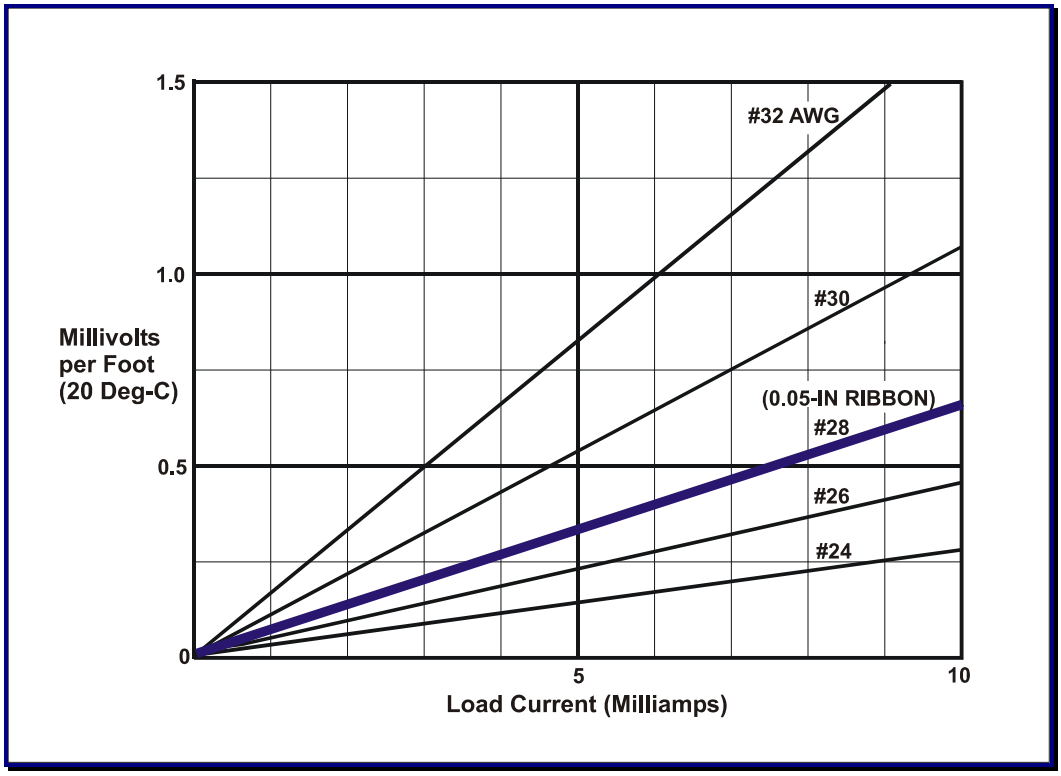

Figure 2.3-3. Line Loss versus Load Current

2.3.3 Multiboard Clocking and Synchronization

Analog input converters on multiple boards can be:

a. Clocked from a single clock source (Multiboard clocking), and/or:

b. Synchronized to a common time reference (Multiboard synchronization).

Clocking multiple converters from a single source prevents the *sampling drift* that occurs when converters are clocked from different sources. *Synchronizing* the converters on multiple boards causes the converters to initiate conversions simultaneously, and can be used to eliminate *sampling skew* between channels.

2.3.3.1 Interboard Connections

Figure 2.3-4 illustrates how multiple PMC66-16HSDI4AO4 boards can be daisy-chained together in an initiator-target sequence to provide common clocking between boards. The INPUT CLK I/O line from an initiator is connected to the INPUT CLK I/O line on each target board, and the TRIGGER I/O and OUTPUT CLK I/O lines are connected similarly. Multiple boards can be multi-dropped together for synchronous operation.

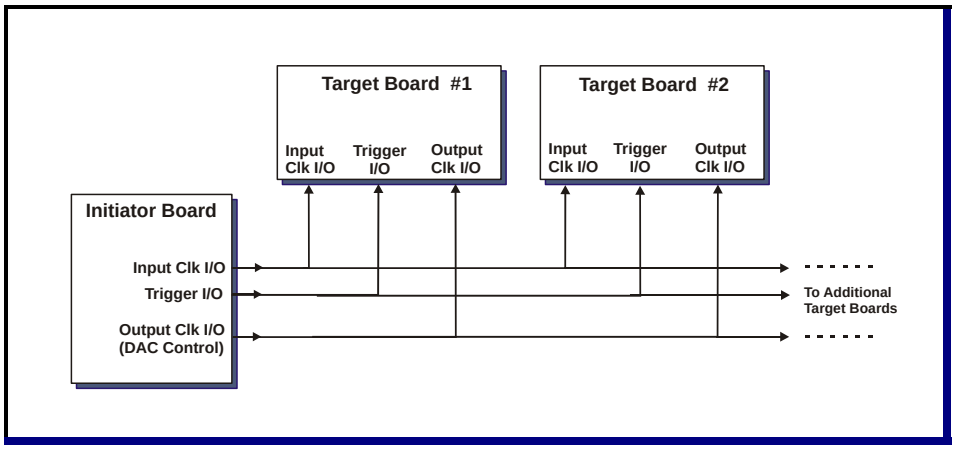

Figure 2.3-4. Multiboard Clock/Sync Connections

Application software controls the designation of each board as an initiator or a target. When a board is software-configured as an ***Initiator***, these I/O signals are outputs that can be used to control multiple *Target* boards. The INPUT CLK I/O ouput is a square wave operating at the ADC clocking frequency (3.7.1). The TRIGGER I/O output is a 70-150 nanosecond pulse, asserted LOW, that occurs at the beginning of each locally triggered burst. Each analog output clock generates a simultaneous 70-150 nanosecond LOW pulse at the OUTPUT CLK I/O output. Output loading on the Initiator should be limited to 8 milliamps or less.

Note: External clock and trigger inputs can be provided from sources other than an initiator board

For ***Target*** boards, the I/O signals become inputs and can synchronize local input and output operations to an Initiator board. The INPUT CLK-I/O input is used internally as Fgen-a (3.7.1). TRIGGER I/O and OUTPUT CLK I/O inputs are edge-detected on the negative (falling) edge, and must be asserted for at least 60 nanoseconds in order to be acknowledged. All three inputs are pulled up internally to +5V through approximately 33 KOhms.

2.3.3.2 Multiboard Synchronization

Boards that are interconnected for multiboard synchronization initiate internal *synchronization sequences* each time a sync pulse is generated by the initiator board. The sync I/O can also be used to reset (clear) the data buffers on target boards.

2.4 Maintenance

This product requires no scheduled maintenance other than periodic verification and possible adjustment of the internal voltage reference. The optimum verification interval will vary with upon the specific application, but in most instances an interval of one year should be sufficient.

In the event of a suspected malfunction, all associated system parameters, such as power voltages, control bus integrity, and system interface signal levels, should be evaluated before troubleshooting of the board itself is attempted. A board that has been determined to be defective should be returned to the factory for detailed problem analysis and repair.

2.5 Reference Verification

All analog channels are software-calibrated to a single internal voltage reference by an embedded autocalibration utility. The procedure presented here describes the verification and adjustment of the reference.

2.5.1 Equipment Required

Table 2.5-1 lists the equipment required for verifying or adjusting the internal reference. Alternative equivalent equipment may be used.

Table 2.5-1. Reference Verification Equipment

EQUIPMENT DESCRIPTION	MANUFACTURER	MODEL
Digital Multimeter, 5-1/2 digit, 0.005% accuracy for DC voltage measurements at ±10 Volts. Input impedance 10 Megohms or greater.	Hewlett Packard	34401A
Host board with single-width PMC adapter	(Existing host)	---
Test cable; suitable for connecting the digital multimeter to the system I/O connector.	---	---

2.5.1 Verification and Adjustment

The following procedure describes the verification of the internal voltage reference. Adjustment of the internal reference, if necessary, is performed with an internal trimmer that is accessible as shown in Figure 2.5-1.

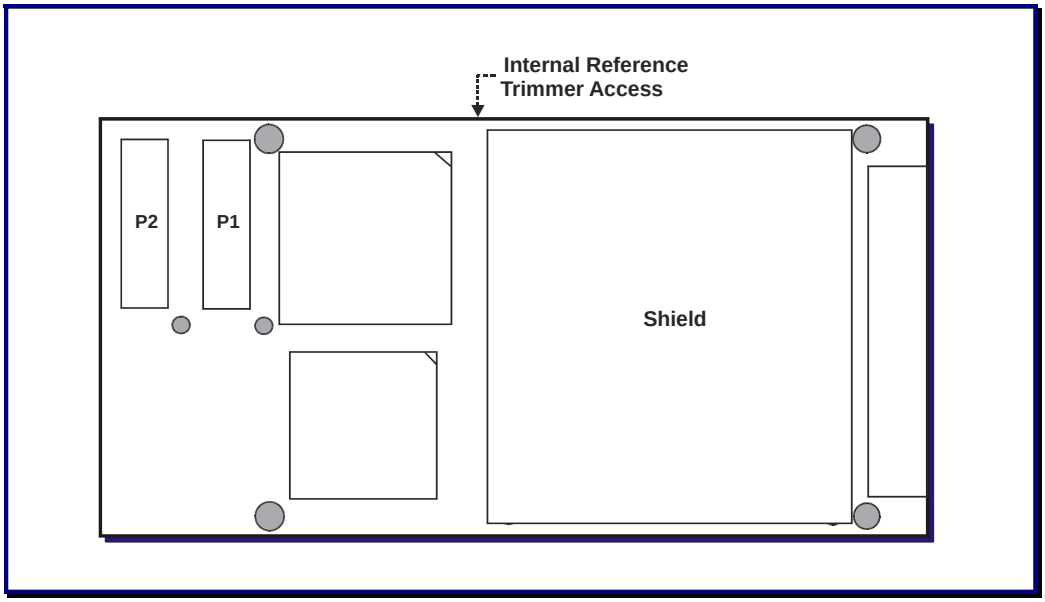

Figure 2.5-1. Reference Adjustment Access

This procedure assumes that the PMC is installed on a host board, and that the host is installed in a system.

1. Connect the digital multimeter between the VTEST pin (+), and the VTEST RTN pin (-) in the System I/O connector.
2. If power has been removed from the board, apply power now. Wait at least 10 minutes after power is applied before proceeding..
3. Verify that the digital multimeter indication is +9.9000 VDC ±0.0015 VDC. If the indication is not within this range, adjust the internal reference trimmer for an in-range digital multimeter indication.
4. Verification and adjustment is completed. Remove all test connections.

SECTION 3.0

CONTROL SOFTWARE

3.1 Introduction

The PMC66-16HSDI4AO4 is compatible with the PCI Local Bus specification Revision 2.3, and a PLX™ PCI-9056 adapter controls the PCI interface. Configuration-space registers are initialized internally to support the location of the board on any 32-longword boundary in memory space. After initialization is completed, communication between the PCI bus and the local bus takes place through the control and data registers listed in Table 3.1-1. All data transfers are long-word D32. DMA access is supported for data transfers from the analog input buffer and to the analog output data buffer. To ensure compatibility with subsequent controller revisions, reserved control bits should be written LOW (zero), and maintenance registers should not be modified.

Table 3.1-1. Control and Status Registers

OFFSET (Hex)	REGISTER	MODE[1]	DEFAULT	PRIMARY FUNCTION	REF
0000	BOARD CONTROL	RW	2202 0020h	Board Control Register (BCR).	3.2
0004	DIGITAL I/O PORT	RW	00XX 00XXh	16-Bit Digital I/O port data.	3.9
0008	ANALOG OUTPUT CHAN 00	RW	0000 8000h	Output Channel 00 data.	3.12
000C	ANALOG OUTPUT CHAN 01	RW	0000 8000h	Output Channel 01 data.	
0010	ANALOG OUTPUT CHAN 02	RW	0000 8000h	Output Channel 02 data.	
0014	ANALOG OUTPUT CHAN 03	RW	0000 8000h	Output Channel 03 data.	
0018	ANALOG INPUT BUFFER	RO	00XX XXXXh	Analog input buffer data.	3.4.5
001C	RATE GENERATOR A	RW	0103 F020h	Rate-A generator control	3.7.1
0020	RATE GENERATOR B	RW	0000 2760h	Rate-B generator divider; 24 bits.	3.7.2
0024	INPUT CONFIGURATION	RW	0F00 0400h	Analog inputs channel-mask and burst-size.	3.4.2 3.4.4.2
0028	INPUT BUFFER SIZE	RO	0000 0000h`	Number of data values in the input buffer.	3.4.5.2
002C	INPUT BUFFER THRESHOLD	RW	0003 FFFEh	Input buffer status flag threshold.	3.4.5.2
0030	PRIMARY STATUS	RW	0000 0X00h	Principal status-flag register	3.11
0034	ASSEMBLY CONFIGURATION	RO	000X XXXXh	Options and firmware revision.	3.16
0038	Autocal Values [2]	RW	0000 XXXXh	Autocal value readback.	---
003C	BUFFERED OUTPUT OPERATIONS	RW	0000 104Fh	Buffered Analog Outputs Control	3.13
0040	OUTPUT BUFFER THRESHOLD	RW	0003 FFFEh	Output buffer status flag threshold.	3.13.2.3
0044	OUTPUT BUFFER SIZE	RO	0000 0000h	Number of data values in the output buffer.	3.13.2.3
0048	ANALOG OUTPUT BUFFER	WO	0000 0000h	Analog Output Data Buffer.	3.13.2
004C	RATE GENERATOR C	RW	0000 007Eh	Rate-C generator divider; 24 bits.	3.13.4.1.2
0050-005C	(Auxiliary Registers)	RW	0000 0000h	Four auxiliary 32-Bit user registers. No internal functions.	---
0060	MASTER CLOCK ADJUST	RW	0000 8000h	Master clock frequency adjustment.	3.17
0064-007C	(Reserved)	---	---	---	---

Notes: 1. RW = Read/Write, RO = Read-Only, WO = Write-Only.
2. Maintenance register; Shown for reference only.

3.2 Board Control Register (BCR)

Basic board functions such as initialization, autocalibration and input/output range selection are controlled through the board control register (BCR) shown in Table 3.2-1. Specific control bits are cleared automatically after the associated operations have been completed. Read-only status flags indicate the states of specific operational functions.

3.3 Configuration and Initialization

3.3.1 Board Configuration

During *board configuration*, initial values for both the PCI configuration registers and the internal control logic are extracted from internal nonvolatile read-only memory. This process is initiated by a PCI bus reset, and should be required only once after the initial application of power. While the PCI configuration registers are being loaded, the response to PCI target accesses is RETRY's. Configuration operations are executed in the sequence shown in Table 3.3-1.

Loading of the PCI configuration registers is completed within 3 milliseconds after the assertion of a PCI bus reset.

3.3.2 Initialization

Internal control logic can be initialized without invoking a full reconfiguration by setting the INITIALIZE control bit HIGH in the BCR. This action initializes the internal logic, but does not affect the PCI configuration registers and does not reconfigure the internal control logic. Initialization requires 3 milliseconds or less for completion, and produces the following default conditions:

- The BCR is initialized; all register defaults are invoked. (Paragraph 3.3).
- Analog input and output data coding is offset binary. (3.6).
- All analog input and output channels are active. (3.4.2, 3.13.1.1.1).
- Analog input and output ranges are ±10V. (3.4.3, 3.13.1.3).
- External clock and trigger signals are in the target (Input) mode. (3.8, 3.13.6).
- The input and output buffers are reset to empty. (3.4.5.1, 3.5.1, 3.13.2.3).
- Analog Inputs:
  - Input channels are differential. (3.4.1.1).
  - Sample clocking is from the Rate-A generator; Bursting is disabled. (3.4.4.2, 3.7).
  - The ADC (Rate-A) generator is adjusted to 320 kHz, and is disabled. (3.7.1),
  - The analog input buffer is reset to empty; buffer threshold is 3FFFEh. (3.4.5).
  - Burst block size is 1024 (0400h). (3.4.4.2).
- Analog Outputs:
  - Analog outputs are at midrange (zero). (3.6).
  - Direct-Register access is selected. (3.12).
  - The DAC (Rate-C) generator is adjusted to 320 kHz, and is disabled. (3.13.4.1.2).
- The burst-trigger (Rate-B) generator is adjusted to 4 kHz, and is disabled. (3.7.2)
- The digital I/O port is configured as two input bytes. (3.9).

Table 3.2-1. Board Control Register (BCR)

Offset: 0000h **Default: 2202 0020h**

BIT	MODE [1]	DESIGNATION	DEF	DESCRIPTION	REF
D00-D02	RW	ANALOG INPUT MODE	0	Analog input mode: 0 => Differential system inputs 1 => Single-ended system inputs 2 => Zero selftest 3 => VREF selftest 4 => Output Channel 00 5 => Output Channel 01 6 => Output Channel 02 7 => Output Channel 03	3.4.1
D03	R/W	(Reserved)	0	---	---
D04-D05	RW	INPUT RANGE	2	Analog input range: 0 => ±2.5V 2 => ±10V 1 => ±5V 3 => (Reserved)	3.4.3
D06-D07	RW	(Reserved)	0	---	---
D08	RW	INPUT S/W CLOCK [2]	0	Initiates a single sample of active input channels. Overrides existing input clocking source.	3.4.4
D09	RW	ENABLE INPUT BURST	0	Enables triggered burst input acquisition.	3.4.4.2
D10	RO	INPUT BURST BUSY	0	HIGH when a triggered input burst is in progress.	3.4.4.2
D11	RW	INPUT S/W TRIGGER [2]	0	Initiates a single input data burst. Overrides existing burst triggering source.	3.4.4.2
D12	RW	ENABLE INPUT BUFFER	0	Enables the analog input buffer for accepting data.	3.4.5.1
D13	RW	CLEAR INPUT BUFFER [2]	0	Clears (empties) the analog input data buffer.	3.4.5.1
D14	RO	INPUT BUFFER THRESHOLD FLAG [3]	0	HIGH when the number of values in the input buffer exceeds the selected buffer threshold.	3.4.5.2
D15	RW	INPUT BUFFER OVERFLOW	0	Set HIGH if the input buffer overflows. Stays HIGH until cleared from the bus or by a board reset.	3.4.5.1
D16-D17	RW	OUTPUT RANGE	2	Analog Output Voltage Range: 0 => ±2.5V 2 => ±10V 1 => ±5V 3 => (Reserved)	3.12.1 3.13.1.2
D18	RW	SIMULTANEOUS OUTPUTS	0	When HIGH, all outputs update simultaneously in response to an output clock. When LOW, each output is updated immediately when new data is received.	3.12.2.2
D19	RW	ENABLE BUFFERED OUTPUTS	0	When HIGH, enables the analog output FIFO buffer, and disables the analog output registers ANALOG OUTPUT CHAN xx.	3.13
D20	RW	OUTPUT S/W CLOCK [2, 3, 4]	0	Produces a single analog output clock. Overrides existing output clocking source.	3.13.4.1
D21	RW	TRIGGER INITIATOR	0	Configures the shared analog input/output hardware trigger pin as an output if HIGH, or as an input if LOW.	3.4.4.2 3.13.5.2
D22	R/W	ENABLE RATE-C GENERATOR	0	Enables the Rate-C generator for analog outputs.	3.13.4.1.2
D23	R/W	INPUT BUFFER UNDERFLOW [5]	0	Set HIGH if the input buffer underflows. Stays HIGH until cleared from the bus or by a board reset.	3.4.5.1
D24	RW	ANALOG INPUT CLK INITIATOR	0	Configures the analog input I/O clock as an *output* if HIGH, or as an *input* if LOW.	3.8
D25	RW	OFFSET BINARY	1	Selects offset-binary analog I/O data format when HIGH, or two's complement when LOW.	3.6
D26	RW	ENABLE RATE-A GENERATOR	0	Enables the Rate-A generator for analog inputs.	3.7.1
D27	RW	ENABLE RATE-B GENERATOR	0	Enables the Rate-B generator for triggered bursts.	3.7.2
D28	RW	AUTOCAL [2]	0	Initiates an autocalibration operation when asserted. Clears automatically upon completion,	3.10
D29	RO	AUTOCAL PASS	1	Set HIGH at reset or autocal initialization. A HIGH state after autocal confirms a successful calibration.	3.10
D30	R/W	SWAP DEMAND MODE CHANNELS	0	Reverses the default demand-mode DMA channels for analog inputs and outputs	3.5.2 3.15.2
D31	RW	INITIALIZE [2]	0	Initializes the board. Sets all register defaults.	3.3.2

Notes: 1. RW = Read/Write, RO = Read-Only. 2. Clears automatically. 3. Duplicated elsewhere
4. May invoke immediate mode output clocking in some systems.
5 Remains HIGH until cleared by a direct write as LOW, or by initialization.

Table 3.3-1. Configuration Operations

Operation	Maximum Duration
PCI configuration registers are loaded from internal ROM	3 ms
Internal control logic is configured from internal ROM	300 ms
Internal control logic is initialized	3 ms

3.4 Analog Inputs

Each of four analog input channels can be digitized simultaneously with 16-bit resolution at rates from 30KSPS to 1.0 MSPS. Data from any combination of inputs can be acquired in a 256 Ksample buffer, and a tag-bit is attached to the first (lowest-numbered) active channel data values. Three voltage ranges are available, and any two of these ranges can be used simultaneously on different channels. Each input channel contains a dedicated 16-Bit ADC.

All active inputs are sampled simultaneously, and the sample clock can be derived: (a) from an internal rate generator, (b) from an external hardware clock input, or (c) directly from the bus.

To illustrate the requirements for initiating analog input acquisition directly after board initialization, setting the following control bits HIGH simultaneously in the BCR would start four-channel acquisition using the Rate-A generator at the default sample rate:

- ANALOG INPUT CLK INITIATOR; Selects the analog input clock initiator mode,
- ENABLE INPUT BUFFER; Enables the analog input buffer,
- ENABLE RATE-A GENERATOR: Enables the Rate-A generator.

3.4.1 Input Modes

An input switching network routes either the system input signals or internal test signals through the input channels, and is controlled by the ANALOG INPUT MODE control field in the BCR. The system inputs are disconnected when internal signals are monitored, and have no effect on test results.

3.4.1.1 System Inputs

Of the eight possible input modes available through the ANALOG INPUT MODE field, two are dedicated to system inputs. In the differential configuration, the signal present between the HI and LO inputs in each channel is acquired. For a single-ended input, the input signal is measured between the HI input and the input return, and the LO input is ignored. The selected system input configuration must agree with the system wiring configuration (Paragraph 2.3).

3.4.1.2 Test Modes

Internal analog nodes can be monitored to verify the functional integrity of the board. The selected input ranges apply in all input modes, including test modes. The following signals are present in *all input channels* when the indicated test modes are selected:

Zero Selftest: Midscale value, ideally equal to 0.000 VDC,

VREF Selftest: Internal voltage reference, ideally equal to +99.00 percent of the ***selected analog output range*** *,

Output Channels: Any of the four analog output channels.

* The VREF Selftest source and the Output DAC's share a common reference.

3.4.2 Active Channel Selection

Input channels are designated as active by setting the corresponding ENABLE CHANNEL XX control bit HIGH in the Input Configuration register (Table 3.4-1), or as inactive by clearing the bit LOW. All active inputs are sampled simultaneously when a sample clock occurs. Inactive channels produce no data in the input buffer.

Table 3.4-1. Input Configuration Register

Offset: 0024h **Default: 0F00 0400h**

BIT	MODE *	DESIGNATION	DEF	DESCRIPTION
D00-D23	RW	BURST BLOCK SIZE	0400h	Number of active channel sets acquired during a triggered burst.
D24	RW	ENABLE INPUT 00	1	Analog input channel selection mask.
D25	RW	ENABLE INPUT 01	1	
D26	RW	ENABLE INPUT 02	1	
D27	RW	ENABLE INPUT 03	1	
D28-D31	RW	(Reserved)	0	---

* RW = Read/Write, RO = Read-Only.

3.4.3 Input Ranges

The analog inputs can be assigned a fullscale input range of ±10V, ±5V or ±2.5V by the INPUT RANGE control field in the BCR. Input voltage levels outside the selected ranges will produce saturation codes of plus or minus fullscale, but will not damage the inputs if they are within the range indicated in the product specification for overvoltage protection.

Note: All input ranges are calibrated during autocalibration, regardless of which input range is selected.

3.4.4 Sampling Modes

All active channels are sampled at each occurrence of the analog input sample clock. If the ANALOG INPUT CLK INITIATOR control bit is HIGH in the BCR, input sample clocks are supplied by either the Rate-A generator or by the INPUT S/W CLOCK control bit in the BCR. If the INITIATOR control bit is HIGH, a squarewave operating at the ADC clocking frequency (3.7.1) appears as an output at the bidirectional INPUT CLK I/O pin in the system I/O connector.

If the INITIATOR control bit is LOW, designating the board as a ***Target***, the INPUT CLK I/O pin becomes an input, and an input squarewave on that pin is used directly internally as the ADC sampling clock. The Rate-A generator is ignored in the target clocking mode, as is the INPUT SW CLOCK control bit.

To avoid contention among multiple boards interconnected for multiboard synchronous operation, the INITIATOR control bit defaults LOW for target mode.

3.4.4.1 Continuous

During continuous sampling, all active input channels are sampled continuously as long as a clock source is present. Continuous sampling is selected when the ENABLE INPUT BURST control bit is LOW in the BCR.

3.4.4.2 Burst Sampling

If burst sampling is enabled by setting the ENABLE INPUT BURST control bit HIGH in the BCR, an input trigger initiates the acquisition of a specific number of samples for each active channel. During a burst, sampling proceeds at the selected input sample rate until the specified number of samples has been acquired, and then terminates until a subsequent trigger occurs. The number of samples acquired during a triggered burst is specified by the 24-Bit BURST BLOCK SIZE control field in the Input Configuration register (Table 3.4-1). The value in this field is the number of samples acquired *for each active channe*l, and the total number of samples acquired equals this value *times* the number of active channels.

Note: If a BURST BLOCK SIZE of zero is selected while bursting is enabled, a burst trigger initiates a nonterminating burst that continues until either the sample clock is disabled or the input buffer goes full.

The END OF BURST status bit in the input buffer (Paragraph 3.4.5) is set HIGH for the last input value acquired in a burst. The INPUT BURST BUSY status flag in the BCR is HIGH during each triggered burst, and is LOW otherwise. *Input triggering cannot occur when INPUT BURST READY is LOW.*

If the TRIGGER INITIATOR control bit in the BCR is HIGH, the board is a trigger ***initiator***, and a burst trigger is provided either by the Rate-B generator or by the INPUT S/W TRIGGER control bit in the BCR. The INPUT S/W TRIGGER bit always produces a burst trigger, regardless of the state of the Rate-B generator or the INITIATOR control bit. In the ***Initiator*** mode, each burst trigger produces a 70-150 nanosecond LOW output pulse at the bidirectional TRIGGER I/O pin in the system I/O connector.

If the TRIGGER INITIATOR control bit is LOW (default), indicating *Target Mode*, the TRIGGER I/O pin becomes an input, and a trigger is generated for each HIGH-to-LOW transition received at the pin. The Rate-B generator is ignored in the target clocking mode, but the INPUT S/W TRIGGER control bit remains active.

NOTE: If TRIGGER INITIATOR is HIGH (initiator mode), the TRIGGER I/O pin is an output and produces a trigger pulse in response to either an input trigger or an output trigger (3.13.5.2). If the control bit is LOW (target mode), an input HIGH-to-LOW transition at the TRIGGER I/O pin produces either an input or output trigger if either is enabled individually, or inputs and outputs simultaneously if both are enabled.

3.4.5 Input Data Buffer

3.4.5.1 Organization

Analog input data accumulates in the input data FIFO buffer until extracted by the PCI bus. The buffer has a capacity of 256K total samples, and contains a 16-bit data field, a 1-bit tag field, and an END OF BURST status bit (Table 3.4-2). Analog input data is right-justified to the LSB, and occupies bit positions D00 through D15.

NOTE: The input buffer capacity of 256 K-Samples is distributed among all active input channels. The capacity in samples-per-channel is:

Sample Capacity per Channel = 256K / Number of active channels.

The channel tag identifies the first (lowest-numbered) active channel in each active channel-set. Reserved bits are always returned as zeros. The END OF BURST (EOB) status bit identifies the last data value in an input burst or function.

Table 3.4-2. Input Data Buffer

Offset: 0018h **Default: 00XX XXXXh**

DATA BIT	DESIGNATION	DESCRIPTION
D00	DATA00	Data value least significant bit (LSB)
D01-D14	DATA01 - DATA14	Data value intermediate bits
D15	DATA15	Data value most significant bit (MSB)
D16	FIRST-CHANNEL TAG	Tag assigned to first (lowest-numbered) active channel.
D17	END OF BURST (EOB)	Identifies the last input value in a burst.
D18-D31	(Reserved)	Always zero.

In order for the input buffer to acquire input data, the ENABLE INPUT BUFFER control bit must be set HIGH in the BCR. The buffer can be cleared, or emptied, by writing a "one" to the CLEAR INPUT BUFFER control bit in the BCR. The CLEAR INPUT BUFFER bit clears automatically. An empty buffer returns an indeterminate value.

The INPUT BUFFER OVERFLOW status bit in the BCR is set HIGH if the buffer overflows, thereby indicating data loss. The INPUT BUFFER UNDERFLOW bit is set HIGH if the buffer underflows (underruns), indicating that indeterminate data was acquired from an empty buffer. Each status bit remains HIGH until cleared, either directly from the bus, by the CLEAR INPUT BUFFER control bit, or by a board reset.

3.4.5.2 Buffer Size and Threshold Registers

The Input Buffer Size control register listed in Table 3.1-1 contains the total number of data values present in the input buffer. The Input Buffer Threshold register (Table 3.4-3) specifies the buffer size value above which the INPUT BUFFER THRESHOLD FLAG is asserted HIGH. The threshold flag is duplicated in the BCR.

Table 3.4-3. Input Buffer Threshold Register

Offset: 002Ch **Default: 0003 FFFEh**

BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00-D18	RW	INPUT BUFFER THRESHOLD	3 FFFEh	Specifies the number of values in the input buffer, above which the threshold flag is asserted HIGH.
D19	RO	INPUT BUFFER THRESHOLD FLAG [1]	0	HIGH when the number of values in the input buffer exceeds the specified buffer threshold.
D20-D31	RO	Reserved	0	---

1. Duplicated in the BCR.

3.5 Analog Input Buffer DMA Operation

DMA transfers from the analog input buffer are supported with the board operating as a bus master. Set Bit 02 in the PCI Command register HIGH to select the bus mastering mode. Refer to the PCI-9056 reference manual for a description of DMA configuration registers.

3.5.1 Block Mode

Table 3.5-1 illustrates a *typical* PCI register configuration that would control a non-chaining, non-incrementing ***block-mode*** DMA transfer in DMA Channel 00, in which a PCI interrupt is generated when the transfer has been completed. For most applications, the DMA Command Status Register would be initialized to 0000 0001h, and then changed to 0000 0003h to initiate a transfer.

Table 3.5-1. Typical Input DMA Register Configuration; Block Mode

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial (constant) local address	0000 0018h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

* Determined by specific transfer requirements.

3.5.2 Demand Mode

Demand mode transfers are controlled in a manner similar to block mode transfers, with the addition of ***demand-mode*** operation selected in the DMA mode register (D[12] = HIGH). Demand mode operation also requires the ***slow terminate*** mode (D[15] = LOW), which is the default state for this control bit. Table 3.5-2 shows a *typical* PCI register configuration for DMA Channel 00 demand mode operation.

Table 3.5-2. Typical Input DMA Register Configuration; Demand Mode

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32)	0002 1943h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial (constant) local address	0000 0018h
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

* Determined by specific transfer requirements.

NOTE: The PCI-9056 adapter extracts data from the 32-Bit (Lword) local bus in 64-Bit (quad-word) increments. Consequently, *if the buffer runs empty or nearly empty*, the situation can arise in which the last one or two samples in an active channel group are retained until subsequent data is acquired. If this occurs, the next sample set flushes the retained data through the PCI-9056 adapter to the PCI bus, and no samples are lost.

NOTE: The default analog input DMA channel for demand-mode operation is Channel 00. To operate in DMA Channel 01, set the SWAP DEMAND MODE CHANNELS control bit HIGH in the BCR and use the Channel 01 PCI registers.

3.6 Data Coding Formats

Analog input and output data is arranged as 16 active right-justified data bits with the coding conventions shown in Figure 3.6-1. The default format is offset binary. Two's complement format is selected by clearing the OFFSET BINARY control bit LOW in the BCR. Unless indicated otherwise, offset binary coding is assumed throughout this document.

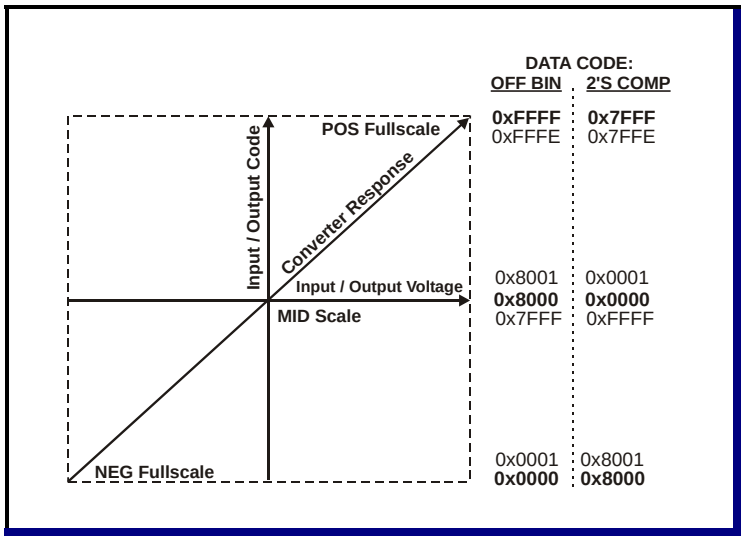

Figure 3.6-1. Analog Data Coding Formats; 16 Bit Data

3.7 Input Rate Generators

Two rate generators support data acquisition by providing the Rate-A ADC sample clock and a Rate-B timebase for triggering acquisition bursts.

3.7.1 Rate-A Generator

The Rate-A generator supplies an internal ADC clock source that supports ADC sample rates from 30 KSPS to 1000 KSPS. The generator frequency **Fgen-a** is adjustable from 9.6MHz to 19.2MHz, and is calculated as:

Fgen-a = (Fclk/2) * (Nvco / Nref),

where **Fclk** = Master clock frequency, and **Nvco** and **Nref** are integers between 30 and 1000, In general, the smallest values of **Nvco** and **Nref** that produce an acceptable value for **Fgen** should be used. Values above 250 may degrade the signal-to-noise ratio.

NOTE: Fclk has a standard value of 40.320MHz, but can have other optional values near this frequency. See Appendix-C for the effect of revised Fclk frequencies.

The frequency Fgen-a is one-half the actual PLL oscillator frequency, due to a final division by two to ensure a 50-percent duty cycle for the ADC clock. An external adc clock drives the ADC's directly and does not undergo this division. Consequently, the external adc clock must have a 50% +/-5% duty cycle.

The input sample rate **Fsamp** is derived from the generator frequency **Fgen** and an integer divisor **Ndiv-a** as:

Fsamp = Fgen-a / 16 for Fsamp > 600ksps (Ndiv = 0)

Fsamp = Fgen-a / (32 * Ndiv-a) for Fsamp = 30ksps to 600ksps.

where **Ndiv-a** has a valid range from 1-20. An **Ndiv-a** value of zero indicates that **Fsamp** is above 600KSPS.

Although the maximum value of Ndiv, i.e.: 20, apparently could produce a sample rate of 15KSPS with Fgen-a = 19.2MHz, sample rates below 30KSPS will produce unpredictable results. The extended range of Ndiv-a is provided only to improve the adjustment resolution of Fgen-a, and only sample rates of 30KSPS and higher should be implemented.

Table 3.7-1. Analog Input Sample Rate-A Generator Control Register

Offset: 001Ch **Default: 0103 F020h**

Bit Field	Mode	Designation	Default	Function
D[09..00]	R/W	VCO FACTOR **(Nvco)**	20h	PLL VCO factor; 30-1000.
D[11..10]	R/W	(Reserved)	0h	---
D[21..12]	R/W	REF FACTOR **(Nref)**	3Fh	PLL Reference factor; 30-1000.
D[23..22]	R/W	(Reserved)	0h	---
D[28..24]	R/W	Divisor **(Ndiv**)	01h	Ndiv (Zero for Fsamp >600KSPS, 1-20 for Fsamp = 30-600KSPS)
D[31..29]	R/W	(Reserved)	0h	---

Table 3.7-2. Sample Rate Fsamp Control Examples

Fclk (MHz)	Nvco [1]	Nref [1]	Fgen (MHz)	Ndiv	Fsamp (KSPS)
40.320	50	63	16.000	0	**1000**
	50	84	12.000	0	**750**
	40	42	9.600	0	**600**
	40	84	19.200	1	**600**
	32	63	10.240	1	**320**
	40	84	19.200	3	**200**
	40	42	9.600	3	**100**
	40	42	9.600	10	**30**
	40	84	19.200	20	**30**

1. Decimal values.

3.7.2 Rate-B Generator

The Rate-B generator output can be used as a trigger source for input burst acquisition, and is enabled by the associated ENABLE RATE-B GENERATOR control bit in the BCR. The Rate-B generator is disabled when this bit is LOW.

Table 3.7-3. Trigger Rate-B Generator Register

Offset: 0020h **Default: 0000 2760h)**

DATA BIT	MODE*	DESIGNATION	DEFAULT	DESCRIPTION
D00-D23	R/W	**Ndiv-b**	---	Rate generator frequency control
D24-D31	RO	(Inactive)	0	---

* R/W = Read/Write, RO = Read-Only.

The frequency **Fgen** (Table 3.7-2) of each generator is calculated as:

Fgen-b = Fclk / Ndiv-b,

where **Fclk** is the master clock frequency for the board, and **Ndiv-b** is the value written to the Rate-Generator register. **Fgen-b** and **Fclk** are both expressed in the same frequency units. For simplicity, **Fclk** is assumed here to be 40.320 MHz, but this is an ordering option and might have another value close to this frequency. The actual value for **Fclk** is identified in the Assembly Configuration register shown in Section 3.16.

Table 3.7-4. Rate-B Generator Frequency Selection

Ndiv-b		FREQUENCY Fgen-b (40.320 MHz Master Clock)*
(Dec)	(Hex)	(kHz)
40	0028	1008.00
41	0029	982.93
---	---	Fgen (Hz) = 40320 (kHz) / Ndiv-b

* ±0.003 percent.

3.8 Multiboard Synchronization

Analog input and output clocking and triggering can be synchronized among multiple boards by designating one of the boards as an ***initiator***, and the remaining boards as ***targets***. In order to implement this function, the boards must be connected together as described in Paragraph 2.3.4.

When multiple boards are configured as an initiator and multiple targets, the analog input clock, the analog input trigger, and the analog output clock generated in the initiator board are duplicated in the target boards with delays of less than 100 nanoseconds.

All boards default to the target mode, with the ANALOG INPUT CLK INITIATOR and TRIGGER INITIATOR control bits cleared LOW in the BCR. To designate a board as a clock or trigger initiator, set the associated control bit HIGH.

NOTE: To avoid contention among boards that are wired in an initiator/target configuration, ensure that all target boards have been designated before initiating clocking operations.

3.9 Digital I/O Port

The 16-Bit bidirectional digital I/O port consists of two independent data bytes, as shown in Table 3.9-1. Data fields DIO BYTE 00 and DIO BYTE 01 represent the 16 digital I/O pins in the system I/O connector. Logic polarities are retained, with a HIGH level at a connector pin associated with a HIGH level for the corresponding bit in the Digital I/O Port register.

Each data byte is an *input field* from the system I/O connector if the corresponding BYTE XX OUTPUT control bit is LOW, or is an *output field* to the connector if the control bit is HIGH. Both byte fields default to inputs.

Table 3.9-1. Digital I/O Port Register

Offset: 0004h **Default: 00XX 00XXh**

DATA BIT	MODE*	DESIGNATION	DEFAULT	DESCRIPTION
D00-D07	RW	DIO BYTE 00	XXh	System connector pins DIO 00 through DIO 07.
D08	RW	BYTE 00 OUTPUT	0	Direction control for DIO BYTE 00. When LOW, DIO BYTE 00 is an input field. When HIGH, DIO BYTE 00 is an output field.
D09-D15	RO	(Reserved)	0h	Read back as all-zero.
D16-D23	RW	DIO BYTE 01	XXh	System connector pins DIO 08 through DIO 15.
D24	RW	BYTE 01 OUTPUT	0	Direction control for DIO BYTE 01. When LOW, DIO BYTE 01 is an input field. When HIGH, DIO BYTE 01 is an output field.
D25-D31	RO	(Reserved)	0h	Read back as all-zero.

3.10 Autocalibration

To obtain maximum measurement accuracy, autocalibration should be performed after:

- Power warmup,
- PCI bus reset,
- Analog output range change.

The analog inputs are always calibrated on all input ranges during autocal, but to prevent damage to possibly low-voltage loads, the analog outputs are calibrated only on the selected output range.

Note: Analog outputs are active on the selected output range during autocalibration.

Autocalibration is invoked by setting the AUTOCAL control bit HIGH in the BCR. The control bit returns LOW automatically at the end of autocalibration. Autocalibration can be invoked at any time, and has a typical duration of less than 5 seconds. Completion of the operation can be detected either by monitoring the 'Autocal Completed' status flag in the primary status register (Table 3.11-1), or by simply waiting a sufficient amount of time to ensure that autocalibration has been completed.

To compensate for component aging and to minimize the effects of temperature on accuracy, the autocalibration function determines the optimum calibration values for current conditions, and stores the necessary correction values in internal volatile memory. If a board is defective, the autocalibration process may be unable to successfully calibrate the inputs. If this situation occurs, the AUTOCAL PASS status bit in the BCR is cleared LOW at the end of the autocalibration interval, and remains LOW until a subsequent initialization or autocalibration occurs. AUTOCAL PASS is initialized HIGH, and remains HIGH unless an autocalibration failure occurs.

3.11 Primary Status Register

Critical status flags are consolidated into a single Primary Status register (Table 3.11-1), which is organized into a selection field and a response field. A response status bit is asserted if the selected event occurs after it has been selected. The response bit remains high until it is cleared from the PCI bus, either by clearing the response bit, *or by clearing the associated selection bit*.

NOTE: Response status bits can *only* be cleared LOW from the PCI bus. A "one" written to a response bit is ignored.

A selected event is edge-detected on a transition of the event from false to true. Once asserted, a response bit remains in that state until cleared from the bus, regardless of subsequent changes in the associated event state.

Table 3.11-1 Primary Status Register

Offset 0x0030 **Default 0x0000 0000**

SELECTION BIT [1]	CRITICAL EVENT	RESPONSE BIT [2]	REFERENCE PARAGRAPH
D00	Autocal completed	D16	3.10
D01	Input Buffer threshold flag HIGH-to-LOW transition	D17	3.4.5.2
D02	Input Buffer threshold flag LOW-to-HIGH transition	D18	
D03	Input Buffer Overflow or Underflow	D19	3.4.5.1
D04	Analog Input Burst initiated (BURST BUSY LO-HI)	D20	3.4.4.2
D05	Analog Input Burst Completed (BURST BUSY HI-LO)	D21	
D06	Analog Input Clock	D22	3.4.4
D07	Analog Output Clock	D23	3.13.4
D08	Digital I/O Port DIO 00 LOW-to-HIGH transition	D24	3.9
D09	Output Buffer threshold flag HIGH-to-LOW transition	D25	3.13.2.3
D10	Output Buffer threshold flag LOW-to-HIGH transition	D26	
D11	Output Load-Ready Flag HIGH-to-LOW transition	D27	3.13.3.3
D12	Output Load-Ready Flag LOW-to-HIGH transition	D28	
D13	Analog Output Burst Ready	D29	3.13.5.2
D14	Output Buffer Overflow or Frame Overflow	D30	3.13.2.3 3.13.3.3
D15	(Reserved)	D31	---

1. Event selection. Enables assertion of the corresponding response bit when the selected event occurs.
2. Event response. Asserted HIGH when a selected event occurs. Remains HIGH until cleared LOW.

3.12 Registered Analog Outputs

If the ENABLE BUFFERED OUTPUTS control bit is LOW in the BCR, the analog outputs are controlled in Direct-Register mode through the four ANALOG OUTPUT CHAN xx registers listed in Table 3.1-1. If the control bit is HIGH, then the outputs are controlled in the Buffered Outputs mode through the output buffer described in Section 3.13.

Each analog output channel is controlled directly through the associated ANALOG OUTPUT CHAN xx register. The outputs are double-buffered, and can be clocked either independently or simultaneously. Output data is written to a 16-bit field that is right-justified in the data registers (Table 3.12-1).

Table 3.12-1. Analog Output Channel Data Register

Offset: 0008h - 0014h **Default: 0000 8000h**

DATA BIT	DESIGNATION	DESCRIPTION
D00	DATA00	Data value least significant data bit
D01-D14	DATA01 - DATA14	Data value intermediate data bits
D15	DATA15	Data value most significant data bit
D16-D31	(Reserved)	Data in this field is ignored.

3.12.1 Output Ranges

An output voltage range of ±10V, ±5V or ±2.5V is assigned by the OUTPUT RANGE control field in the BCR. The default output range is ±10V.

3.12.2 Clocking Modes

3.12.2.1 Immediate

When the SIMULTANEOUS OUTPUTS control bit is LOW in the BCR, each analog output channel is updated immediately when the associated data register receives a new value.

3.12.2.2 Simultaneous

When the SIMULTANEOUS OUTPUTS control bit is HIGH in the BCR, all analog outputs retain their existing values until an output clock occurs. An output clock updates all output channels simultaneously with the most recent data received by the data registers.

As is shown in Table 3.12-2, when operating in the simultaneous output clocking mode, an output clock is generated by:

- The OUTPUT S/W CLOCK control bit in the BCR, or:
- The internal Rate-C generator, or:
- An external clock input from the I/O connecter, or:
- The analog inputs.

Table 3.12-2 Simultaneous Output Clock Source Selection

		Output Clock Source				
Register	**Selection Control Bit**	**S/W Clock (BCR, BOR)**	**Rate-C Gen**	**External Input**	**Analog Inputs (Fsamp)**	**Analog Inputs (Acquis)**
BCR	SIMULTANEOUS OUTPUTS	HIGH	HIGH	HIGH	HIGH	HIGH
	ENABLE RATE-C GENERATOR	X	HIGH	X	X	X
BOR [1]	ANALOG OUTPUT CLK INITIATOR	X	HIGH	LOW	LOW	X
	SYNC AO WITH INPUTS	0	0	0	0	1h [2]
						2h [3]

1. Buffered Outputs Operations register (Table 3.13-2).
2. ADC sample rate Fsamp (Active whether or not input acquisition is disabled; for example between input bursts).
3. ADC acquisition rate (Only those samples that produce data in the input buffer).

To select the output clock ***Initiator*** mode, set ANALOG OUTPUT CLK INITIATOR **HIGH** in the Buffered Outputs Operations control register (Table 3.13-2). In this mode, the bidirectional OUTPUT CLK I/O pin in the system I/O connector is an output, and each output clock produces a 70-150 nanosecond LOW output pulse.

If ANALOG OUTPUT CLK INITIATOR is **LOW**, designating the board as an output clock ***Target***, the OUTPUT CLK I/O pin becomes an input, and an output clock is generated for each HIGH-to-LOW transition received at the pin. The Rate-C generator is ignored when operating in the target clocking mode, or if the analog input sampling or acquisition rate is selected for output clocking.

Clocking from the analog inputs synchronizes the output clocking rate to the analog inputs. The ADC's can be clocked without producing data in the input buffer, for example before a burst trigger if input bursting is enabled. For this reason, two control modes are provided with the SYNC AO WITH INPUTS control field in the BOR.

If the 'ADC sample rate' is selected (SYNC AO WITH INPUTS = 1), the outputs clock at the frequency of the selected analog inputs sample clock, whether or not input data is acquired.

If the 'ADC acquisition rate' is selected (SYNC AO WITH INPUTS = 2), a single output clock is generated for each ADC sample that produces data in the input buffer. For example, if input bursting is enabled while operating in this mode, the outputs will be clocked only during input bursts.

NOTE: The SYNC AO WITH INPUTS control field in the BOR is active in both direct (registered) output access and buffered output access (3.13).

3.13 Buffered Analog Output Control

If the ENABLE BUFFERED OUTPUTS control bit is set HIGH in the BCR, the analog outputs are controlled through the output buffer in the *Buffered Outputs* mode described in this section (3.13).

This section describes those operations that control the movement of data from the PCI bus through the analog output buffer. These functions include the selection of active channels, the organization of data within the buffer, and the clocking of data from the buffer to the analog outputs. The principal parameters associated with controlling the analog output channels are summarized below in Table 3.13-1.

Table 3.13-1. Summary of Output Control Parameters

Parameter	Mode	Description
Data Control	Active Channels; **Channel Group**	A single set of all active output channels constitutes an ***Active Channel Group***. Active channels are selected under a channel mask.
	Data Frame	All data values in the buffer comprise a *Data Fr*ame.
	Data Coding	Output data can be coded either in offset-binary format or in two's complement format.
Buffer Configuration	Open	Data read from the buffer is used and then discarded, until the buffer is empty.
	Circular (closed)	Data within the buffer is recirculated. Each value read from the output of the buffer FIFO is written back to the input of the FIFO. An end-of-frame (EOF) flag tracks the movement of data through the buffer.
Clock Source	External	External hardware provides the sample clock.
	Internal	The sample clock is provided by an internal rate generator, at a rate determined by the sample rate control register.
Clocking Mode	Simultaneous	At each clock occurrence, the next channel group (i.e.: a single group of all active channel values) in the output buffer is transferred to the respective analog output channels. All outputs are updated simultaneously.
	Sequential	At each clock occurrence, the next active channel value in the output buffer is transferred to the associated analog output channel, which is updated immediately.
Sampling Mode	Continuous	The contents of the output buffer are sampled continuously at the selected clock rate.
	Triggered Burst	A single data frame in the buffer is clocked to the outputs.

3.13.1 Data Organization

3.13.1.1 Active Channels

Analog output data is loaded into the output buffer in discrete groups or frames of channel data. An active *channel group* consists of a single set of output values for all active channels.

Only active output channels receive data from the output buffer. A channel that is deselected to the inactive state retains the last value that was received while the channel was still active. During initialization, all channels are designated as active and are set to midrange (zero output level).

3.13.1.1.1 Selection

An output channel is selected as *active* by setting the corresponding AO CHANNEL-xx-ACTIVE selection bit HIGH in the Buffered Output Operations register shown in Table 3.13-2. A channel is deselected to the *inactive* state by clearing the corresponding selection bit.

3.13.1.1.2 Loading

Channel data values are loaded into the output buffer in ascending order of active channels. The channel groups are loaded contiguously, beginning with the first group to be transferred to the outputs, and proceeding sequentially to the last group. Figure 3.13-1 illustrates a loading example that represents three active channels, with 100 values per channel. Each channel group consists of active channels 0, 1 and 3.

NOTE: Data can be loaded from the PCI bus to the output buffer only if the buffer is open; that is, not circular or closed (3.13.2.4).

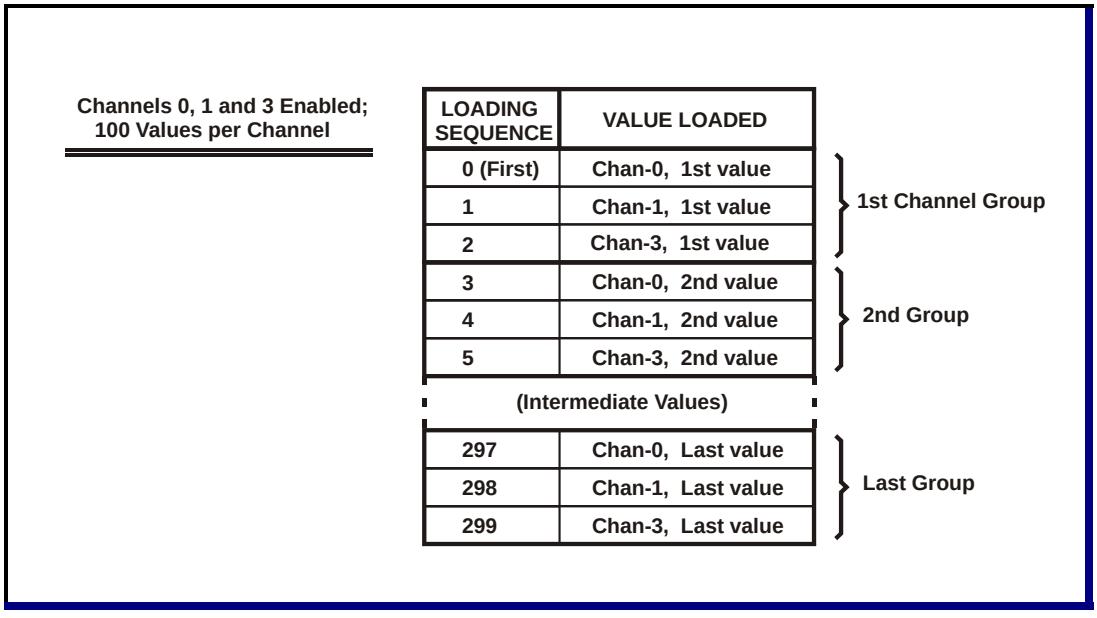

Figure 3.13-1. Typical Buffer Loading Sequence

Table 3.13-2. Buffered Output Operations Register

Offset: 003Ch **Default: 0000_104Fh**

BIT	MODE	DESIGNATION	DEF	DESCRIPTION	REF
D00	R/W	AO CHAN 00 ACTIVE	1	Active-channel mask for analog output channels. HIGH => Active; LOW => Inactive.	3.13.1.1
D01	R/W	AO CHAN 01 ACTIVE	1		
D02	R/W	AO CHAN 02 ACTIVE	1		
D03	R/W	AO CHAN 03 ACTIVE	1		
D04	R/W	ANALOG OUTPUT CLK INITIATOR	0	Selects the internal Rate-C generator for output clocking if HIGH, or the Output Clock I/O hardware input if LOW. Ignored if 'SYNC AO WITH INPUTS' is nonzero.	3.13.4.1
D05	R/W	ENABLE OUTPUT CLOCKING	0	Enables output clocking when HIGH. Disables clocking when LOW. Default is LOW (clocking disabled).	3.13.4
D06	RO	OUTPUT CLOCK READY	1	Indicates when HIGH that an output clock will be accepted. If LOW, indicates that the output will not respond to a clock.	3.13.4
D07	R/W	OUTPUT SW CLOCK [1, 3]	0	Produces a single output clock event when asserted. Independent of clocking mode. Duplicated in the BCR.	3.13.4.1
D08	R/W	CIRCULAR BUFFER	0	Selects circular buffer configuration if HIGH, or open self-flushing buffer configuration if LOW. Access for loading new data into the circular buffer must be requested by asserting LOAD REQUEST. Default is LOW; i.e. open buffer.	3.13.2.5
D09	R/W	LOAD REQUEST [1]	0	When set HIGH, requests loading access to the circular buffer. Initializes LOW.	3.13.3.3
D10	RO	LOAD READY	0	Set HIGH when the frame index passes through zero, if both CIRCULAR BUFFER and LOAD REQUEST are HIGH. When HIGH, indicates that the circular buffer is ready to accept new data. Available also in the PSR. Defaults HIGH.	3.13.3.3
D11	R/W	CLEAR OUTPUT BUFFER [1]	0	Resets the output buffer to empty.	3.13.2.3
D12	RO	AO BUFFER EMPTY	1	Indicates the analog output buffer is empty.	3.13.2.3
D13	RO	AO BUFFER THRESHOLD	0	Analog output buffer threshold flag. Duplicated in the AO Buffer Threshold register.	3.13.2.3
D14	RO	(Reserved)	0	Inactive; Returns zero.	---
D15	RO	AO BUFFER FULL	0	Indicates the output buffer is full.	3.13.2.3
D16	R/W	AO BUFFER OVERFLOW [2]	0	Set HIGH when data is written to a full buffer	3.13.2.3
D17	R/W	FRAME OVERFLOW [2]	0	Set HIGH when data is written to a closed buffer.	3.13.3.3
D18	RO	BURST READY	0	If HIGH, indicates that a burst trigger will be accepted. If LOW, indicates that the output will not respond to a trigger.	3.13.5.2
D19	R/W	ENABLE OUTPUT BURST	0	Enables analog output burst operation.	3.13.5.1
D20	R/W	OUTPUT SW TRIGGER [1]	0	Produces a single output trigger event when asserted. Clears LOW automatically when the clock event is completed. Independent of triggering mode. Duplicated in the BCR.	3.13.5.2
D21-D22	R/W	SYNC AO WITH INPUTS	0h	Analog input mode: 0 => Independent outputs clocking. 1 => Output clocking rate equals ADC sample rate. 2 => Output clocking rate equals ADC acquisition rate. 3 => (Reserved)	3.12.2.2
D23-D31	RO	(Reserved)	0	Inactive. Returns all-zero.	---

1. Clears LOW automatically when operation is completed.
2 Remains HIGH until cleared by a direct write as LOW, or by initialization.
3 May invoke immediate mode output clocking in some systems. Duplicated in the BCR.

3.13.1.2 Data Frame

A *data frame* consists of an integral number of channel groups.

For triggered bursts, or for function concatenation, the last active channel in the last channel group is designated as the *end-of-frame* (EOF). The EOF designation is applied by setting the EOF flag (D16) HIGH when loading the last channel value into the buffer. Thereafter, the EOF flag follows the last channel value through the buffer.

3.13.1.3 Voltage Range Selection

An output voltage range of ±10V, ±5V or ±2.5V is assigned by the OUTPUT RANGE control field in the BCR. The default output range is ±10V.

For maximum accuracy, autocalibration should be performed after a new input or output range is selected.

3.13.2 Output Buffer

Analog output data from the PCI bus is first corrected for offset and gain errors, and then flows directly into the 256K-sample analog output FIFO data buffer (Table 3.13.1). From the buffer, the corrected data is routed to the analog output DAC channels.

NOTE: The output buffer capacity of 256 K-Samples is distributed among all active output channels. The capacity in samples-per-channel is:

Sample Capacity per Channel = 256K / Number of active channels.

3.13.2.1 Output Data Format

Analog output data values are written in Lword-serial sequence from the PCI bus to the Analog Output Buffer register shown in Table 3.13-3. Bits D15..0 represent the output data value. Bit D16 is set HIGH to indicate the last value in a data frame, and is the end-of-frame (EOF) flag. Bits D31..17 are inactive. Access to the output buffer is supported for both single-longword transfers and single-address multiple-longword DMA transfers. The output buffer appears to the PCI bus as a single register, and a read-access to this register returns an all-zero value.

Table 3.13-3. Analog Output Buffer

Offset: 0048h **Default: N/A (Write-Only)**

BIT	MODE*	DESIGNATION	DESCRIPTION
D00	WO	DATA 00	Least significant data bit
D01-D14	WO	DATA 01 - DATA 14	Intermediate data bits
D15	WO	DATA 15	Most significant data bit
D16	WO	EOF FLAG	End-of-frame (EOF) flag.
D17-D31	WO	---	(Inactive)

* WO indicates write-only access. Read-access returns all-zero value.

3.13.2.2 Output Data Coding

Analog output data coding is described in Paragraph 3.6.

3.13.2.3 Output Buffer Control

The Buffered Output Operations register in Table 3.13-2 controls and monitors the flow of data through the analog output data buffer. Asserting the CLEAR OUTPUT BUFFER control bit HIGH clears, or empties, the buffer.

The AO BUFFER OVERFLOW flag is set HIGH if data is written to a full buffer, and the FRAME OVERFLOW flag indicates that an attempt was made to write data to a closed buffer. Both flags indicate data loss. Once set, each of these flags remains HIGH until written LOW directly from the bus, or by initialization .

The AO BUFFER EMPTY flag indicates that the buffer contains no output data. The AO BUFFER FULL flag is asserted when the buffer is full. Data written to a full output buffer is discarded.

The Output Buffer Size register shown in Table 3.13-4 contains the number of output data values present in the buffer, and is updated continuously.

Table 3.13-4. Output Buffer Size Register

Offset: 0044h **Default: 0000 0000h**

DATA BIT	MODE*	DESIGNATION	DEF	DESCRIPTION
D00-D18	RO	BUFFER SIZE	0 0000h	Number of values in the output buffer
D19-D31	RO	(Inactive)	0	---

The Output Buffer Threshold register in Table 3.13-5 specifies the buffer size value above which the OUTPUT BUFFER THRESHOLD FLAG is asserted HIGH.

Table 3.13-5. Output Buffer Threshold Register

Offset: 0040h **Default: 0003 FFFEh**

BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00-D18	RW	OUTPUT BUFFER THRESHOLD	3 FFFEh	Specifies the number of values in the output buffer, above which the threshold flag is asserted HIGH.
D19	RO	OUTPUT BUFFER THRESHOLD FLAG	0	HIGH when the number of values in the output buffer *exceeds* the specified buffer threshold.
D20-D31	RO	Reserved	0	---

3.13.2.4 Open Buffer

If the CIRCULAR BUFFER control bit is LOW in the buffer operations register (Table 3.13-2), the output buffer operates in the open mode. Data in an open buffer is discarded as it is used. Consequently, the buffer is self-flushing, and will empty itself unless it is replenished from the PCI bus. This mode of operation permits the continuous flow of data from the PCI bus to the analog outputs.

The open-buffer configuration also can be used to produce a one-shot waveform, provided the particular waveform is to be used only once. Figure 3.13-2 illustrates the movement of a single data frame through an open buffer.

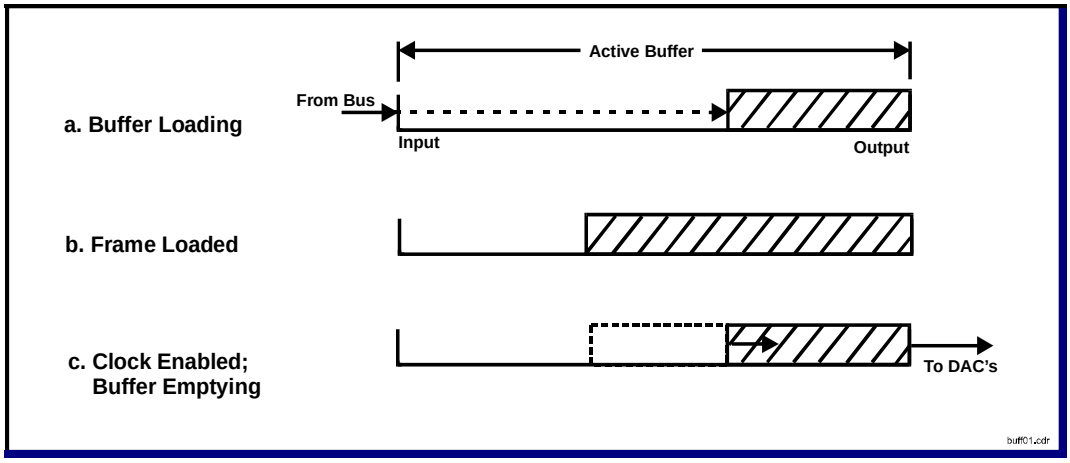

Figure 3.13-2. Open Buffer Data Flow

3.13.2.5 Circular Buffer

Data in a circular (closed) buffer is retained indefinitely. This configuration generally is implemented to produce either periodic waveforms of constant frequency, or one-shot transient waveforms that will be used repeatedly but not necessarily periodically. While closed, the buffer is not accessible from the PCI bus.

In Figure 3.13-3 a single data frame is loaded into the buffer. The buffer is then closed (CIRCULAR BUFFER set HIGH) and clocking is enabled. The data frame subsequently circulates in the buffer while passing data values to the output channels.

An end-of-frame (EOF) flag accompanies the end-point, or last value in a data frame. The EOF flag is D16 in the buffer, and is set HIGH when the last value in a data frame is loaded. This flag is used at the end of a function or triggered burst to define the last value. Multiple contiguous burst functions, or frames, can reside in the buffer simultaneously.

NOTE: Disable output clocking before loading the output buffer for circular operation.

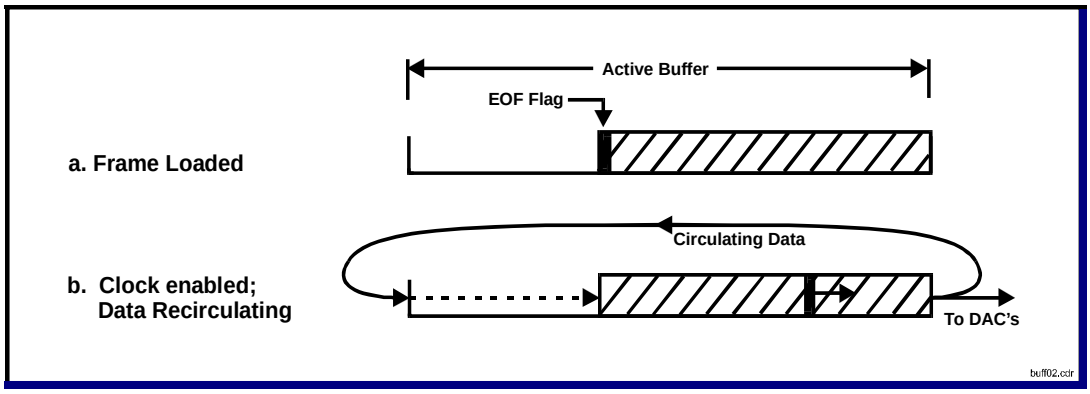

Figure 3.13-3. Circular Buffer Data Flow

3.13.3 Function Generation

3.13.3.1 Periodic and One-Shot Functions

Periodic waveforms are produced when the buffer is configured for continuous sampling and circular operation. In this mode, the contents of the buffer are scanned continuously as long as clocking is enabled and a clock is present. The data frame is recirculated through the buffer repeatedly. Clocking is enabled when the ENABLE OUTPUT CLOCKING control bit in the buffer operations register is HIGH.

If triggered-burst sampling is used in conjunction with a circular buffer, a *one-shot waveform* is produced that contains all values within a single data frame. The triggered burst is initiated by a software or hardware trigger, and terminates automatically when the end-of-frame (EOF) flag is encountered. Because the buffer is circular, the waveform is retained in the buffer and can be reproduced repeatedly by subsequent triggers.

3.13.3.2 Multiple Functions

When multiple functions are loaded into the buffer as contiguous data frames, and if triggered-burst sampling is selected, the functions will be generated sequentially in response to a series of burst triggers. If the buffer is open, the functions are flushed from the buffer as they are clocked to the analog outputs. However, if the buffer is closed (circular), the functions are retained in the buffer, and the series of functions is repeated indefinitely. .

3.13.3.3 Function Sequencing (Concatenation)

A new function can be concatenated to the end of an existing function in a circular buffer, while the existing function is being flushed from the buffer. During this operation, the existing function is flushed from the buffer as it is clocked to the outputs, and is replaced by the new function. When the last value of the existing function is clocked out of the buffer, the buffer closes and the new function seamlessly begins circulating in the buffer and producing an output.

Introduction of a new function commences by setting the LOAD REQUEST flag HIGH in the buffered output operations register (Table 3.13-2), and by then waiting for the LOAD READY flag to be asserted. (In effect, LOAD REQUEST is an "interrupt request" to the buffer). The LOAD READY flag indicates that the buffer has opened, and that the existing function is being flushed from the buffer, beginning with the first value in the function's data frame.

After LOAD READY goes HIGH, the new function is written to the buffer and is terminated with an EOF flag (output data bit D16 set HIGH). The EOF flag of the existing function causes the buffer to close, and clears both the LOAD READY flag and the LOAD REQUEST control bit. Notice that the loading of the new function into the buffer must be completed before the existing function terminates.

In Figure 3.13-4, an existing function is replaced by a new function while the existing ('old') function is flushed from the buffer.

NOTE: If the loading of a new function extends beyond the LOAD-READY interval, the FRAME OVERFLOW flag is set HIGH in the Buffer Operations register, indicating data loss. Once set, this flag remains HIGH until written LOW directly from the bus, or by initialization

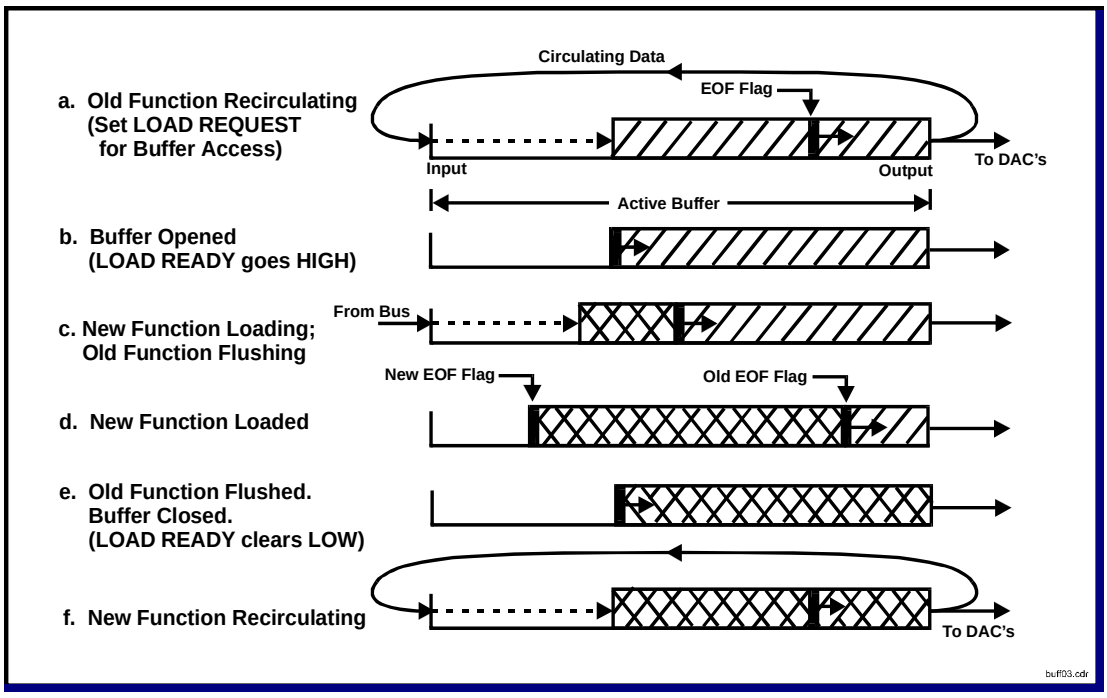

Figure 3.13-4. Function Sequencing

3.13.4 Output Clocking

If the ENABLE OUTPUT CLOCKING control bit in the buffer operations register is asserted HIGH, clocking is enabled and the active analog outputs are updated at each occurrence of the sample clock. The sample clock can be generated internally by the rate generator, or can be supplied externally through the I/O connector. Output clocking is disabled when the ENABLE OUTPUT CLOCKING control bit is LOW. The OUTPUT CLOCK READY flag indicates that data is available to be clocked to the output channels .

Hardware output signal OUTPUT CLK I/O (Table 2.2-1) goes LOW momentarily each time a sample clock occurs, Connecting this signal to the OUTPUT CLK I/O pins of other boards permits synchronous clocking of multiple boards.

3.13.4.1 Clock Source

When buffer operations register bit ANALOG OUTPUT CLK INITIATOR is LOW, the output clock is supplied externally through the I/O connector as OUTPUT CLK I/O. If the control bit is HIGH, the output clock is derived from the internal Rate-C generator. An output clock can also be supplied at any time by asserting the OUTPUT SW CLOCK control bit, which clears automatically. See also Paragraph 3.12.2.2 for the application of the SYNC AO WITH INPUTS control field in synchronizing the analog output clock with analog input sampling.

3.13.4.1.1 External Clock

The external clock source can have any frequency up to the maximum value specified for the sampling rate. When the external clock source is selected, sampling occurs on a HIGH-to-LOW transition of the OUTPUT CLK I/O pin in the I/O connector.

3.13.4.1.2 Internal Output Rate Generator

The internal Rate-C generator provides a sample clock that is adjustable by the RATE[23..0] control bits in the Output Sample Rate control register shown in Table 3.13-6. The Rate-C generator is enabled by setting the ENABLE RATE-C GENERATOR control bit HIGH in the BCR.

Table 3.13-6. Output Sample Rate Control Register (Rate-C)

Offset: 004Ch **Default: 0000_007Eh**

DATA BIT	MODE	DESIGNATION	DESCRIPTION
D00	R/W	RATE 00	Least significant rate bit
D01-D22	R/W	RATE 01 - RATE 22	Intermediate rate bits
D23	R/W	RATE 23	Most significant rate bit
D24-D31	RO	---	Inactive. Returns all-zero.

The output clocking rate **Fclock** is calculated from the relationship:

Fclock (Hz) = Fclk / Ndiv-c ,

where **Ndiv-c** is the decimal equivalent of the value in the RATE value in the Sample Rate control register, and **Fclk** is the master clock frequency for the board. For simplicity, **Fclk** is assumed here to be 40.320 MHz, but is an ordering option and can have any value close to this frequency. The actual value for **Fclk** is identified in the Assembly Configuration register shown in Section 3.16.

Table 3.13-7 illustrates the effect of **Ndiv-c** on the sample rate. Clocking rates above **1030 KSPS** can produce unpredictable results and are not recommended. **Ndiv-c** should not be modified during function generation.

Table 3.13-7. Output Sample Rate Selection

Ndiv-c		FREQUENCY Fgen (40.320 MHz Master Clock)*
(Dec)	(Hex)	(kHz)
40	0028	1008.00
41	0029	982.93
---	---	Fgen (Hz) = 40320 (kHz) / Ndiv-c

* ±0.003 percent.

3.13.4.2 Simultaneous Clocking

Simultaneous sampling is selected by setting the SIMULTANEOUS OUTPUTS control bit in the board control register HIGH. If simultaneous sampling is selected, the analog values in each successive channel group appear simultaneously at the outputs, with minimum time-skew between channels. Upon each occurrence of the sampling clock, an entire active channel group is transferred from the output buffer, and all outputs are updated simultaneously. In this mode, the effective sample rate for each channel equals the output clocking rate **Fclock**.

3.13.4.3 Sequential Operation

Sequential sampling is selected when the SIMULTANEOUS OUTPUTS control bit in the board control register is LOW. At each clock occurrence in sequential operation, a single channel value is transferred from the buffer to the associated output channel, and the channel is updated immediately. Channel values are read from the buffer beginning with the lowest-numbered active channel in a channel group, and proceeding upward through the highest-numbered active channel. When operating in this mode, the effective sample rate for each channel equals the output clocking rate **Fclock** divided by the number of active channels.

3.13.5 Sampling Mode

3.13.5.1 Continuous Sampling

If the ENABLE OUTPUT BURST control bit in the Buffered Output Operations register is LOW (default), the *continuous sampling* mode is selected and data is transferred continuously from the buffer to the analog outputs, assuming that the buffer is not empty and that an output clock is present.

3.13.5.2 Data Bursts

If the ENABLE OUTPUT BURST control bit in the Buffered Output Operations register is HIGH, burst operation is selected. During a *triggered output burs*t, data is transferred continuously from the output buffer to the analog outputs until either the ***buffer goes empty, or the end-of-frame (EOF) flag is encountered***. In the triggered-burst sampling mode, an internal or external output trigger initiates the transfer of data from the output buffer to the output channels.

If the TRIGGER INITIATOR control bit in the BCR is HIGH, *internal triggering* is selected, and either a software or hardware trigger will initiate a burst. A software trigger is generated by setting the OUTPUT S/W TRIGGER control bit HIGH, and a hardware trigger is provided by the

Rate-B generator, if enabled. These trigger sources are independent of each other, and the occurrence of either or both will initiate a burst. The OUTPUT SW TRIGGER bit remains HIGH during the burst, and clears automatically when the burst is completed.

In the initiator mode, hardware output pin TRIGGER I/O produces a LOW pulse at the beginning of each burst. Connecting this signal to the TRIGGER I/O pins of other boards permits synchronous burst triggering of multiple boards.

If the TRIGGER INITIATOR control bit is LOW in the BCR, indicating *Target Mode or External triggering*, a hardware burst trigger occurs upon a HIGH-to-LOW transition of the TRIGGER I/O pin in the I/O connector, *if* the ENABLE OUTPUT BURST control bit in the operations register is HIGH, *and* if the BURST READY flag also is HIGH. The BURST READY flag is LOW during a burst, and is HIGH if no burst is in progress. The OUTPUT S/W TRIGGER control bit also is active in the target mode.

Multiple burst functions can exist simultaneously within the buffer if the end-of-frame (EOF) flag is used (Paragraph 3.13.2.1). The EOF flag defines the last output value in each data burst. After a burst is triggered, data values from the buffer are clocked to the analog outputs at the selected sample rate until the EOF flag is encountered. The burst then terminates, and clocking of the buffer ceases until a subsequent trigger occurs.

Refer also to the Trigger Initiator note in 3.4.4.2.

3.13.6 Multiboard Synchronization

Boards that are configured for *synchronous clocking* update their outputs simultaneously in response to a common *clock* signal. Boards that are configured for *synchronous burst triggering* initiate data bursts simultaneously in response to a common *trigger* signal. Multiple boards can be arranged to operate with:

a. Independent clocking and burst triggering
b. Synchronous burst triggering (Common burst trigger)
c. Synchronous clocking (Common DAC clock)
d. Synchronous clocking and burst triggering (Common trigger and DAC clock).

As many as four boards can be synchronized together. External clock and trigger I/O signaling uses standard TTL levels.

3.13.6.1 Synchronous Bursts

To ***burst-synchronize*** a group of boards, the TRIGGER I/O signal from one board, the *burst-initiator*, is connected to the TRIGGER I/O pins of a group *of burst-target* boards. Each burst-target, when operated in the triggered-burst mode, initiates a single burst from its buffer each time the burst-initiator initiates a burst.

3.13.6.2 Synchronous Clocking

To ***clock-synchronize*** multiple boards together, the OUTPUT CLK I/O from one board, designated the *clock-initiator*, is connected to the OUTPUT CLK I/O pin of one or *more clock-target* boards. In this case, the clock-targets are configured for external clocking (ANALOG OUTPUT CLK INITIATOR cleared LOW in the operations control register), and the initiator is configured for internal clocking.

3.14 Buffered Analog Output Application Examples

NOTE: This section provides examples of operation in the Buffered Outputs mode, and assumes that the ENABLE BUFFERED OUTPUTS control bit is set HIGH in the BCR.

Specific operating modes and procedures vary widely according to the unique requirements of each application. The examples presented in this section (Table 3.14-1) illustrate several basic operating modes, and can be modified or combined for more complex operations.

References to *functions* in these examples generally apply to a single output channel for simplicity of explanation. However, each active channel represents an independent set of function values, and all channels share a common output clock.

Table 3.14-1. Summary of Operation Examples

Operation Example	Description
Sequential Direct Outputs	Each value written to the output data buffer updates the associated analog output channel when clocked, independently of the other channels.
Simultaneous Direct Outputs	Data values accumulate in the output data buffer until an entire channel group has been loaded. When the last channel is loaded, all active output channels update simultaneously when clocked.
Continuous Function	An extension of Simultaneous Direct Outputs, in which the buffer is not allowed to become either empty or full.
Periodic Function	A single function is generated repeatedly in each active channel.
Function Burst	One or more functions are generated as discrete data bursts. The burst cycle is repeated indefinitely if the circular-buffer mode is selected.
Function Sequencing	An existing active function is replaced seamlessly by a new function.

Each of the examples in this section assumes that the initial operations listed in Table 3.14-2 have already been performed.

Table 3.14-2. Initial Operations

Operation	Default Value	Applicable Paragraph
The board has been reset or initialized.	---	3.3.2
The active channel group has been defined .	All channels active	3.13.1.1
The required output coding has been selected.	Offset binary	3.6

The remaining operational parameters are assumed to be in the following *default* states initially:

Parameter	Default
Buffer mode:	Open
Buffer status:	Empty
Clock source:	External (Buffer Operations register)
Clock status:	Disabled (Buffer Operations register)

Parameter	Default
Sample rate:	320KSPS
Sampling mode:	Sequential

3.14.1 Sequential Direct Outputs

Table 3.14-3. Sequential Direct Outputs Example

Operation	PCI Bus Action	Board Response
Select Internal Clocking	Set the ANALOG OUTPUT CLK INITIATOR control bit HIGH in the buffer operations register.	The internal Rate-C generator is selected as the output clocking source.
Enable clocking	Set the ENABLE OUTPUT CLOCKING control bit HIGH in the buffer operations register. Set the ENABLE RATE-C GENERATOR control bit HIGH in the BCR.	Clocking is enabled at the default rate.
Load the output value for the first active channel.	Write the first value to the output data buffer.	Output value appears immediately (when clocked) at the analog output.
Load the output values for the remaining active channels.	Write the remaining active channel values to the output data buffer.	Remaining active analog outputs are updated in ascending sequence.
Repeat the above operations for subsequent channel groups.	Continue to write output values to the output data buffer.	Each value written to the buffer is transferred immediately to the associated analog output when clocked

Notes:
1. End-of-frame (EOF) flags are ignored when operating in the open-buffer mode. Only D15..0 are active in the output buffer.
2. Data written to the buffer at rates above 1000KSPS will accumulate in the buffer.
3. Access to an individual output channel is accomplished by first selecting (enabling) only the specific channel, and by then writing the output value to the buffer.

3.14.2 Simultaneous Direct Outputs

Table 3.14-4. Simultaneous Direct (Single Group) Outputs Example

Operation	PCI Bus Action	Board Response
Select simultaneous clocking.	Set SIMULTANEOUS OUTPUTS in the BCR.	Simultaneous clocking is selected.
Select Internal Clocking	Set the ANALOG OUTPUT CLK INITIATOR control bit HIGH in the buffer operations register.	The internal Rate-C generator is selected as the output clocking source.
Enable clocking	Set the ENABLE OUTPUT CLOCKING control bit HIGH in the buffer operations register. Set the ENABLE RATE-C GENERATOR control bit HIGH in the BCR.	Clocking is enabled at the default rate.
Clear the output buffer.	Set the CLEAR OUT BUFFER bit in the output operations register.	The output buffer clears to empty.
Load the output value for the first active channel.	Write the first value to the output data buffer.	First value is retained in the buffer.
Load the output values for the remaining active channels.	Write the remaining active channel values to the output data buffer.	Remaining values are accumulated in the buffer. When the last value is loaded, all values are extracted from the buffer and appear simultaneously at the associated output channels.
Repeat the above operations for subsequent channel groups.	Continue to write output values to the output data buffer.	All active channels are updated simultaneously when the last value in each group is written to the buffer.

Notes: 1. Data written to the buffer at rates above 1000KSPS will accumulate in the buffer.

3.14.3 Continuous Function

Table 3.14-5. Continuous Function Example

Operation	PCI Bus Action	Board Response
Select simultaneous clocking.	Set SIMULTANEOUS OUTPUTS in the board control register.	Simultaneous clocking is selected.
Set the buffer threshold flag to 1/4 of the expected block size.	Write 1/4 block size to the threshold register (Table 3.13-5).	The threshold flag will go LOW when the buffer contents drop below the threshold.
If the internal rate generator is to be used, select the sample rate. (Skip this step if external clocking will be used).	Write the required sample clocking rate to the Rate-C generator control register.	The frequency of the internal rate generator is selected, if internal clocking is required.
If internal clocking is required, select internal clocking.	To select internal clocking, set the ANALOG OUTPUT CLK INITIATOR bit HIGH in the buffer operations register.	Internal clocking is selected, if required.
Enable clocking	Set the ENABLE OUTPUT CLOCKING control bit HIGH in the buffer operations register. Set the ENABLE RATE-C GENERATOR control bit HIGH in the BCR.	Clocking is enabled at the selected rate. The internal rate generator is enabled, if internal clocking is required.
Clear the output buffer.	Set the CLEAR OUT BUFFER bit in the output operations register.	The output buffer clears to empty.
Write a block of values to all active channels. To avoid discontinuities in the output functions, the effective loading rate for channel groups must be greater than the sample (clocking) rate times the number of active channels. Maximum loading rate is 40MSPS during DMA transfers.	Write function values for all active channels to the output data buffer.	All active channels produce their respective output functions.
Wait for the buffer threshold flag to go LOW. (See Note 1).	Monitor the analog output buffer threshold flag until LOW.	The output buffer empties to less than 1/4-full status.
Repeat the previous two steps to sustain function generation.		All output functions proceed continuously.

Notes:
1. Response to the flag must be fast enough to prevent the buffer from going empty.

3.14.4 Periodic Function

Table 3.14-6. Periodic Function Example

Operation	PCI Bus Action	Board Response
Select simultaneous clocking.	Set SIMULTANEOUS OUTPUTS in the board control register.	Simultaneous clocking is selected.
Clear the output buffer.	Set the CLEAR OUTPUT BUFFER bit in the output operations register.	The output buffer clears to empty.
Load the first function value for each active channel.	Write the values for the first active group to the output data buffer.	Initial values for all active channels accumulate in the buffer.
Load the remaining function values for all active channels. (Note 1) Set the end-of-frame (EOF) flag.	Write all remaining function values for all active channels to the output buffer. Set the EOF flag (D16 in the output buffer) HIGH when writing the data value for the last channel in the last group.	Remaining function values for all active channels accumulate in the buffer. The EOF flag is set HIGH in the buffer location that contains the last channel value in the last channel group.
If the internal rate generator is to be used, select the sample rate. (Skip this step if external clocking will be used).	Write the required sample clocking rate to the Rate-C generator control register.	The frequency of the internal rate generator is selected, if internal clocking is required.
Note: The remaining operations may be performed simultaneously with a single write-transaction to the buffer operations register:	---	---
Select the circular buffer mode.	Set CIRCULAR BUFFER in the buffer operations register.	The output buffer is closed (circular).
If the internal rate generator is to be used, select internal clocking.	To select internal clocking, set the ANALOG OUTPUT CLK INITIATOR bit HIGH in the buffer operations register.	The internal Rate-C generator is selected, if required.
Enable the sample clock.	Set ENABLE OUTPUT CLOCKING in the buffer operations register. Set the ENABLE RATE-C GENERATOR control bit HIGH in the BCR.	Clocking is enabled. All active channels produce their respective functions repeatedly until the clock is disabled or the operating mode is changed. All outputs update simultaneously at the sample clock rate.

Notes:

1. To generate periodic functions simultaneously in multiple channels, all functions must be commensurate. That is, the functions in all channels must have frequencies that are exact integer multiples of the frequency of the lowest-frequency channel. Conversely, the period of the lowest-frequency channel must be an exact integer multiple of the period of each of the other channels.

3.14.5 Function Burst

Table 3.14-7. Function Burst Example

Operation	PCI Bus Action	Board Response
Select simultaneous clocking.	Set SIMULTANEOUS OUTPUTS in the board control register.	Simultaneous clocking is selected.
Clear the output buffer.	Set the CLEAR OUT BUFFER bit in the output operations register.	The output buffer clears to empty.
Load the first function value for each active channel.	Write the values for the first active group to the output data buffer.	Initial values for all active channels accumulate in the buffer.
Load the remaining function values for all active channels. Set the end-of-frame (EOF) flag.	Write all remaining function values for all active channels to the output buffer. Set the EOF flag (D16 in the output buffer) HIGH when writing the data value for the last channel in the last group.	All function values for all active channels accumulate in the buffer. The EOF flag is set HIGH in the buffer location that contains the last channel value in the last channel group.
If more than one burst-function is required, repeat the previous operations for each additional function.	---	If required, additional burst functions accumulate in the output buffer.
Select the trigger source.	For internal triggering, set the TRIGGER INITIATOR bit HIGH in the BCR. For external triggering, clear the bit LOW (default).	The frequency of the internal rate generator is selected, if internal clocking is required.
If the internal rate generator is to be used for ***clocking***, select the clocking rate.	Write the required clocking rate to the Rate-C generator control register.	The frequency of the internal rate generator is selected, if internal clocking is required.
If the internal rate generator is to be used for ***triggering***, select the triggering rate.	Write the required triggering rate to the Rate-B generator control register.	The frequency of the internal rate generator is selected, if internal triggering is required.
Select triggered-burst mode.	Set ENABLE OUTPUT BURST in the buffer operations register.	The triggered-burst operating mode is selected.
Prepare the buffer operations register for burst mode:	Write to the buffer operations register:	---
If the burst functions will be used repeatedly, select the circular buffer mode.	To select the circular buffer mode, set CIRCULAR BUFFER.	If required, the output buffer is closed (circular), and all functions will be retained in the buffer indefinitely.
If internal clocking is required, select internal clocking.	To select internal clocking, set ANALOG OUTPUT CLK INITIATOR.	Internal clocking is selected, if required.
Enable the sample clock.	Set ENABLE OUTPUT CLOCKING.	Output clocking is enabled.
Enable the internal rate generators, if required.	Set the ENABLE RATE-B and RATE-C GENERATOR control bits in the BCR.	Required internal rate generators are enabled.

3.14.5 Function Burst (Continued)

Table 3.14-7. Function Burst Example (Continued)

Operation	PCI Bus Action	Board Response
For software burst triggering, generate a software trigger to produce a single burst on all active output channels.	Set OUTPUT SW TRIGGER in the buffer operations register..	All active output channels produce a single burst in response to each software trigger, if software triggering is used.
For external burst triggering, or internal rate-generator triggering, no further bus activity is required.	---	All active output channels produce a single burst in response to each internal or external trigger.

3.14.6 Function Sequencing (Concatenation)

Table 3.14-8. Function Sequencing Example

Operation	PCI Bus Action	Board Response
Establish a periodic function as described in Paragraph 3.14.4. The following operations will replace the original ('old') function in each channel with a new function.	---	Each active output is producing a specific output function or waveform. The output buffer is circular (closed), and is not accessible from the bus.
Request buffer access	Set LOAD REQUEST in the buffer operations register.	The board will assert the LOAD READY flag when the EOF flag in the original function occurs.
Wait for the buffer to open.	Monitor the LOAD READY status flag. The buffer is open when this flag goes HIGH.	The EOF flag in the existing function set causes the LOAD READY bit in the buffer operations register to be asserted. The buffer is now open, and the original functions are being flushed from the buffer.
Load the new function for each active channel into the buffer. Set the end-of-frame (EOF) flag.	Write the function values for all active channels to the output buffer. Set the EOF flag (D16 in the output buffer) HIGH when writing the data value for the last channel in the last group.	New function values for all active channels reside in the buffer. The EOF flag is set HIGH in the buffer location that contains the last channel value in the last channel group. The original functions are still active, and the remaining values are flushed from the buffer as they are sent to the output channels.
(None required)	No further attention is required from the PCI bus.	The buffer returns to circular (closed) mode after the last data value in the original function set leaves the buffer. The new function then commences seamlessly and circulates within the buffer. Both the Load Request control bit and the Load Ready flag are cleared automatically when the buffer closes.

3.15 Analog Outputs DMA Operation

DMA transfers to the analog output FIFO buffer are supported in either block-mode or demand-mode, with the board operating as bus master. Bit 02 in the PCI Command register must be set HIGH to select the bus mastering mode. Refer to the PCI-9056 reference manual for a detailed description of the associated DMA configuration registers.

3.15.1 Block Mode

Table 3.15-1 illustrates a *typical* PCI register configuration that would control a non-chaining, non-incrementing ***block-mode*** DMA transfer in DMA Channel 01, in which a PCI interrupt is generated when the transfer has been completed.

Table 3.15-1. Typical Output DMA Register Configuration; Block Mode

PCI Offset	PCI Register	Function	Typical Value
94h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
98h	DMA PCI Address	Initial PCI data source address	*
9Ch	DMA Local Address	Initial (constant) local address	0000 0048h
A0h	DMA Transfer Byte Count	Number of bytes in transfer	*
A4h	DMA Descriptor Counter	Transfer direction (PCI bus to Local bus)	0000 0000h
A9h (A8, D15:8)	DMA Command/Status	Command and Status Register	01h 03h (See Text)

* Determined by specific transfer requirements.

For typical applications, the DMA Command Status Register would be initialized to 0000 0001h, and then changed to 0000 0003h to initiate a transfer.

3.15.2 Demand Mode

Demand mode transfers are controlled in a manner similar to block mode transfers, with the addition of ***demand-mode*** operation selected in the DMA mode register (D[12] = HIGH). Demand mode operation also requires the ***slow terminate*** mode (D[15] = LOW), which is the default state for this control bit. Table 3.15-2 shows a *typical* PCI register configuration for DMA Channel 01 demand mode operation.

Table 3.15-2. Typical Output DMA Register Configuration; Demand Mode

PCI Offset	PCI Register	Function	Typical Value
94h	DMA Mode	Bus width (32)	0002 1943h
98h	DMA PCI Address	Initial PCI data source address	*
9Ch	DMA Local Address	Initial (constant) local address	0000 0048h
A4h	DMA Descriptor Counter	Transfer direction (PCI bus to Local bus)	0000 0000h
A9h (A8, D15:8)	DMA Command/Status	Command and Status Register	01h 03h (See Text)

* Determined by specific transfer requirements.

NOTE: The default analog output DMA channel for demand-mode operation is Channel 1. To operate in DMA Channel-00, set the SWAP DEMAND MODE CHANNELS control bit HIGH in the BCR and use the Channel-00 PCI registers.

3.16 Assembly Configuration Register

The read-only Assembly Configuration register (Table 3.16-1) contains the existing firmware revision and a status field that indicates the availability of optional features.

Table 3.16-1. Assembly Configuration Register

Offset: 0000 0034h **Default: 00XX XXXXh**

BIT FIELD	DESCRIPTION
D00-D11	Firmware Revision
D12-D15	(Reserved bit field; Revision extension)
D16	Number of analog input channels: 0 => 4 Analog input channels. 1 => 2 Analog input channels.
D17	Number of analog output channels: 0 => 4 analog output channels. 1 => No analog outputs.
D18-D19	Master clock frequency: 0 => 40.320MHz Fixed 1 => 44.000MHz Fixed 2 => 40.000MHz, Voltage-Controlled 3 => (Reserved)
D20-D31	(Reserved bit field; returns all-zero).

3.17 Master Clock Frequency Adjustment (Firmware Revision-002 and Higher)

The master clock oscillator frequency **Fclk** can be adjusted approximately 50PPM to either side of its nominal value. The control field for this adjustment is the lower 16 bits (D00-15) of the MASTER CLOCK ADJUST register listed in Table 3.1-1. This field defaults to 8000h after initialization, and is adjustable from 0000h to FFFFh. Lower values produce lower frequencies, with 0000h producing a negative frequency deviation approximately 50PPM below nominal, and FFFFh producing a positive deviation 50PPM above nominal.

Writing to this register automatically initiates a loading sequence in which the new contents of the register are transferred to the DAC that controls the master clock oscillator. The entire sequence has a duration of less than ten microseconds.

SECTION 4.0

PRINCIPLES OF OPERATION

4.1 General Description

Each of four analog input channels contains a selftest input switching network, a differential amplifier, a scaling network and a 16-Bit ADC (Figure 4.1-1), and provides input ranges of ±10V, ±5V and ±2.5V. A 256 Ksample FIFO buffer accumulates analog input data for subsequent retrieval through the PCI bus. Four 16-bit analog output channels provide software-selected output ranges of ±2.5V, ±5V or ±10V, and are accessed either directly through dedicated control registers, or through a 256 Ksample FIFO buffer. A 16-Bit bidirectional digital port can be configured as two independent byte-wide ports.

A PCI interface adapter provides the interface between the controlling PCI bus and an internal local controller, and supports universal signaling. +5 VDC power from the PCI bus is converted into regulated power voltages for the internal analog networks.

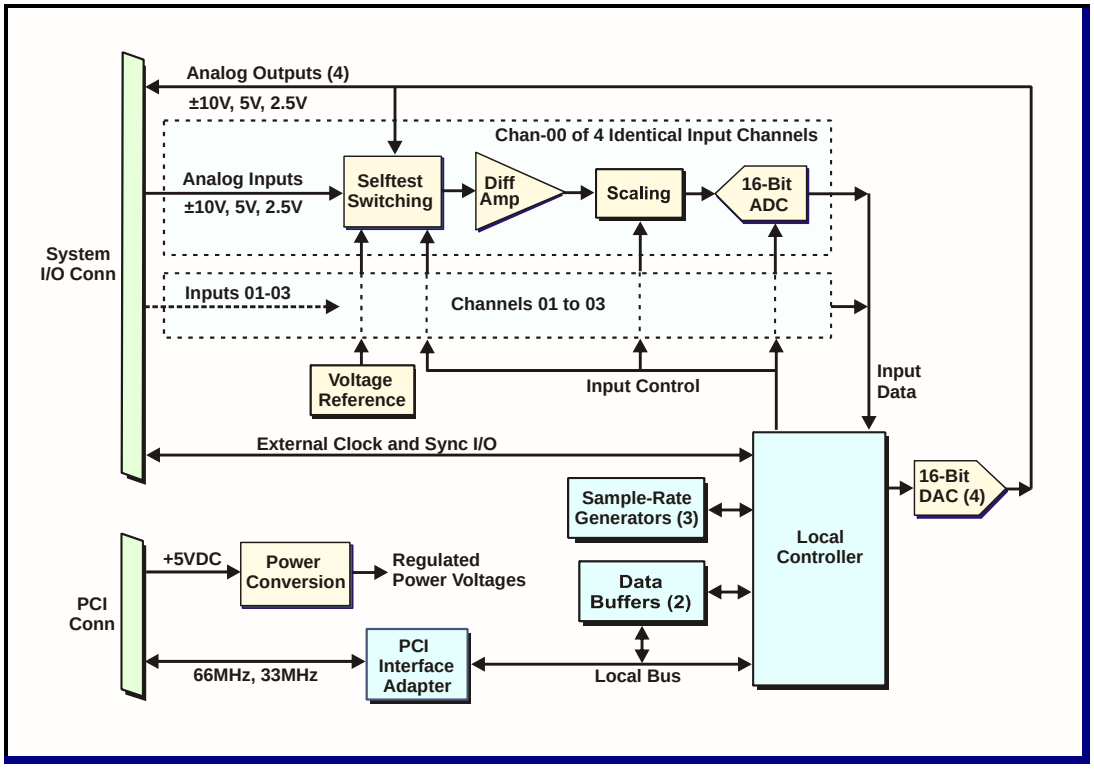

Figure 4.1-1. Functional Block Diagram

Selftest switches at the inputs provide test signals for autocalibration of all input and output channels, and can be configured to accept either differential or single-ended system inputs.

Analog input sampling and output clocking on multiple target boards can be synchronized to a single software-designated initiator board.

4.2 Analog Inputs

Analog-to-digital conversions can be performed on signals from any of several sources, which are selected by the selftest switches shown in Figure 4.1-1. During normal operation, four 16-bit sigma-delta ADC's receive system analog input signals from the system I/O connector. For integrity testing and autocalibration operations, the internal voltage reference and the analog outputs can be routed through the selftest switches to the ADC's. An attenuator in each channel provides the necessary scaling for software-controlled input ranging.

The serial input data from each ADC is deserialized and multiplexed into a continuous data stream within the local controller. The output of the data multiplexer passes through a digital processor that applies gain and offset correction values obtained during autocalibration. The corrected data is formatted, and the final processed and formatted data is loaded into the analog input data buffer.

ADC clocking can be supplied either from an internal PLL rate generator, or from an external source. Triggered bursts can be acquired by using a second internal rate generator, or an external input as a trigger source. The burst block-size can be controlled by a 24-Bit counter, or sampling can be configured to operate continuously after a trigger. The ADC external clock and trigger pins can be configured independently as inputs or outputs.

4.3 Input Data Buffer

A 256K-sample FIFO buffer accumulates analog input data for subsequent retrieval through the PCIbus. The buffer is supported by a 'size' register that tracks the number of values in the buffer, and by an adjustable threshold flag that generates a status flag in response to the number of samples contained within the buffer.

4.4 Analog Outputs

Four independent 16-bit DAC's are controlled either directly through dedicated control registers, or through a 256 Ksample FIFO buffer. The buffer can be operated either open for data streaming, or closed (circular) for periodic function generation. Function concatenation from the PCI bus is supported.

Output clocking can be supplied either from a third internal 24-Bit rate generator, or from an external source. Triggered bursts are supported, and share the triggering function with the analog inputs (4.2). The output burst size is controlled by a tag-bit attached to the last output value in a sequence. If the tag-bit is not attached, a burst will operate continuously after a trigger, or until the buffer goes empty.

4.5 Autocalibration

Autocalibration is an embedded firmware utility that calibrates all analog input and output channels to a single internal voltage reference. The utility can be invoked at any time by the control software.

The internal voltage reference is used to calibrate the span of each channel, and a zero-reference is used to calibrate the offset value. Correction values determined during autocalibration are applied to each digitized sample acquired during acquisition, and to each output value written to the DAC channels. Correction values are retained until the autocalibration sequence is repeated, or until power is removed.

4.6 Power Control

Regulated and low-noise supply voltages of +5 VDC and ±15 VDC are required for the analog networks, and are derived from the raw +5-Volt input provided by the PCI bus, both by switching preregulators and by linear postregulators.

APPENDIX A

LOCAL REGISTER QUICK REFERENCE

APPENDIX A
LOCAL REGISTER QUICK REFERENCE

This appendix summarizes the local registers and principal control-bit fields described in Section 3.

Table 3.1-1. Control and Status Registers

OFFSET (Hex)	REGISTER	MODE[1]	DEFAULT	PRIMARY FUNCTION	REF
0000	BOARD CONTROL	RW	2202 0020h	Board Control Register (BCR).	3.2
0004	DIGITAL I/O PORT	RW	00XX 00XXh	16-Bit Digital I/O port data.	3.9
0008	ANALOG OUTPUT CHAN 00	RW	0000 8000h	Output Channel 00 data.	3.12
000C	ANALOG OUTPUT CHAN 01	RW	0000 8000h	Output Channel 01 data.	
0010	ANALOG OUTPUT CHAN 02	RW	0000 8000h	Output Channel 02 data.	
0014	ANALOG OUTPUT CHAN 03	RW	0000 8000h	Output Channel 03 data.	
0018	ANALOG INPUT BUFFER	RO	00XX XXXXh	Analog input buffer data.	3.4.5
001C	RATE GENERATOR A	RW	0103 F020h	Rate-A generator control	3.7.1
0020	RATE GENERATOR B	RW	0000 2760h	Rate-B generator divider; 24 bits.	3.7.2
0024	INPUT CONFIGURATION	RW	0F00 0400h	Analog inputs channel-mask and burst-size.	3.4.2 3.4.4.2
0028	INPUT BUFFER SIZE	RO	0000 0000h`	Number of data values in the input buffer.	3.4.5.2
002C	INPUT BUFFER THRESHOLD	RW	0003 FFFEh	Input buffer status flag threshold.	3.4.5.2
0030	PRIMARY STATUS	RW	0000 0X00h	Principal status-flag register	3.11
0034	ASSEMBLY CONFIGURATION	RO	000X XXXXh	Options and firmware revision.	3.16
0038	Autocal Values [2]	RW	0000 XXXXh	Autocal value readback.	---
003C	BUFFERED OUTPUT OPERATIONS	RW	0000 104Fh	Buffered Analog Outputs Control	3.13
0040	OUTPUT BUFFER THRESHOLD	RW	0003 FFFEh	Output buffer status flag threshold.	3.13.2.3
0044	OUTPUT BUFFER SIZE	RO	0000 0000h	Number of data values in the output buffer.	3.13.2.3
0048	ANALOG OUTPUT BUFFER	WO	0000 0000h	Analog Output Data Buffer.	3.13.2
004C	RATE GENERATOR C	RW	0000 007Eh	Rate-C generator divider; 24 bits.	3.13.4.1.2
0050-005C	(Auxiliary Registers)	RW	0000 0000h	Four auxiliary 32-Bit user registers. No internal functions.	---
0060	MASTER CLOCK ADJUST	RW	0000 8000h	Master clock frequency adjustment.	3.17
0064-007C	(Reserved)	---	---	---	---

Notes: 1. RW = Read/Write, RO = Read-Only, WO = Write-Only.
2. Maintenance register; Shown for reference only.

Table 3.2-1. Board Control Register (BCR)

Offset: 0000h **Default: 2202 0020h**

BIT	MODE [1]	DESIGNATION	DEF	DESCRIPTION	REF
D00-D02	RW	ANALOG INPUT MODE	0	Analog input mode: 0 => Differential system inputs 1 => Single-ended system inputs 2 => Zero selftest 3 => VREF selftest 4 => Output Channel 00 5 => Output Channel 01 6 => Output Channel 02 7 => Output Channel 03	3.4.1
D03	R/W	(Reserved)	0	---	---
D04-D05	RW	INPUT RANGE	2	Analog input range: 0 => ±2.5V 2 => ±10V 1 => ±5V 3 => (Reserved)	3.4.3
D06-D07	RW	(Reserved)	0	---	---
D08	RW	INPUT S/W CLOCK [2]	0	Initiates a single sample of active input channels. Overrides existing input clocking source.	3.4.4
D09	RW	ENABLE INPUT BURST	0	Enables triggered burst input acquisition.	3.4.4.2
D10	RO	INPUT BURST BUSY	0	HIGH when a triggered input burst is in progress.	3.4.4.2
D11	RW	INPUT S/W TRIGGER [2]	0	Initiates a single input data burst. Overrides existing burst triggering source.	3.4.4.2
D12	RW	ENABLE INPUT BUFFER	0	Enables the analog input buffer for accepting data.	3.4.5.1
D13	RW	CLEAR INPUT BUFFER [2]	0	Clears (empties) the analog input data buffer.	3.4.5.1
D14	RO	INPUT BUFFER THRESHOLD FLAG [3]	0	HIGH when the number of values in the input buffer exceeds the selected buffer threshold.	3.4.5.2
D15	RW	INPUT BUFFER OVERFLOW	0	Set HIGH if the input buffer overflows. Stays HIGH until cleared from the bus or by a board reset.	3.4.5.1
D16-D17	RW	OUTPUT RANGE	2	Analog Output Voltage Range: 0 => ±2.5V 2 => ±10V 1 => ±5V 3 => (Reserved)	3.12.1 3.13.1.2
D18	RW	SIMULTANEOUS OUTPUTS	0	When HIGH, all outputs update simultaneously in response to an output clock. When LOW, each output is updated immediately when new data is received.	3.12.2.2
D19	RW	ENABLE BUFFERED OUTPUTS	0	When HIGH, enables the analog output FIFO buffer, and disables the analog output registers ANALOG OUTPUT CHAN xx.	3.13
D20	RW	OUTPUT S/W CLOCK [2, 3, 4]	0	Produces a single analog output clock. Overrides existing output clocking source.	3.13.4.1
D21	RW	TRIGGER INITIATOR	0	Configures the shared analog input/output hardware trigger pin as an output if HIGH, or as an input if LOW.	3.4.4.2 3.13.5.2
D22	R/W	ENABLE RATE-C GENERATOR	0	Enables the Rate-C generator for analog outputs.	3.13.4.1.2
D23	R/W	INPUT BUFFER UNDERFLOW [5]	0	Set HIGH if the input buffer underflows. Stays HIGH until cleared from the bus or by a board reset.	3.4.5.1
D24	RW	ANALOG INPUT CLK INITIATOR	0	Configures the analog input I/O clock as an *output* if HIGH, or as an *input* if LOW.	3.8
D25	RW	OFFSET BINARY	1	Selects offset-binary analog I/O data format when HIGH, or two's complement when LOW.	3.6
D26	RW	ENABLE RATE-A GENERATOR	0	Enables the Rate-A generator for analog inputs.	3.7.1
D27	RW	ENABLE RATE-B GENERATOR	0	Enables the Rate-B generator for triggered bursts.	3.7.2
D28	RW	AUTOCAL [2]	0	Initiates an autocalibration operation when asserted. Clears automatically upon completion,	3.10
D29	RO	AUTOCAL PASS	1	Set HIGH at reset or autocal initialization. A HIGH state after autocal confirms a successful calibration.	3.10
D30	R/W	SWAP DEMAND MODE CHANNELS	0	Reverses the default demand-mode DMA channels for analog inputs and outputs	3.5.2 3.15.2
D31	RW	INITIALIZE [2]	0	Initializes the board. Sets all register defaults.	3.3.2

Notes: 1. RW = Read/Write, RO = Read-Only. 2. Clears automatically. 3. Duplicated elsewhere
4. May invoke immediate mode output clocking in some systems.
5 Remains HIGH until cleared by a direct write as LOW, or by initialization.

Table 3.3-1. Configuration Operations

Operation	Maximum Duration
PCI configuration registers are loaded from internal ROM	3 ms
Internal control logic is configured from internal ROM	300 ms
Internal control logic is initialized	3 ms

Table 3.4-1. Input Configuration Register

Offset: 0024h **Default: 0F00 0400h**

BIT	MODE *	DESIGNATION	DEF	DESCRIPTION
D00-D23	RW	BURST BLOCK SIZE	0400h	Number of active channel sets acquired during a triggered burst.
D24	RW	ENABLE INPUT 00	1	Analog input channel selection mask.
D25	RW	ENABLE INPUT 01	1	
D26	RW	ENABLE INPUT 02	1	
D27	RW	ENABLE INPUT 03	1	
D28-D31	RW	(Reserved)	0	---

* RW = Read/Write, RO = Read-Only.

Table 3.4-2. Input Data Buffer

Offset: 0018h **Default: 00XX XXXXh**

DATA BIT	DESIGNATION	DESCRIPTION
D00	DATA00	Data value least significant bit (LSB)
D01-D14	DATA01 - DATA14	Data value intermediate bits
D15	DATA15	Data value most significant bit (MSB)
D16	FIRST-CHANNEL TAG	Tag assigned to first (lowest-numbered) active channel.
D17	END OF BURST (EOB)	Identifies the last input value in a burst.
D18-D31	(Reserved)	Always zero.

Table 3.4-3. Input Buffer Threshold Register

Offset: 002Ch **Default: 0003 FFFEh**

BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00-D18	RW	INPUT BUFFER THRESHOLD	3 FFFEh	Specifies the number of values in the input buffer, above which the threshold flag is asserted HIGH.
D19	RO	INPUT BUFFER THRESHOLD FLAG [1]	0	HIGH when the number of values in the input buffer exceeds the specified buffer threshold.
D20-D31	RO	Reserved	0	---

1. Duplicated in the BCR.

Table 3.5-1. Typical Input DMA Register Configuration; Block Mode

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial (constant) local address	0000 0018h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

* Determined by specific transfer requirements.

Table 3.5-2. Typical Input DMA Register Configuration; Demand Mode

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32)	0002 1943h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial (constant) local address	0000 0018h
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

* Determined by specific transfer requirements.

Table 3.7-1. Analog Input Sample Rate-A Generator Control Register

Offset: 001Ch **Default: 0103 F020h**

Bit Field	Mode	Designation	Default	Function
D[09..00]	R/W	VCO FACTOR **(Nvco)**	20h	PLL VCO factor; 30-1000.
D[11..10]	R/W	(Reserved)	0h	---
D[21..12]	R/W	REF FACTOR **(Nref)**	3Fh	PLL Reference factor; 30-1000.
D[23..22]	R/W	(Reserved)	0h	---
D[28..24]	R/W	Divisor **(Ndiv**)	01h	Ndiv (Zero for Fsamp >600KSPS, 1-20 for Fsamp = 30-600KSPS)
D[31..29]	R/W	(Reserved)	0h	---

Table 3.7-2. Sample Rate Fsamp Control Examples

Fclk (MHz)	Nvco [1]	Nref [1]	Fgen (MHz)	Ndiv	Fsamp (KSPS)
40.320	50	63	16.000	0	**1000**
	50	84	12.000	0	**750**
	40	42	9.600	0	**600**
	40	84	19.200	1	**600**
	32	63	10.240	1	**320**
	40	84	19.200	3	**200**
	40	42	9.600	3	**100**
	40	42	9.600	10	**30**
	40	84	19.200	20	**30**

1. Decimal values.

Table 3.7-3. Analog Input Trigger Rate-B Generator Register

Offset: 0020h **Default: 0000 2760h)**

DATA BIT	MODE*	DESIGNATION	DEFAULT	DESCRIPTION
D00-D23	R/W	**Ndiv-b**	---	Rate generator frequency control
D24-D31	RO	(Inactive)	0	---

* R/W = Read/Write, RO = Read-Only.

Table 3.7-4. Rate-B Generator Frequency Selection

Ndiv-b		FREQUENCY Fgen-b (40.320 MHz Master Clock)*
(Dec)	(Hex)	(kHz)
40	0028	1008.00
41	0029	982.93
---	---	Fgen (Hz) = 40320 (kHz) / Ndiv-b

* ±0.003 percent.

Table 3.9-1. Digital I/O Port Register

Offset: 0004h **Default: 00XX 00XXh**

DATA BIT	MODE*	DESIGNATION	DEFAULT	DESCRIPTION
D00-D07	RW	DIO BYTE 00	XXh	System connector pins DIO 00 through DIO 07.
D08	RW	BYTE 00 OUTPUT	0	Direction control for DIO BYTE 00. When LOW, DIO BYTE 00 is an input field. When HIGH, DIO BYTE 00 is an output field.
D09-D15	RO	(Reserved)	0h	Read back as all-zero.
D16-D23	RW	DIO BYTE 01	XXh	System connector pins DIO 08 through DIO 15.
D24	RW	BYTE 01 OUTPUT	0	Direction control for DIO BYTE 01. When LOW, DIO BYTE 01 is an input field. When HIGH, DIO BYTE 01 is an output field.
D25-D31	RO	(Reserved)	0h	Read back as all-zero.

Table 3.11-1 Primary Status Register

Offset 0x0030 **Default 0x0000 0X00**

SELECTION BIT [1]	CRITICAL EVENT	RESPONSE BIT [2]	REFERENCE PARAGRAPH
D00	Autocal completed	D16	3.10
D01	Input Buffer threshold flag HIGH-to-LOW transition	D17	3.4.5.2
D02	Input Buffer threshold flag LOW-to-HIGH transition	D18	
D03	Input Buffer Overflow or Underflow	D19	3.4.5.1
D04	Analog Input Burst initiated (BURST BUSY LO-HI)	D20	3.4.4.2
D05	Analog Input Burst Completed (BURST BUSY HI-LO)	D21	
D06	Analog Input Clock	D22	3.4.4
D07	Analog Output Clock	D23	3.13.4
D08	Digital I/O Port DIO 00 LOW-to-HIGH transition	D24	3.9
D09	Output Buffer threshold flag HIGH-to-LOW transition	D25	3.13.2.3
D10	Output Buffer threshold flag LOW-to-HIGH transition	D26	
D11	Output Load-Ready Flag HIGH-to-LOW transition	D27	3.13.3.3
D12	Output Load-Ready Flag LOW-to-HIGH transition	D28	
D13	Analog Output Burst Ready	D29	3.13.5.2
D14	Output Buffer Overflow or Frame Overflow	D30	3.13.2.3 3.13.3.3
D15	(Reserved)	D31	---

1. Event selection. Enables assertion of the corresponding response bit when the selected event occurs.
2. Event response. Asserted HIGH when a selected event occurs. Remains HIGH until cleared LOW.

Table 3.12-1. Analog Output Channel Data Register

Offset: 0008h - 0014h **Default: 0000 8000h**

DATA BIT	DESIGNATION	DESCRIPTION
D00	DATA00	Data value least significant data bit
D01-D14	DATA01 - DATA14	Data value intermediate data bits
D15	DATA15	Data value most significant data bit
D16-D31	(Reserved)	Data in this field is ignored.

Table 3.12-2 Simultaneous Output Clock Source Selection

Register	Selection Control Bit	Output Clock Source				
		S/W Clock (BCR, BOR)	Rate-C Gen	External Input	Analog Inputs (Fsamp)	Analog Inputs (Acquis)
BCR	SIMULTANEOUS OUTPUTS	HIGH	HIGH	HIGH	HIGH	HIGH
	ENABLE RATE-C GENERATOR	X	HIGH	X	X	X
BOR [1]	ANALOG OUTPUT CLK INITIATOR	X	HIGH	LOW	LOW	X
	SYNC AO WITH INPUTS	0	0	0	0	1h [2]
						2h [3]

1. Buffered Outputs Operations register (Table 3.13-2).
2. ADC sample rate Fsamp (Active whether or not input acquisition is disabled; for example between input bursts).
3. ADC acquisition rate (Only those samples that produce data in the input buffer).

Table 3.13-1. Summary of Output Control Parameters

Parameter	Mode	Description
Data Control	Active Channels; **Channel Group**	A single set of all active output channels constitutes an ***Active Channel Group***. Active channels are selected under a channel mask.
	Data Frame	All data values in the buffer comprise a *Data Fr*ame.
	Data Coding	Output data can be coded either in offset-binary format or in two's complement format.
Buffer Configuration	Open	Data read from the buffer is used and then discarded, until the buffer is empty.
	Circular (closed)	Data within the buffer is recirculated. Each value read from the output of the buffer FIFO is written back to the input of the FIFO. An end-of-frame (EOF) flag tracks the movement of data through the buffer.
Clock Source	External	External hardware provides the sample clock.
	Internal	The sample clock is provided by an internal rate generator, at a rate determined by the sample rate control register.
Clocking Mode	Simultaneous	At each clock occurrence, the next channel group (i.e.: a single group of all active channel values) in the output buffer is transferred to the respective analog output channels. All outputs are updated simultaneously.
	Sequential	At each clock occurrence, the next active channel value in the output buffer is transferred to the associated analog output channel, which is updated immediately.
Sampling Mode	Continuous	The contents of the output buffer are sampled continuously at the selected clock rate.
	Triggered Burst	A single data frame in the buffer is clocked to the outputs.

Table 3.13-2. Buffered Output Operations Register

Offset: 003Ch **Default: 0000_104Fh**

BIT	MODE	DESIGNATION	DEF	DESCRIPTION	REF
D00	R/W	AO CHAN 00 ACTIVE	1	Active-channel mask for analog output channels. HIGH => Active; LOW => Inactive.	3.13.1.1
D01	R/W	AO CHAN 01 ACTIVE	1		
D02	R/W	AO CHAN 02 ACTIVE	1		
D03	R/W	AO CHAN 03 ACTIVE	1		
D04	R/W	ANALOG OUTPUT CLK INITIATOR	0	Selects the internal Rate-C generator for output clocking if HIGH, or the Output Clock I/O hardware input if LOW. Ignored if 'SYNC AO WITH INPUTS' is nonzero.	3.13.4.1
D05	R/W	ENABLE OUTPUT CLOCKING	0	Enables output clocking when HIGH. Disables clocking when LOW. Default is LOW (clocking disabled).	3.13.4
D06	RO	OUTPUT CLOCK READY	1	Indicates when HIGH that an output clock will be accepted. If LOW, indicates that the output will not respond to a clock.	3.13.4
D07	R/W	OUTPUT SW CLOCK [1, 3]	0	Produces a single output clock event when asserted. Independent of clocking mode. Duplicated in the BCR.	3.13.4.1
D08	R/W	CIRCULAR BUFFER	0	Selects circular buffer configuration if HIGH, or open self-flushing buffer configuration if LOW. Access for loading new data into the circular buffer must be requested by asserting LOAD REQUEST. Default is LOW; i.e. open buffer.	3.13.2.5
D09	R/W	LOAD REQUEST [1]	0	When set HIGH, requests loading access to the circular buffer. Initializes LOW.	3.13.3.3
D10	RO	LOAD READY	0	Set HIGH when the frame index passes through zero, if both CIRCULAR BUFFER and LOAD REQUEST are HIGH. When HIGH, indicates that the circular buffer is ready to accept new data. Available also in the PSR. Defaults HIGH.	3.13.3.3
D11	R/W	CLEAR OUTPUT BUFFER [1]	0	Resets the output buffer to empty.	3.13.2.3
D12	RO	AO BUFFER EMPTY	1	Indicates the analog output buffer is empty.	3.13.2.3
D13	RO	AO BUFFER THRESHOLD	0	Analog output buffer threshold flag. Duplicated in the AO Buffer Threshold register.	3.13.2.3
D14	RO	(Reserved)	0	Inactive; Returns zero.	---
D15	RO	AO BUFFER FULL	0	Indicates the output buffer is full.	3.13.2.3
D16	R/W	AO BUFFER OVERFLOW [2]	0	Set HIGH when data is written to a full buffer	3.13.2.3
D17	R/W	FRAME OVERFLOW [2]	0	Set HIGH when data is written to a closed buffer.	3.13.3.3
D18	RO	BURST READY	0	If HIGH, indicates that a burst trigger will be accepted. If LOW, indicates that the output will not respond to a trigger.	3.13.5.2
D19	R/W	ENABLE OUTPUT BURST	0	Enables analog output burst operation.	3.13.5.1
D20	R/W	OUTPUT SW TRIGGER [1]	0	Produces a single output trigger event when asserted. Clears LOW automatically when the clock event is completed. Independent of triggering mode. Duplicated in the BCR.	3.13.5.2
D21-D22	R/W	SYNC AO WITH INPUTS	0h	Analog input mode: 0 => Independent outputs clocking. 1 => Output clocking rate equals ADC sample rate. 2 => Output clocking rate equals ADC acquisition rate. 3 => (Reserved)	3.12.2.2
D23-D31	RO	(Reserved)	0	Inactive. Returns all-zero.	---

1. Clears LOW automatically when operation is completed.
2 Remains HIGH until cleared by a direct write as LOW, or by initialization.
3 May invoke immediate mode output clocking in some systems. Duplicated in the BCR.

Table 3.13-3. Analog Output Buffer

Offset: 0048h **Default: N/A (Write-Only)**

BIT	MODE*	DESIGNATION	DESCRIPTION
D00	WO	DATA 00	Least significant data bit
D01-D14	WO	DATA 01 - DATA 14	Intermediate data bits
D15	WO	DATA 15	Most significant data bit
D16	WO	EOF FLAG	End-of-frame (EOF) flag.
D17-D31	WO	---	(Inactive)

* WO indicates write-only access. Read-access returns all-zero value.

Table 3.13-4. Output Buffer Size Register

Offset: 0044h **Default: 0000 0000h**

DATA BIT	MODE*	DESIGNATION	DEF	DESCRIPTION
D00-D18	RO	BUFFER SIZE	0 0000h	Number of values in the output buffer
D19-D31	RO	(Inactive)	0	---

Table 3.13-5. Output Buffer Threshold Register

Offset: 0040h **Default: 0003 FFFEh**

BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00-D18	RW	OUTPUT BUFFER THRESHOLD	3 FFFEh	Specifies the number of values in the output buffer, above which the threshold flag is asserted HIGH.
D19	RO	OUTPUT BUFFER THRESHOLD FLAG	0	HIGH when the number of values in the output buffer *exceeds* the specified buffer threshold.
D20-D31	RO	Reserved	0	---

Table 3.13-6. Output Sample Rate Control Register (Rate-C)

Offset: 004Ch **Default: 0000_007Eh**

DATA BIT	MODE	DESIGNATION	DESCRIPTION
D00	R/W	RATE 00	Least significant rate bit
D01-D22	R/W	RATE 01 - RATE 22	Intermediate rate bits
D23	R/W	RATE 23	Most significant rate bit
D24-D31	RO	---	Inactive. Returns all-zero.

Table 3.13-7. Output Sample Rate Selection

Ndiv-c		FREQUENCY Fgen (40.320 MHz Master Clock)*
(Dec)	(Hex)	(kHz)
40	0028	1008.00
41	0029	982.93
---	---	Fgen (Hz) = 40320 (kHz) / Ndiv-c

* ±0.003 percent.

Table 3.15-1. Typical Output DMA Register Configuration; Block Mode

PCI Offset	PCI Register	Function	Typical Value
94h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
98h	DMA PCI Address	Initial PCI data source address	*
9Ch	DMA Local Address	Initial (constant) local address	0000 0048h
A0h	DMA Transfer Byte Count	Number of bytes in transfer	*
A4h	DMA Descriptor Counter	Transfer direction (PCI bus to Local bus)	0000 0000h
A9h (A8, D15:8)	DMA Command/Status	Command and Status Register	01h 03h (See Text)

* Determined by specific transfer requirements.

Table 3.15-2. Typical Output DMA Register Configuration; Demand Mode

PCI Offset	PCI Register	Function	Typical Value
94h	DMA Mode	Bus width (32)	0002 1943h
98h	DMA PCI Address	Initial PCI data source address	*
9Ch	DMA Local Address	Initial (constant) local address	0000 0048h
A4h	DMA Descriptor Counter	Transfer direction (PCI bus to Local bus)	0000 0000h
A9h (A8, D15:8)	DMA Command/Status	Command and Status Register	01h 03h (See Text)

* Determined by specific transfer requirements.

Table 3.16-1. Assembly Configuration Register

Offset: 0000 0034h **Default: 00XX XXXXh**

BIT FIELD	DESCRIPTION
D00-D11	Firmware Revision
D12-D15	(Reserved bit field; Revision extension)
D16	Number of analog input channels: 0 => 4 Analog input channels. 1 => 2 Analog input channels.
D17	Number of analog output channels: 0 => 4 analog output channels. 1 => No analog outputs.
D18-D19	Master clock frequency: 0 => 40.320MHz Fixed 1 => 44.000MHz Fixed 2 => 40.000MHz, Voltage-Controlled 3 => (Reserved)
D20-D31	(Reserved bit field; returns all-zero).

APPENDIX B

MIGRATION ISSUES FROM PMC66-16AISS8AO4

Appendix B

Migration Issues From PMC66-16AISS16AO2

Operation of the PMC66-16HSDI4AO4 is very similar to that of the PMC66-16AISS8AO4. This appendix summarizes the principal similarities and differences between the two products, and is provided as a general guide rather than a definitive list of migration requirements.

B.1. Comparison of Features

Table B.1 compares principal PMC66-16HSDI4AO4 and PMC66-16AISS8AO4 features. Modified features are highlighted in bold type.

Table B.1. PMC66-16HSDI4O4, PMC66-16AISS8AO4 Comparison

Feature	PMC66-16HSDI4AO4	PMC66-16AISS8AO4
Input Channels	**Four 16-Bit ADC's; Sigma-Delta**	**Eight 16-Bit ADC's; SAR**
Input Sample Rates	**30-1000 KSPS/Chan**	**Zero to 2.0MSPS/Chan**
Input/Output Synchronization	**Yes**	**No**
Input Buffer	256K-Sample FIFO	256K-Sample FIFO
Input Ranges	±10V, ±5V, ±2.5V	±10V, ±5V, ±2.5V
Output Channels	Four 16-Bit Dac's	Four 16-Bit Dac's
Output Registers *	Four; One per channel	Four; One per channel
Output Buffer *	256K-Sample FIFO	256K-Sample FIFO
Output FIFO Buffer Organization	Fixed size, with adjustable threshold flag	Fixed size, with adjustable threshold flag
Output Clock Rates	Zero to 1.0MSPS/Chan	Zero to 1.0MSPS/Chan
Output Configuration	Single-Ended	Single-Ended
Function Generation	Yes	Yes
Digital I/O Port	16-Bit Bidirectional TTL; Byte oriented.	16-Bit Bidirectional TTL; Byte oriented.
PCI Adapter	PCI-9056 (66MHz PCI)	PCI-9056 (66MHz PCI)
Rate Generators	Three, with 24-Bit dividers	Three, with 24-Bit dividers
Interrupt	Replaced with a primary status register	Replaced with a primary status register
PCI Interface	PCI 2.3; 33MHz/66MHz	PCI 2.3; 33MHz/66MHz
DMA (Buffers)	Block mode, Demand mode	Block mode, Demand mode
Local Clock	40.32 MHz Standard	40.32 MHz Standard

* Output control is selectable as 'buffer' or 'register.'

B.2. Migration Issues from PMC66-16AISS8AO4

Table 2.2-1. System I/O Connector Pin Functions:

- Input channels 04 through 07 have been deleted.

Table 3.1-1. Control and Data Registers:

- 'BCR, 'Rate Gen A' and 'Input Config' control register default values have changed.

Table 3.2-1. Board Control Register (BCR):

- The original two input range control fields have been consolidated into a single field.

Paragraph 3.4. Analog Inputs:

- Input channels 04 through 07 have been deleted.

Paragraph 3.4.3. Input Ranges:

- All input channels share a common range.

Paragraph 3.7.1. Rate-A Generator:

- To support the sigma-delta input converters, the Rate-A generator has been converted to an adjustable high-frequency PLL oscillator that is controlled by two integer parameters.
- The analog input sample rate is now constrained to 30-1000KSPS.

Paragraph 3.12.2.2. Simultaneous (Clocking):

- Analog output clocking can now be synchronized with analog input sampling.

Table 3.13-2. Buffered Output Operations Register:

- A new control field 'Sync AO With Inputs' controls synchronized input/output clocking.

Table 3.16-1. Assembly Configuration Register:

- Assembly options have been modified to conform to PMC66-16HSDI4AO4 requirements.

Paragraph 3.17. Master Clock Frequency Adjustment:

- Provision was added for fine-adjustment of the master clock frequency.

APPENDIX C

EFFECTS OF MODIFIED MASTER CLOCK FREQUENCY

C.0 Overview

The standard value for the master clock frequency **Fclk** is 40.320MHz, but **Fclk** can be supplied as any frequency listed in the product specification as available. The remainder of this appendix outlines those board characteristics that are controlled by **Fclk**, using 44.000MHz and 44.000MHz as an example frequencies.

C.1a Default Sample and Clocking Rates with Fclk = 44MHz (Paragraph 3.3.2):

- The ADC (Rate-A) generator is adjusted to **349.2 kHz**, and is disabled. (3.7.1),
- The burst-trigger (Rate-B) generator is adjusted to **4.365 kHz**, and is disabled. (3.7.2)
- The DAC (Rate-C) generator is adjusted to **349.2 kHz**, and is disabled. (3.13.4.1.2).

C.1b Default Sample and Clocking Rates with Fclk = 40MHz (Paragraph 3.3.2):

- The ADC (Rate-A) generator is adjusted to **317.5 kHz**, and is disabled. (3.7.1),
- The burst-trigger (Rate-B) generator is adjusted to **3.968 kHz**, and is disabled. (3.7.2)
- The DAC (Rate-C) generator is adjusted to **317.5 kHz**, and is disabled. (3.13.4.1.2).

C.2 Rate-A Generator Frequency (Paragraph 3.7.1)**:**

Fgen-a = (Fclk/2) * (Nvco / Nref),
= 22MHz * (Nvco / Nref) if **Fclk** = 44MHz,
= 20MHz * (Nvco / Nref) if **Fclk** = 40MHz,

where **Fclk** = Master clock frequency, and **Nvco** and **Nref** are integers between 30 and 1000. **Fgen-a** and **Fclk** are both expressed in the same frequency units.

Table C.2-1. Sample Rate Fsamp Control Examples

Fclk (MHz)	Nvco [1]	Nref [1]	Fgen (MHz)	Ndiv	Fsamp (KSPS)
44.000	32	44	16.000	0	**1000**
	40	55	16.000	0	**1000**
	30	55	12.000	0	**750**
	24	55	9.600	0	**600**
	48	55	19.200	1	**600**
40.000	40	50	16.000	0	**1000**
	30	50	12.000	0	**750**
	24	50	9.600	0	**600**
	48	50	19.200	1	**600**

1. Decimal values.

C.3 Rate-B Generator Frequency (Paragraph 3.7.2)**:**

Fgen-b = Fclk / Ndiv-b,

= 44MHz / Ndiv-b if **Fclk** = 44MHz,

= 40MHz / Ndiv-b if **Fclk** = 40MHz,

where **Fclk** is the master clock frequency for the board, and **Ndiv-b** is the value written to the Rate-B Generator register. **Fgen-b** and **Fclk** are both expressed in the same frequency units.

Table C.3-1a. Input Rate Generator-B Frequency Selection; Fclk = 44MHz

Ndiv		FREQUENCY Fgen-b (44.000 MHz Master Clock)*
(Dec)	(Hex)	(kHz)
44	002C	1000.00
45	002D	977.78
---	---	Fgen (Hz) = 44,000 (kHz) / Ndiv

Table C.3-1b. Input Rate Generator-B Frequency Selection; Fclk=40MHz

Ndiv		FREQUENCY Fgen-b (40.000 MHz Master Clock)*
(Dec)	(Hex)	(kHz)
40	0028	1000.00
41	0029	975.61
---	---	Fgen (Hz) = 40,000 (kHz) / Ndiv

C.4 Rate-C Generator Frequency (Paragraph 3.13.4.1.2)**:**

Fclock = Fclk / Ndiv-c,

= 44MHz / Ndiv-c if **Fclk** = 44MHz,

= 40MHz / Ndiv-c if **Fclk** = 40MHz,

where **Fclk** is the master clock frequency for the board, and **Ndiv-c** is the value written to the Rate-C Generator register. **Fgen-c** and **Fclk** are both expressed in the same frequency units. Example Table C.3-1 applies to the Rate-C generator as well as to the Rate-B rate generator.

Revision History:

02-11-2009: Origination. Preliminary draft.

05-17-2009: Paragraph 3.12.2.2: Added note regarding 'Sync AO with inputs' control bit.
Paragraph 3.13.4.1: Added paragraph reference.

09-03-2009: Title page: Corrected title.
Paragraph 3.7.1: Modified Fgen frequency range.
Tables 3.2-1, 3.13-2: Added Note pertaining to output software clocking.

02-20-2010: Table 3.1-1: Added new register Master Clock Adjust
Paragraph 3.4: Revised max sample rate.
Table 3.16-1: Updated assembly configuration register.
Paragraph 3.17: New paragraph describing master clock frequency fine adjustment.
Appendix-C: Added operation with a 40.000MHz master clock frequency..

03-23-2010: Paragraph 3.10: Updated autocal requirements.

06-30-2010: Figure 1.1-1: Number of input channels.
Paragraph 2.3.3: Regenerated.
Paragraph 3.4: Revised minimum sample rate to 30KSPS.
Paragraph 3.4.4: Updated definition of external output clock.
Paragraph 3.4.4.2, 3.12.2.2: Extended maximum output pulse width from 100ns to 150ns.
Paragraph 3.13.4.1: Revised clock source reference to Rate-C.

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