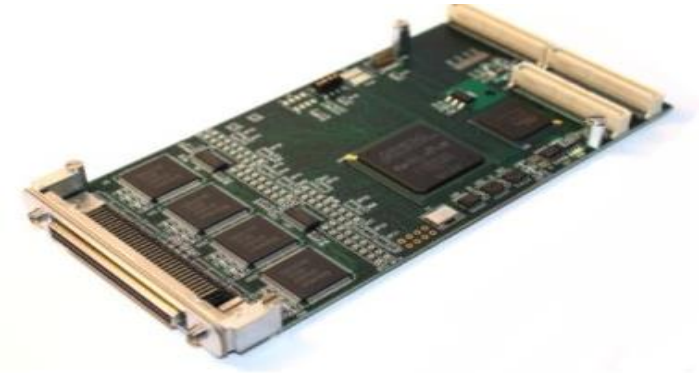
PMC66-SIO4BXR-SPI
User's Manual



RS422 Interface

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Revision C

PREFACE

Revision History

1. Rev NR – Apr 2012 – Original Rev (firmware vB00)
2. Rev A – Apr 2012 – Add Master/Slave selection (firmware vB01)
3. Rev B – May 2012 – Add ProgClk Appendix, misc cleanup (firmware vB02)
4. Rev C – Jan 2022 – Update for latest FW (vB04) and PCB Rev E/F

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RELATED PUBLICATIONS

PLX PCI 9056 Data Book

PLX Technology Inc.
390 Potrero Avenue
Sunnyvale, CA 4085
(408) 774-3735
http://www.plxtech.com/

EIA-422-A – Electrical Characteristics of Balanced Voltage Digital Interface Circuits
(EIA order number EIA-RS-422A)

EIA Standards and Publications can be purchased from:

GLOBAL ENGINEERING DOCUMENTS
15 Inverness Way East
Englewood, CO 80112
Phone: (800) 854-7179
http://global.ihs.com/

PCI Local Bus Specification Revision 2.2 December 18, 1998

Copies of PCI specifications available from:
PCI Special Interest Group
NE 2575 Kathryn Street, #17
Hillsboro, OR 97124
http://www.pcisig.com/

CHAPTER 1: INTRODUCTION

1.0 General Description

The PMC66-SI04BXR-SPI is a custom modification to interface to a SPI device. The PMC66-SI04BXR-SPI board will provide the RS422 differential interface signals of a Master SPI Controller or a generic Slave SPI device.

1.1 SPI Interface (Differential RS422)

SPI_CLK (Active High - Master Output / Slave Input)

Master clock used to transfer data. Clock rate may be from 3MHz down to 25Hz. Output Data will change on the falling edge of the clock, and input data will be clocked on the rising edge.

SPI_CS[3:0] (Active Low – Master Output / Slave Input)

Four Chip select signals which can be are individually enabled. This allows one Master Controller to interface more than one device. The chip select will go low at the beginning of the SPI Word one clock period prior to data clocking, and will remain asserted one clock after the SPI Word has completed.

SPI_MOSI (Active High – Master Output / Slave Input)

Master Out/Slave In Data. . Data is clocked out MSB first.
For a Master Controller, the serial output data will change on the falling edge of the SPI clock.
For a Slave Interface, the serial input data will be clocked in on the rising edge of the SPI clock.

SPI_MISO (Active High – Master Input / Slave Output)

Master In/Slave Out Data. Data is clocked in MSB first.
For a Master Controller, the serial input data will be clocked in on the rising edge of the SPI clock.
For a Slave Interface, the serial output data will change on the falling edge of the SPI clock.

1.2 Spare IO (Differential RS422)

SPARE (Active High Input/Output)

The Spare signal is a general purpose IO signal that may be configured as an input or output. As an input, this signal can be used as an interrupt source.

CHAPTER 2: LOCAL SPACE REGISTERS

2.0 GSC Firmware (Local Space) Registers

The PMC66-SIO4BXR-SPI is accessed through two sets of registers – PCI Registers and GSC Firmware Registers. The GSC Firmware Registers (referred to as Local Space Registers), which provide the control/status for the SIO4BXR-SPI board, are described below. The PCI registers (internal to the PLX 9056 PCI controller) are discussed in Chapter 4.

Offset Address	Size	Access*	Register Name	Default Value (Hex)
0x0000	D32	Read Only	Firmware Revision	E2240BXX
0x0004	D32	Read/Write	Board Control	00000000
0x0008	D32	Read Only	Board Status	000001XX
0x000C	--	--	Reserved	00000000
0x0010	D32	Read/Write	Ch 1 Tx Almost Full/Empty	00070007
0x0014	D32	Read/Write	Ch 1 Rx Almost Full/Empty	00070007
0x0018	D32	Read/Write	Ch l Data FIFO	000000XX
0x001C	D32	Read/Write	Ch 1 Control/Status	0000CC00
0x0020	D32	Read/Write	Ch 2 Tx Almost Full/Empty	00070007
0x0024	D32	Read/Write	Ch 2 Rx Almost Full/Empty	00070007
0x0028	D32	Read/Write	Ch 2 Data FIFO	000000XX
0x002C	D32	Read/Write	Ch 2 Control/Status	0000CC00
0x0030	D32	Read/Write	Ch 3 Tx Almost Full/Empty	00070007
0x0034	D32	Read/Write	Ch 3 Rx Almost Full/Empty	00070007
0x0038	D32	Read/Write	Ch 3 Data FIFO	000000XX
0x003C	D32	Read/Write	Ch 3 Control/Status	0000CC00
0x0040	D32	Read/Write	Ch 4 Tx Almost Full/Empty	00070007
0x0044	D32	Read/Write	Ch 4 Rx Almost Full/Empty	00070007
0x0048	D32	Read/Write	Ch 4 Data FIFO	000000XX
0x004C	D32	Read/Write	Ch 4 Control/Status	0000CC00
0x0050-0x005C	---	--	RESERVED	--------
0x0060	D32	Read/Write	Interrupt Control	00000000
0x0064	D32	Read/Write	Interrupt Status/Clear	00000000
0x0068	D32	Read Only	Interrupt Edge/Level	FFFFFFFF
0x006C	D32	Read/Write	Interrupt High/Low	FFFFFFFF
0x0070-0x007C	---	--	RESERVED	--------
0x0080	D32	Read/Write	Ch 1Pin Source	00000020
0x0084	D32	Read/Write	Ch 2 Pin Source	00000020
0x0088	D32	Read/Write	Ch 3 Pin Source	00000020
0x008C	D32	Read/Write	Ch 4 Pin Source	00000020
0x0090	D32	Read Only	Ch 1Pin Status	000000XX
0x0094	D32	Read Only	Ch 2 Pin Status	000000XX
0x0098	D32	Read Only	Ch 3 Pin Status	000000XX
0x009C	D32	Read Only	Ch 4 Pin Status	000000XX
0x00A0	D32	Read/Write	Prog Osc RAM Addr	00000000
0x00A4	D32	Read/Write	Prog Osc RAM Data (Ch 1-3)	00000000
0x00A8	D32	Read/Write	Prog Osc Control/Status	00000000
0x00AC	D32	Read/Write	Prog Osc RAM Data (Ch 4)	00000000
0x00B0	D32	Read/Write	Ch1 Count / Gap	00000000
0x00B4	D32	Read/Write	Ch2 Count / Gap	00000000
0x00B8	D32	Read/Write	Ch3 Count / Gap	00000000
0x00BC	D32	Read/Write	Ch4 Count / Gap	00000000
0x00C0-CC	D32		Reserved	00000000
0x00D0	D32	Read Only	Ch1 FIFO Count	00000000
0x00D4	D32	Read Only	Ch2 FIFO Count	00000000
0x00D8	D32	Read Only	Ch3 FIFO Count	00000000

0x00DC	D32	Read Only	Ch4 FIFO Count	00000000
0x00E0	D32	Read Only	Ch1 FIFO Size	XXXXXXXX
0x00E4	D32	Read Only	Ch2 FIFO Size	XXXXXXXX
0x00E8	D32	Read Only	Ch3 FIFO Size	XXXXXXXX
0x00EC	D32	Read Only	Ch4 FIFO Size	XXXXXXXX
0x00F0-0x00F4	---	--	RESERVED	--------
0x00F8	D32	Read Only	FW Type Register	0X0X0X0X
0x00FC	D32	Read Only	Features Register	001979F4

2.1 Firmware Revision: Local Offset 0x0000

The Firmware ID register provides version information about the firmware on the board. This is useful for technical support to identify the firmware version.

D31:16	HW Board Rev	0xE224	PMC66-SIO4BXR Rev D
D15:8	Firmware Type ID	0x0B	SPI Firmware
D7:0	Firmware Revision	XX	Firmware Version

2.2 Board Control: Local Offset 0x0004

The Board Control Register defines the general control functions for the board. The main function in this register defines the Demand mode DMA channel requests.

D31 Board Reset
1 = Reset all Local Registers and FIFOs to their default values
Notes: This bit will automatically clear to 0 following the board reset.
Board Reset will NOT reset programmable oscillator.
Following a Board Reset, ResetInProgress bit (D31) of the Board Status Register will remain set until the Board reset is complete;

D30 RESERVED (Debug Test)

D29 FIFO Test
0 = Normal Mode - FIFO Write to Tx FIFO / FIFO Read from Rx FIFO
1 = Test Mode - FIFO Write to Rx FIFO / FIFO Read from Tx FIFO

D28:27 Reserved

D26:24 LED D3-D1
1 = Turn on green LED D1, D2, D3

D23:9 RESERVED

D8 Rx FIFO Stop on Full
1 = If Rx FIFO becomes full, stop receiving data (disable receiver).

D7 Demand Mode DMA Channel 1 Single Cycle Disable

D6:4	Demand Mode DMA Channel 1 Request 000 = Ch1 Rx 100 = Ch1 Tx 010 = Ch2 Rx 110 = Ch2 Tx 001 = Ch3 Rx 101 = Ch3 Tx 011 = Ch4 Rx 111 = Ch4 Tx
D3	Demand Mode DMA Channel 0 Single Cycle Disable
D2:0	Demand Mode DMA Channel 0 Request 000 = Ch1 Rx 100 = Ch1 Tx 010 = Ch2 Rx 110 = Ch2 Tx 001 = Ch3 Rx 101 = Ch3 Tx 011 = Ch4 Rx 111 = Ch4 Tx

2.3 Board Status: Local Offset 0x0008

The Board Status Register gives general overall status for a board. The Board Jumpers (D1:D0) are physical jumpers which can be used to distinguish between boards if multiple SIO4 boards are present in a system.

D31:D6	RESERVED
D5:D4	FIFO Size 11=256K
D3:D0	Board Jumper (J5)
D3	Board ID4 0=J5:7-J5:8 jumper installed
D2	Board ID3 0=J5:5-J5:6 jumper installed
D1	Board ID2 0=J5:3-J5:4 jumper installed
D0	Board ID1 0=J5:1-J5:2 jumper installed

2.4 Channel TX Almost Flags: Local Offset 0x0010 / 0x0020 / 0x0030 / 0x0040

The Tx Almost Flag Registers are used to set the Almost Full and Almost Empty Flags for the transmit FIFOs. The Almost Full/Empty Flags may be read as status bits in the Channel Control/Status Register, and are also edge-triggered interrupt sources to the Interrupt Register.

D31:16 TX Almost Full Flag Value
Number of words from FIFO Full when the Almost Full Flag will be asserted (i.e. FIFO contains{FIFO Size – Almost Full Value} words or more.)
D15:0 TX Almost Empty Flag Value
Number of words from FIFO Empty when the Almost Empty Flag will be asserted.

2.5 Channel Rx Almost Flags: Local Offset 0x0014 / 0x0024 / 0x0034 / 0x0044

The Rx Almost Flag Registers are used to set the Almost Full and Almost Empty Flags for the transmit FIFOs. The Almost Full/Empty Flags may be read as status bits in the Channel Control/Status Register, and are also edge-triggered interrupt sources to the Interrupt Register.

D31:16 RX Almost Full Flag Value
Number of words from FIFO Full when the Almost Full Flag will be asserted (i.e. FIFO contains {FIFO Size – Almost Full Value} words or more.)
D15:0 RX Almost Empty Flag Value
Number of words from FIFO Empty when the Almost Empty Flag will be asserted

2.6 Channel FIFO: Local Offset 0x0018 / 0x0028 / 0x0038 / 0x0048

The Channel FIFO Register passes serial data to/from the serial controller. The same register is used to access both the Transmit FIFO (writes) and Receive FIFO (reads).

D31:8 RESERVED
D7:0 Channel FIFO Data

2.7 Channel Control/Status: Local Offset 0x001C / 0x002C / 0x003C / 0x004C

The Channel Control/Status Register provides the reset functions and data transceiver enable controls, and the FIFO Flag status for each channel.

D31 Master/Slave
0 = Channel will function as SPI Master Controller
1 = Channel will function as SPI Slave Device
D30 CS3 Enable
D29 CS2 Enable
D28 CS1 Enable
D27 CS0 Enable
D26 Stop Tx on Empty
0 = SPI will remain enabled (D25) if Tx FIFO is empty
1 = SPI will be disabled (D25=0) if TX FIFO is empty

D25 SPI Enable

0 = SPI disabled

1 = SPI enabled

D24 RESERVED

D23:20 LED Control

Each Channel controls 2 LEDs on the back of the PCB. See Section 5.3 for more detailed information about the LEDs.

D19 RESERVED

D18:8 Channel Status Bits

D18 Rx FIFO Underflow

D17 Tx FIFO Overflow (Latched)

D16 Rx FIFO Overflow (Latched)

1= Rx Data was lost due to Rx Overflow.

Note: This bit is latched. Write D16=1 to clear.

D15	Rx FIFO Full Flag Lo	(0 = Rx FIFO Full)
D14	Rx FIFO Almost Full Flag Lo	(0 = Rx FIFO Almost Full)
D13	Rx FIFO Almost Empty Flag Lo	(0 = Rx FIFO Almost Empty)
D12	Rx FIFO Empty Flag Lo	(0 = Rx FIFO Empty)
D11	Tx FIFO Full Flag Lo	(0 = Tx FIFO Full)
D10	Tx FIFO Almost Full Flag Lo	(0 = Tx FIFO Almost Full)
D9	Tx FIFO Almost Empty Flag Lo	(0 = Tx FIFO Almost Empty)
D8	Tx FIFO Empty Flag Lo	(0 = Tx FIFO Empty)

D7:0 Channel Control Bits

D7 RESERVED

D6 Reset Channel (Pulsed)

Note: This value will automatically clear to '0'.

D5:D2 RESERVED

D1 Tx FIFO Reset (Pulsed)

Note: This value will automatically clear to '0'.

D0 Rx FIFO Reset (Pulsed)

Note: This value will automatically clear to '0'.

2.8 Interrupt Registers

There are 32 on-board interrupt sources (in addition to PLX interrupts), each of which may be individually enabled. Four interrupt registers control the on-board interrupts – Interrupt Control, Interrupt Status, Interrupt Edge/Level, and Interrupt Hi/Lo. The Interrupt sources are:

IRQ #	Source	Default Level	Alternate Level
IRQ0	Reserved	X	X
IRQ1	Ch1 Tx FIFO Almost Empty	Rising Edge	Falling Edge
IRQ2	Ch1 Rx FIFO Almost Full	Rising Edge	Falling Edge
IRQ3	Ch1 RxSpare	Rising Edge	Falling Edge
IRQ4	Reserved	X	X
IRQ5	Ch2 Tx FIFO Almost Empty	Rising Edge	Falling Edge
IRQ6	Ch2 Rx FIFO Almost Full	Rising Edge	Falling Edge
IRQ7	Ch2 RxSpare	Rising Edge	Falling Edge
IRQ8	Reserved	X	X
IRQ9	Ch3 Tx FIFO Almost Empty	Rising Edge	Falling Edge
IRQ10	Ch3 Rx FIFO Almost Full	Rising Edge	Falling Edge
IRQ11	Ch3 RxSpare	Rising Edge	Falling Edge
IRQ12	Reserved	X	X
IRQ13	Ch4 Tx FIFO Almost Empty	Rising Edge	Falling Edge
IRQ14	Ch4 Rx FIFO Almost Full	Rising Edge	Falling Edge
IRQ15	Ch4 RxSpare	Rising Edge	Falling Edge
IRQ16	Ch1 Tx FIFO Empty	Rising Edge	Falling Edge
IRQ17	Ch1 Tx FIFO Full	Rising Edge	Falling Edge
IRQ18	Ch1 Rx FIFO Empty	Rising Edge	Falling Edge
IRQ19	Ch1 Rx FIFO Full	Rising Edge	Falling Edge
IRQ20	Ch2 Tx FIFO Empty	Rising Edge	Falling Edge
IRQ21	Ch2 Tx FIFO Full	Rising Edge	Falling Edge
IRQ22	Ch2 Rx FIFO Empty	Rising Edge	Falling Edge
IRQ23	Ch2 Rx FIFO Full	Rising Edge	Falling Edge
IRQ24	Ch3 Tx FIFO Empty	Rising Edge	Falling Edge
IRQ25	Ch3 Tx FIFO Full	Rising Edge	Falling Edge
IRQ26	Ch3 Rx FIFO Empty	Rising Edge	Falling Edge
IRQ27	Ch3 Rx FIFO Full	Rising Edge	Falling Edge
IRQ28	Ch4 Tx FIFO Empty	Rising Edge	Falling Edge
IRQ29	Ch4 Tx FIFO Full	Rising Edge	Falling Edge
IRQ30	Ch4 Rx FIFO Empty	Rising Edge	Falling Edge
IRQ31	Ch4 Rx FIFO Full	Rising Edge	Falling Edge

For all interrupt registers, the IRQ source (IRQ31:IRQ0) will correspond to the respective data bit (D31:D0) of each register. (D0 = IRQ0, D1 = IRQ1, etc.)

All FIFO interrupts are edge triggered active high. This means that an interrupt will be asserted (assuming it is enabled) when a FIFO Flag transitions from FALSE to TRUE (rising edge triggered) or TRUE to FALSE (falling edge). For example: If Tx FIFO Empty Interrupt is set for Rising Edge Triggered, the interrupt will occur when the FIFO transitions from NOT EMPTY to EMPTY. Likewise, if Tx FIFO Empty Interrupt is set as Falling Edge Triggered, the interrupt will occur when the FIFO transitions from EMPTY to NOT EMPTY.

All Interrupt Sources share a single interrupt request back to Local Interrupt Input of the PCI9056 PLX chip. This Local Interrupt input must be enabled in the PLX Interrupt Control/Status Register to be recognized as a PCI interrupt source.

2.8.1 Interrupt Control: Local Offset 0x0060

The Interrupt Control register individually enables each interrupt source. A '1' enables each interrupt source; a '0' disables. An interrupt source must be enabled for an interrupt to be generated.

2.8.2 Interrupt Status/Clear: Local Offset 0x0064

The Interrupt Status Register shows the status of each respective interrupt source. If an interrupt source is enabled in the Interrupt Control Register, a '1' in the Interrupt Status Register indicates the respective interrupt has occurred. The interrupt source will remain latched until the interrupt is cleared, either by writing to the Interrupt Status/Clear Register with a '1' in the respective interrupt bit position, or the interrupt is disabled in the Interrupt Control Register. Clearing an interrupt which is not enabled or not asserted will have no effect.

2.8.3 Interrupt Edge/Level: Local Offset 0x0068

The Interrupt Edge Register is an information only (read only) register. This register can be used by a generic driver to determine if the interrupt source is edge or level triggered. All interrupt sources on the SIO4BXR-SYNC are edge triggered.

2.8.4 Interrupt Hi/Lo: Local Offset 0x006C

The Interrupt Edge Register is an information only register which denotes all interrupt sources as edge triggered. The Interrupt Hi/Lo Register define each interrupt source as rising edge or falling edge. For example, a rising edge of the TX Empty source will generate an interrupt when the TX FIFO becomes empty. Defining the source as falling edge will trigger an interrupt when the TX FIFO becomes "NOT Empty".

2.9 Channel Pin Source: Local Offset 0x0080 / 0x0084 / 0x0088 / 0x008C

The Channel Pin Source Register configures the function of the cable interface signals as well as controls the transceiver protocols.

31	30	29	28	27	26	25	24
Cable Xcvr Enable	0	Ext LB Test	0	Transceiver Protocol Mode 0000			

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Int LB Test	00		CLK Idle	0							Spare Src		MISO Test Src		MOSI Test Src			CS Test Src		0	CLK Test Src		

Pin Source Register

D31 Cable Transceiver Enable
0 = Transceivers Tri-Stated
1 = Transceivers Enabled

D30 RESERVED

D29 Ext LB Test External Loopback Test Mode
0 Normal Mode
1 External Master Loopback Test (MISO = !MOSI)

D28 RESERVED

D27:24 Transceiver Protocol Mode
0000 = RS422 / RS485

D23 Int LB Test Internal Loopback Test Mode
0 Normal Mode
1 Internal Master Loopback Test (MISO = MOSI)

D22:21 RESERVED

D20 CLK Idle State 0 = CLK returns low between SPI words
1 = CLK remains high between SPI words

D19:13 RESERVED

D12:11 Spare Control 00 = Disabled (Tri-state)
01 = Input
10 = Output '0'
11 = Output '1'

D10:9 MISO Test 0X = Normal (Input)
10 = Output '0'
11 = Output '1'

D8:6 MOSI Test 0XX = Normal (Output)
110 = Output '0'
111 = Output '1'

D5:4 CS Test 0X = Normal (Output)
10 w/ CS Enabled = Output '0'
10 w/ CS Disabled = Output '1'
11 w/ CS Enabled = Output '1'
11 w/ CS Disabled = Output '0'

D3 RESERVED

D2:0 CLK Test 0X = Normal (Input)
10 = Output '0'
11 = Output '1'

2.10 Channel Pin Status: Local Offset 0x0090 / 0x0094 / 0x0098 / 0x009C

The Channel Pin Status Register allows the input state of all the IO pins to be monitored. Output signals as well as inputs are included to aid in debug operation. As the input signals are inputs from the cable, the transceivers must be enabled before the Inputs are read. Signals denoted "Test" are used in testing to monitor output or drive input signals.

D31:D8 RESERVED

D15	Spare Input
D6	SPI_MISO Input
D5	SPI_MOSI Input
D4	CS3 Input
D3	CS2 Input
D2	CS1 Input
D1	CS0 Input
D0	SPI_CLK Input
D7	Spare Output
D6	SPI_MISO Output
D5	SPI_MOSI Output
D4	CS3 Output
D3	CS2 Output
D2	CS1 Output
D1	CS0 Output
D0	SPI_CLK Output

2.11 Programmable Clock Registers: Local Offset 0x00A0 / 0x00A4 / 0x00A8

The Programmable Clock Registers allow the user to program the on-board programmable oscillator and configure the channel clock post-dividers. As GSC should provide software routines to program the clock, the user should have no need to access these registers. See Section Appendix A for more information.

2.12 Tx Count Register: Local Offset 0x00B0 / 0x00B4 / 0x00B8 / 0xBC

D31:16	Gap Bit Count Number of clocks between SPI words This can be used to ensure CS returns high between SPI words. This field is only used in Master mode.
D15:0	Transmit Bit Count Indicates size of SPI word.

2.13 FIFO Count Register: Local Offset 0x00D0 / 0x00D4 / 0x00D8 / 0x00DC

The FIFO Count Registers display the current number of words in each FIFO. This value, along with the FIFO Size Registers, may be used to determine the amount of data which can be safely transferred without over-running (or under-running) the FIFOs.

D31:D16	Number of words in Rx FIFO
D15:D0	Number of words in Tx FIFO

2.14 FIFO Size Register: Local Offset 0x00E0 / 0x00E4 / 0x00E8 / 0x00EC

The FIFO Size Registers display the sizes of the installed data FIFOs. This value is calculated at power-up This value, along with the FIFO Count Registers, may be used to determine the amount of data which can be safely transferred without over-running (or under-running) the FIFOs. This value is fixed.

D31:D16	Size of installed Rx FIFO
D15:D0	Size of installed Tx FIFO

2.15 FW Type ID Register: Local Offset 0x00F8

This register allows boards to be designed with different functionality on each channel. For example, a board could contain two Standard SIO channels (with Z16C30), and two Raw Synchronous channels. Each byte corresponds to a channel. This register is read only – it reflects the implemented logic.

D31:D24	Channel 4 FW Type – 0B = SPI
D23:D16	Channel 3 FW Type – 0B = SPI
D15:D8	Channel 2 FW Type – 0B = SPI
D7:D0	Channel 1 FW Type – 0B = SPI

2.16 Features Register: Local Offset 0x00FC

The Features Register allows software to account for added features in the firmware versions. Bits will be assigned as new features are added. See Appendix B for more details.

D31:21	RESERVED
D20	1 = No Rx Status byte (std only)
D19:D18	10 = Internal Timestamp (std only)
D17:D16	01 = FPGA Reprogram field
D15:D14	01 = configurable FIFO space
D13	1 = FIFO Test Bit
D12	1 = FW Type Reg
D11:8	Features Rev Level 0x9 = BXR level
D7	1 = Demand Mode DMA Single Cycle Disable feature implemented
D6	1 = Board Reset
D5	1 = FIFO Counters/Size
D4	1
D3:0	Programmable Clock Configuration 0x4 = Two CY22393 - 6 Oscillators

CHAPTER 3: QUICKSTART GUIDE

3.0 Overview

The SPI interface setup is fairly simple. Only a few registers are required to interface to SPI devices.

3.1 Clock

The channel clock should be set to twice the SPI clock. The driver should have a standard clock setup function to set the clock frequency. This should only need to be setup for Master mode as the Slave will use the SPI clock from the cable.

The state of the clock between SPI words can be defined high or low. Bit D20 of the Pin Status Register controls this CLK Idle State. This bit needs to be setup for both Master and Slave.

3.2 Chip Selects

Each channel has 4 chip selects which can be individually enabled. Chip selects can be individually enabled in the Channel Control Status Register (D30:D27). If a single chip select is needed, simply use CS0 and set D27=1. When a Chip Select is not enabled, it will be driven to a high level. Ideally, one CS should be enabled per channel (both Master and Slave).

In Master mode, the chip selects are asserted at the beginning of the cycle one clock period prior to the start of the SPI word transfer, and are asserted one clock after the word completes. The time between words is set by the Gap Bit Count field of the TX Count Register (D31:16). If the Gap value is set below 3, the CS will remain low between SPI word transfers. The Gap field has no effect in Slave mode.

3.3 SPI Word Size

The SPI word size is set in the Transmit Bit Count field of the Tx Count Register (D15:0). This value will define the number of consecutive bits in a SPI word. This should be setup in both Master and Slave mode.

SPI data will be transmitted MSB first. Therefore, if the SPI size is greater than 8 bits, the most significant byte should be written to the Tx FIFO first. Likewise, the Most Significant Byte will be received first in the RX FIFO.

For SPI word size greater than 8 bits, the user will need to ensure the entire word is written to the Tx FIFO before the SPI is enabled (Channel Control/Status Register D25). Otherwise, the SPI word may be broken into 8 bit segments if the Tx FIFO becomes empty.

3.4 Master SPI Controller Setup

- Set Clock to 2x SPI clock frequency.
- Set Pin Source Register – Enable Transceiver (D31=1) and Clk Idle (D20)
- Set Channel Control Status Register - Master (D31=0), CS Enables (D30:D27), and Tx Stop on Idle (D26).
- Set Tx Count Register – Gap and Tx Count = SPI Word Size
- Load Data into Tx FIFO – if Word Size >8, write Most Significant Byte first
- Enable SPI - Channel Control Status Register D25
- As data transmits, MISO data received in Rx FIFO.
- If Tx Stop on Idle Set, Enable SPI will reset when TX FIFO empty.
- Read data from Rx FIFO. Rx FIFO Count will show number of bytes received.

3.5 Slave SPI Setup

- Set Pin Source Register – Enable Transceiver (D31=1) and Clk Idle (D20)
- Set Channel Control Status Register - Slave (D31=1), CS Enables (D30:D27)
- Set Stop On Rx FIFO Full in Board Control Register (D8)
- Set Tx Count Register –Tx Count =SPI Word Size
- Load Data into Tx FIFO – if Word Size >8, Most Significant Byte first
- Enable SPI - Channel Control Status Register D25
- Wait for SPI Controller to send data
- MOSI data received in Rx FIFO.
- If Rx Stop on Full Set, Enable SPI will reset when Rx FIFO full.
- Read data from Rx FIFO. Rx FIFO Count will show number of bytes received.

CHAPTER 4: PCI INTERFACE

4.0 PCI Interface Registers

The PMC/PCI interface is handled by a PCI9056 I/O Accelerator from PLX Technology. The PCI interface is compliant with the 5V, 66MHz 32-bit PCI Specification 2.2. The PCI9056 provides dual DMA controllers for fast data transfers to and from the on-board FIFOs. Fast DMA burst accesses provide for a maximum burst throughput of 264MB/s to the PCI interface. To reduce CPU overhead during DMA transfers, the controller also implements Chained (Scatter/Gather) DMA, as well as Demand Mode DMA.

Since many features of the PCI9056 are not utilized in this design, it is beyond the scope of this document to duplicate the PCI9056 User's Manual. Only those features, which will clarify areas specific to the PMC66-SIO4BXR are detailed here. Please refer to the PCI9056 User's Manual (See Related Publications) for more detailed information. Note that the BIOS configuration and software driver will handle most of the PCI9056 interface. Unless the user is writing a device driver, the details of this PCI Interface Chapter may be skipped.

4.1 PCI Registers

The PLX 9056 contains many registers, many of which have no effect on the SIO4BXR performance. The following section attempts to filter the information from the PCI9056 manual to provide the necessary information for a SIO4BXR specific driver.

The SIO4BXR uses an on-board serial EEPROM to initialize many of the PCI9056 registers after a PCI Reset. This allows board specific information to be preconfigured correctly.

4.1.1 PCI Configuration Registers

The PCI Configuration Registers allow the PCI controller to identify and control the cards in a system.

PCI device identification is provided by the Vendor ID/Device ID (Addr 0x0000) and Sub-Vendor ID/Sub-Device ID Registers (0x002C). The following definitions are unique to the General Standards SIO4BXR boards. All drivers should verify the ID/Sub-ID information before attaching to this card. These values are fixed via the Serial EEPROM load following a PCI Reset, and cannot be changed by software.

Vendor ID	0x10B5	PLX Technology
Device ID	0x9056	PCI9056
Sub-Vendor ID	0x10B5	PLX Technology
Sub-Device ID	0x3198	GSC SIO4BXR

The configuration registers also setup the PCI IO and Memory mapping for the SIO4BXR. The PCI9056 is setup to use PCIBAR0 and PCIBAR1 to map the internal PLX registers into PCI Memory and IO space respectively. PCIBAR2 will map the Local Space Registers into PCI memory space, and PCIBAR3 is unused. Typically, the OS will configure the PCI configuration space.

For further information of the PCI configuration registers, please consult the PLX Technology PCI9056 Manual.

4.1.2 Local Configuration Registers

The Local Configuration registers give information on the Local side implementation. These include the required memory size. The SIO4BXR memory size is initialized to 4k Bytes. All other Local Registers initialize to the default values described in the PCI9056 Manual.

4.1.3 Runtime Registers

The Runtime registers consist of mailbox registers, doorbell registers, and a general-purpose control register. The mailbox and doorbell registers are not used and serve no purpose on the SIO4BXR. All other Runtime Registers initialize to the default values described in the PCI9056 Manual.

4.1.4 DMA Registers

DMA is not used on the PMC66-SIO4BXR-BAE-BIC board.

5. 0 Board Layout

The following figure is a drawing of the physical components of the PMC66-SIO4BXR:

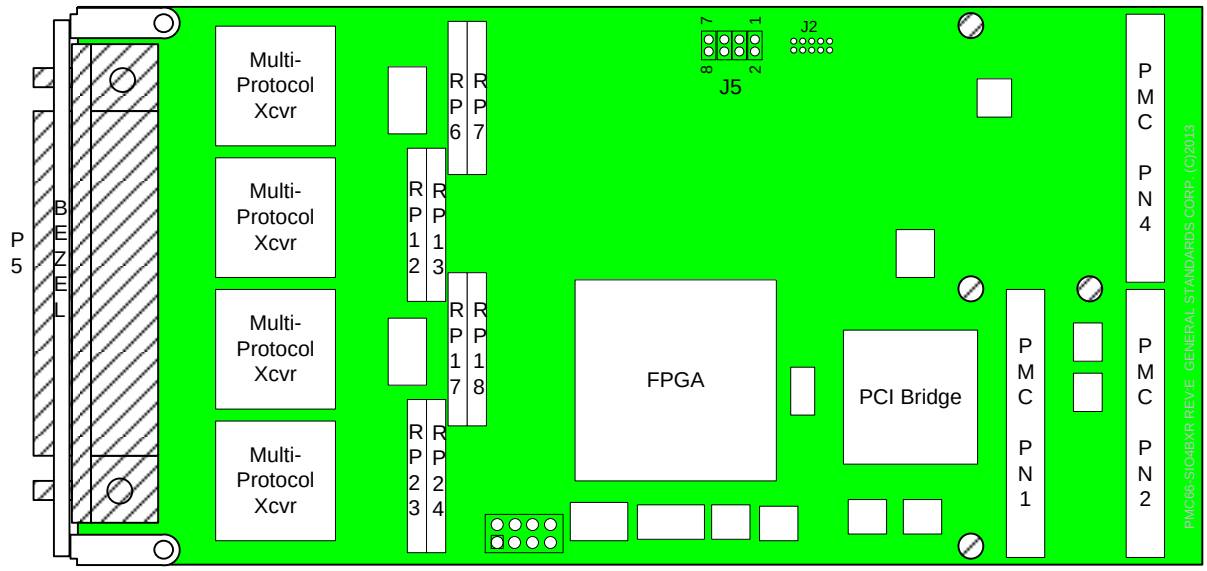

Figure 5-1: Board Layout – Top

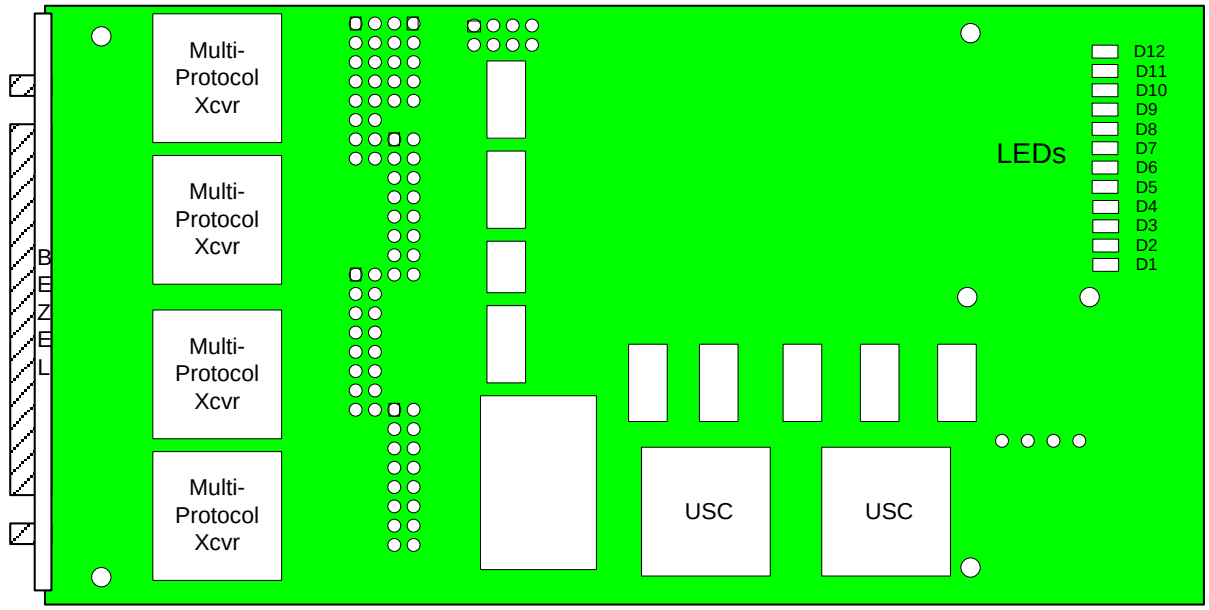

Figure 5-2: Board Layout - Bottom

5.1 Board ID Jumper J5

Jumper J5 allows the user to set the Board ID in the GSC Board Status Register (See Section 2.1.3). This is useful to uniquely identify a board if more than one SIO4BXR card is in a system. When the Board ID jumper is installed, it will read '1' in the Board Status Register. The Board Status Register bit will report '0' when the jumper is removed. Refer to Figure 5-1 for Jumper J5 location.

J5 Jumper	Description	Notes
1 - 2	Board ID 1	Board ID 1 in Board Status Register (D0)
3 - 4	Board ID 2	Board ID 2 in Board Status Register (D1)
5 - 6	Board ID 3	Board ID 3 in Board Status Register (D2)
7 - 8	Board ID 4	Board ID 4 in Board Status Register (D3)

5.2 LEDs

Eleven green LEDs (D2,D3,D4,D5,D6,D7,D8,D9,D10,D11,D12) are accessible via software Refer to Figure 5-2 for these LED locations.

LED_D2 is controlled by Board Control Register D24.
LED_D3 is controlled by Board Control Register D25.
LED_D4 is controlled by Board Control Register D26.

The remaining 8 LEDs are controlled 2 each from D23:D20 of the Channel Control Register. Additionally, if all the LED controls are set to 0 in all four of the Channel Control Registers (power up default), the LEDs will display the lower 6 bits of the firmware revision in LED_D7 to LED_D12

Channel Control Register D23:D20 allow software control of the LEDs. Each Channel Control Register controls 2 LEDs (in order from Ch4 to Ch1). If D23:D22="10", the upper LED will turn off. Likewise, if D23:D22="11", the upper LED will turn on. D21:D20 control the lower LED in the pair.

5.3 Interface Connector

Pin #	DTE Signal	DCE Signal	Pin #	DTE Signal	DCE Signal
1	Ch1_Spare +		35	Ch3_Spare +	
2	Ch1_Spare -		36	Ch3_Spare -	
3	Ch1_SPI_CS3 +		37	Ch3_SPI_CS3 +	
4	Ch1_SPI_CS3 -		38	Ch3_SPI_CS3 -	
5	Ch1_SPI_CS2 +		39	Ch3_SPI_CS2 +	
6	Ch1_SPI_CS2 -		40	Ch3_SPI_CS2 -	
7	Ch1_SPI_CS1 +		41	Ch3_SPI_CS1 +	
8	Ch1_SPI_CS1 -		42	Ch3_SPI_CS1 -	
9	Ch1_SPI_CS0 +		43	Ch3_SPI_CS0 +	
10	Ch1_SPI_CS0 -		44	Ch3_SPI_CS0 -	
11	Ch1_SPI_MISO +		45	Ch3_SPI_MISO +	
12	Ch1_SPI_MISO -		46	Ch3_SPI_MISO -	
13	Ch1_SPI_MOSI +		47	Ch3_SPI_MOSI +	
14	Ch1_SPI_MOSI -		48	Ch3_SPI_MOSI -	
15	Ch1_SPI_Clk +		49	Ch3_SPI_Clk +	
16	Ch1_SPI_Clk -		50	Ch3_SPI_Clk -	
17	GND		51	GND	
18	GND		52	GND	
19	Ch2_SPI_CS2 +		53	Ch4_SPI_CS2 +	
20	Ch2_SPI_CS2 -		54	Ch4_SPI_CS2 -	
21	Ch2_SPI_CS1 +		55	Ch4_SPI_CS1 +	
22	Ch2_SPI_CS1 -		56	Ch4_SPI_CS1 -	
23	Ch2_SPI_CS0 +		57	Ch4_SPI_CS0 +	
24	Ch2_SPI_CS0 -		58	Ch4_SPI_CS0 -	
25	Ch2_SPI_MISO +		59	Ch4_SPI_MISO +	
26	Ch2_SPI_MISO -		60	Ch4_SPI_MISO -	
27	Ch2_SPI_MOSI +		61	Ch4_SPI_MOSI +	
28	Ch2_SPI_MOSI -		62	Ch4_SPI_MOSI -	
29	Ch2_SPI_Clk +		63	Ch4_SPI_Clk +	
30	Ch2_SPI_Clk -		64	Ch4_SPI_Clk -	
31	Ch2_SPI_CS3 +		65	Ch4_SPI_CS3 +	
32	Ch2_SPI_CS3 -		66	Ch4_SPI_CS3 -	
33	Ch2 Spare +		67	Ch4 Spare +	
34	Ch2 Spare -		68	Ch4 Spare -	

Table 5-1: RS422 Cable Pin-Out

The user interface connector for the PCI66-SIO4BXR is a SCSI type 68-pin connector (female) mounted to the front edge of the board (P3).

Part Number: TE Connectivity 787170-7 or 5787170-7

Mating Connector: TE Connectivity 749621-7 or 749111-6 (or equivalent)

CHAPTER 6: ORDERING OPTIONS

6.0 Ordering Information

PMC66-SIO4BXR-SPI ***[Temperature]***

Temperature Option	= Operating Temperature Range	
	<blank>	0° to 70° (Commercial)
	I	-40° to 85° (Industrial)

Please consult our sales department with your application requirements to determine the correct ordering options. (quotes@generalstandards.com).

6.1 Interface Cable

General Standards Corporation can provide off-the-shelf or custom interface cables for the PMC66-SIO4BXR-SPI board. The standard cable is a non-shielded, twisted pair 68-conductor ribbon cable for increased noise immunity. Several standard cable lengths are offered, or the cable length can be custom ordered. Versions of the cable are available with connectors on both ends, or the cable may be ordered with a single connector to allow the user to adapt the other end for a specific application. A standard cable is also available which will breakout the serial channels into four DB25 connectors. Shielded cable options are also available. Please consult our sales department for more information on cabling options and pricing.

6.2 Device Drivers

General Standards has developed many device drivers for the PMC66-SIO4BXR boards, including VxWorks, Windows, Linux, and LabView. As new drivers are always being added, please consult our website (www.generalstandards.com) or consult our sales department for a complete list of available drivers and pricing.

APPENDIX A: PROGRAMMABLE OSCILLATOR PROGRAMMING

The 4 on-baord clock frequencies are supplies via two Cypress Semiconductor CY22393 Programmable Clock Generatosr. In order to change the clock frequencies, this chip must be reprogrammed. This document supplies the information necessary to reprogram the on-board clock frequencies. GSC has developed routines to calculate and program the on-board oscillator for a given set of frequencies, so it should not be necessary for the user need the following information – it is provided for documentation purposes. Please contact GSC for help in setting up the on-board oscillator.

The CY22393 contains several internal address which contain the programming information. GSC has mirrored this data internal to the FPGA (CLOCK RAM) to allow the user to simply setup the data in the FPGA RAM and then command the on-board logic to program the clock chip. This isolates the user from the hardware serial interface to the chip. For detailed CY22393 programming details, please refer to the Cypress Semiconductor CY22393 dat sheet.

For the SIO4BXR, a second programmable oscillator has been added to assure that each channel has a dedicated PLL. (The older SIO4BX uses 3 PLLs in a single CY22393 to generate all four clocks). To implement this, a second CLOCK RAM block was added. CLOCK RAM1 programs the first CY22393 (using CLKA=Ch1_Clk, CLKB=Ch2_Clk, CLKC=Ch3_Clk), and CLOCK_RAM2 programs the second CY22393 (using CLKD=Ch4_Clk). Since the original SIO4BX (with a single CY22393) used CLKD for Ch4_Clk, the same code can be made to support both schemes by simply programming CLKD of the first CY22393.

Each CLOCK RAM block is accessed through 2 registers – Address Offset at local offset 0x00A0 and Data at local ffset at 0x00A4 (CLOCK RAM1) or 0x00AC (CLOCK RAM2). The user simply sets the RAM Address register to the appropriate offset, then reads or writes the the RAM data. The Programmable Osc Control/Status register allows the user to program the CY22393 or setup the clock post-dividers.

The GSC Local Programmable Clock Registers are defined as follows:

0x00A0 – RAM Address Register

Defines the internal CLOCK RAM address to read/write

0x00A4 – RAM Data1 Register

Provides access to the CLOCK RAM1 pointed to by the RAM Addr Register.

0x00AC – RAM Data2 Register

Provides access to the CLOCK RAM2 pointed to by the RAM Addr Register.

0x00A8 – Programmable Osc Control/Status Register

Provides control to write the contents of the CLOCK RAM to the CY22393 and setup additional post-dividers for the input clocks.

Control Word (Write Only)

D0	Program Oscillator 1 = Program contents of CLOCK RAM to CY22393. Automatically resets to 0.
D1	Measure Channel 1 Clock
D2	Measure Channel 2 Clock
D3	Measure Channel 3 Clock
D4	Measure Channel 4 Clock
D5	Reserved (Unused)
D6	Status Word Readback Control 0 => Status Word D31-D8 == Measured Channel Value 1 => Status Word D31-D8 == Control Word D23-D0

D7	Post-divider set 0 = Ignore D23-D8 during Command Word Write 1 = Set Channel Post-Dividers from D23-D8 during Command Word Write
D11-D8	Channel 1 Post-Divider
D15-D12	Channel 2 Post-Divider
D19-D16	Channel 3 Post-Divider
D23-D20	Channel 4 Post-Divider
D31-D24	Reserved (Unused)

Status Word (Read Only)

D0	Program Oscillator Done 0 = Oscillator Programming in progress.
D1	Program Oscillator Error 1 = Oscillator Programming Error has occurred.
D2	Clock Measurement complete. 0 = Clock Measurement in progress.
D7-D3	Reserved (Unused)
D31-D8	If Command Word D6 = 0, Measured Channel Clock Value If Command Word D6 = 1, Control Word D23-D0

Channel Clock Post-Dividers:

The Control Word defines 4 fields for Channel Clock Post-dividers. These post-dividers will further divide down the input clock from the programmable oscillator to provide for slow baud rates. Each 4 bit field will allow a post divider of 2^n. For example, if the post-divider value=0, the input clock is not post-divided. A value of 2 will provide a post-divide of 4 (2^2). This will allow for a post-divide value of up to 32768 (2^15) for each input clock. Bit D7 of the Control word qualifies writes to the post-divide registers. This allows other bits in the command register to be set while the post-divide values are maintained.

Channel Clock Measurement:

The Control Word defines 4 bits which will select one of the 4 channel clocks (input clock + post-divide) for a measurement. This will allow the user feedback as to whether the programmable oscillator was programmed correctly. To measure a clock, select the clock to measure in the Control word, and also clear Bit D6 to allow for readback of the result. Read back the Status Word until D2 is set. Status Word D31-D8 should contain a value representing 1/10 the measured clock frequency (Value * 10 = Measured Frequency in MHz). Keep in mind that this value will not be exactly the programmed frequency due to the 100ppm (0.01%) accuracy of the on-board reference.

The Internal RAM is defined as follows: RAM Address 0x08–0x57 correspond directly to the CY22393 registers.

Address	Description	Default Value
0x00 – 0x05	Reserved (Unused)	0x00
0x06	Reserved	0xD2
0x07	Reserved	0x08
0x08	ClkA Divisor (Setup0)	0x01
0x09	ClkA Divisor (Setup1)	0x01
0x0A	ClkB Divisor (Setup0)	0x01
0x0B	ClkB Divisor (Setup1)	0x01
0x0C	ClkC Divisor	0x01
0x0D	ClkD Divisor	0x01
0x0E	Source Select	0x00
0x0F	Bank Select	0x50
0x10	Drive Setting	0x55
0x11	PLL2 Q	0x00
0x12	PLL2 P Lo	0x00
0x13	PLL2 Enable/PLL2 P Hi	0x00
0x14	PLL3 Q	0x00
0x15	PLL3 P Lo	0x00
0x16	PLL3 Enable/PLL3 P Hi	0x00
0x17	OSC Setting	0x00
0x18	Reserved	0x00
0x19	Reserved	0x00
0x1A	Reserved	0xE9
0x1B	Reserved	0x08
0x1C-0x3F	Reserved (Unused)	0x00
0x40	PLL1 Q (Setup0)	0x00
0x41	PLL1 P Lo 0 (Setup0)	0x00
0x41	PLL1 Enable/PLL1 P Hi (Setup0)	0x00
0x43	PLL1 Q (Setup1)	0x00
0x44	PLL1 P Lo 0 (Setup1)	0x00
0x45	PLL1 Enable/PLL1 P Hi (Setup1)	0x00
0x46	PLL1 Q (Setup2)	0x00
0x47	PLL1 P Lo 0 (Setup2)	0x00
0x48	PLL1 Enable/PLL1 P Hi (Setup2)	0x00
0x49	PLL1 Q (Setup3)	0x00
0x4A	PLL1 P Lo 0 (Setup3)	0x00
0x4B	PLL1 Enable/PLL1 P Hi (Setup3)	0x00
0x4C	PLL1 Q (Setup4)	0x00
0x4D	PLL1 P Lo 0 (Setup4)	0x00
0x4E	PLL1 Enable/PLL1 P Hi (Setup4)	0x00
0x4F	PLL1 Q (Setup5)	0x00
0x50	PLL1 P Lo 0 (Setup5)	0x00
0x51	PLL1 Enable/PLL1 P Hi (Setup5)	0x00
0x52	PLL1 Q (Setup6)	0x00
0x53	PLL1 P Lo 0 (Setup6)	0x00
0x54	PLL1 Enable/PLL1 P Hi (Setup6)	0x00
0x55	PLL1 Q (Setup7)	0x00
0x56	PLL1 P Lo 0 (Setup7)	0x00
0x57	PLL1 Enable/PLL1 P Hi (Setup7)	0x00
0x58-0xFF	Reserved (Unused)	0x00

APPENDIX B: FIRMWARE REVISIONS / FEATURES REGISTER

Since SIO4 boards can exist across multiple form factors and with various hardware features, the firmware/features registers attempt to help identify the exact version of a SIO4 board. This appendix provides a more detailed breakdown of what the firmware and features registers, and detail differences between the firmware revisions.

Firmware Register - Local Offset 0x00 (0xE2250B04)

D31:16 HW Board Rev 0xE225 PMC66-SIO4BXR Rev E/F

- D31 **1** = Features Register Present
- D30 **1** = Complies with this standard
- D29 **1** = 66MHz PCI bus interface
  0 = 33MHz PCI bus interface
- D28 1 = 64 bit PCI bus interface
  0 = 32 bit bus interface
- D27:D24 Form Factor
  - 0 = Reserved
  - 1 = PCI
  - **2** = PMC
  - 3 = cPCI
  - 4 = PC104P
- D23:D20 HW Board (sub-field of form factor)
  - 0 = PMC-SIO4AR
  - 1 = PMC-SIO4BX
  - **2** = PMC66-SIO4BXR
- D19:D16 HW Board Rev (lowest rev for firmware version)
  - 0=NR
  - 1=A,
  - 2=B
  - 3=C
  - **4**=D
  - **5**=E/F

D15:8	Firmware Type ID	0x01	Std Firmware default
		0x04	Sync Firmware default
		0x0B	Spi Firmware (custom)
D7:0	Firmware Revision	XX	Firmware Version

0x00 – Initial Rev (Master Only)
0x01 – Integrate Slave
0x02 – Fix “Tx Stop On Empty” (add syncFF FlowThru), Update clock programming
0x03 – Not Released
0x04 – Update for Rev E/F PCB Rev (no functional changes from vB02)

Feature Register - Local Offset 0xFC

D31:D17	Unused
D16	FPGA Reprogram field Present
D15:D14	configurable fifo space 01 - Rx/Tx select. Up to 32k deep FIFOs
D13	1 = FIFO Test Bit
D12:D8	FW Feature Level (Set at common code level) 0x01 = RS232 support, Pin Source Change 0x02 = Multi-Protocol support 0x03 = Common Internal/External FIFO Support 0x04 = FIFO Latched Underrun/Overrun/Level 0x05 = Demand mode DMA Single Cycle for Tx 0x06 = DMA_Single_Cycle_Dis, updated Pin_Src 0x07 = Rx Underrun Only, Reset Status 0x08 = Clock to 50Hz with 10Hz resolution 0x09 = No Legacy Support (No Clock Control Register)
D7	1 = DMA Single Cycle Disable
D6	1 = Board Reset, FIFO present bits
D5	1 = FIFO Size/Counters present
D4	1 = FW ID complies with this standard
D3:D0	Clock Oscillator 0x0 = Fixed 0x1 = ICD2053B (1 Osc) 0x2 = ICD2053B (4 Osc) 0x3 = CY22393 (4 Osc) 0x4 = 2 x CY22393 (6 Osc)