General Standards Corporation

High Performance Bus Interface Solutions

Rev: 090406

PMC-16AO4MF

16-BIT, FOUR-CHANNEL, MULTIFREQUENCY PMC ANALOG OUTPUT BOARD

REFERENCE MANUAL

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General Standards Corp.
8302A Whitesburg Dr.
Huntsville, Alabama 35802
Telephone: (256) 880-8787
FAX: (256) 880-8788

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SECTION 1.0

INTRODUCTION

1.1 General Description

The PMC-16AO4MF board is a single-width PCI mezzanine card (PMC) that provides precision high-speed analog output capability for the PCI bus. Four 16-bit differential analog output channels provide output ranges of ±5V, ±10V or ±12V, and can be clocked either simultaneously or sequentially at rates up to 400 KSPS (Kilosamples per second) per channel. Each channel is supported by an independent data buffer and rate clock. A bidirectional digital port provides eight digital I/O lines. The board is functionally compatible with the IEEE PCI local bus specification Revision 2.2, and is mechanically and electrically compatible with the IEEE compact mezzanine card (CMC) specification. A PCI interface adapter supports the "plug-n-play" initialization concept.

Power requirements consist of +5 VDC from the PCI bus in accordance with the PCI specification, and operation over the specified temperature range is achieved with conventional convection cooling. Specific details of physical characteristics and power requirements are contained in the PMC-16AO4MFproduct specification. Figure 1.1-1 shows the physical configuration of the board, and the arrangement of major components.

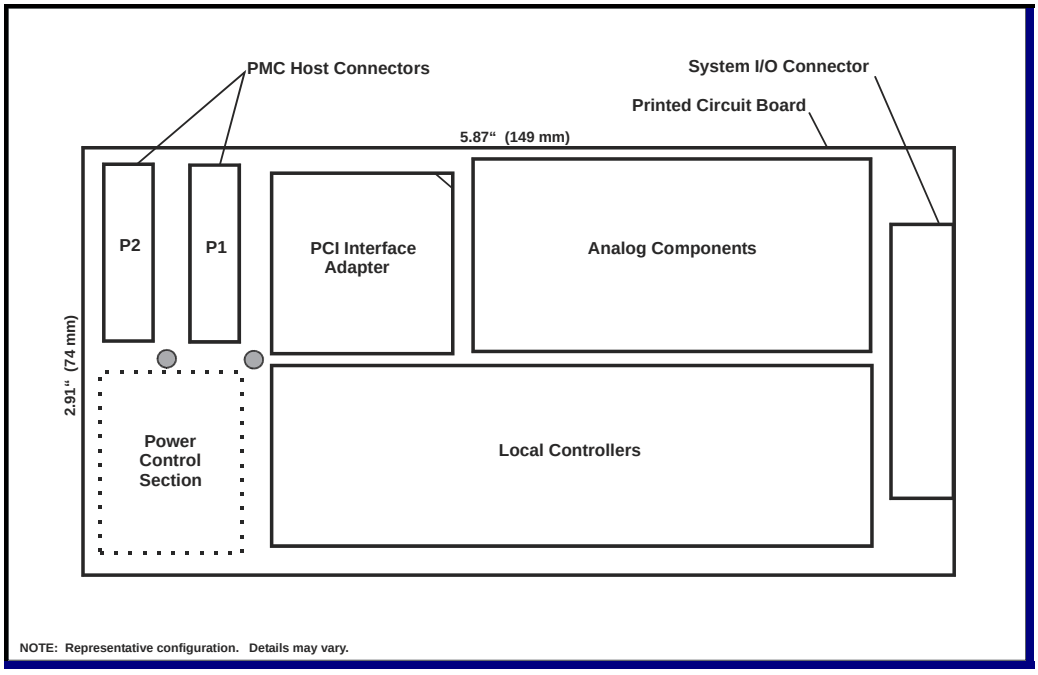

Figure 1.1-1. Physical Configuration

The board is designed for minimum off-line maintenance, and includes internal monitoring and autocalibration features that eliminate the need for disconnecting or removing the module from the system for calibration. All system input and output connections are made through a single 50-pin, dual-ribbon front-access I/O connector. The analog outputs are set to zero-level (midrange) during initialization.

1.2 Functional Overview

Principal capabilities of the PMC-16AO4MF board are summarized in the following list of features.

- Four Differential High-Speed Analog Output Channels
- 16-Bit Resolution; D/A Converter per Channel
- Output Ranges of ±12V, ±10V or ±5V
- Continuous and Triggered-Burst (One-Shot) Clocking Modes
- Data Rate Controlled by Adjustable Internal Clock or by Externally Supplied Clock
- Independent Rate Clock per Analog Output Channel.
- Supports Multiboard Synchronization.
- Internal Autocalibration of all Channels
- Fast Settling; 5 us to 0.1%; 8 us to 0.01%;with No-filter Option
- Bidirectional Byte-Wide Digital Port
- Integral Shield Assures Minimum Susceptibility to Radiated Noise
- Single-width PMC Form Factor.

Figure 1.2-1 outlines the internal functional organization of the board. Each analog output channels is controlled through a dedicated output buffer. Output sample rates can be controlled by internal rate generators, or by an external clock source. Internal selftest networks permit all channels to be calibrated automatically to a single internal voltage reference.

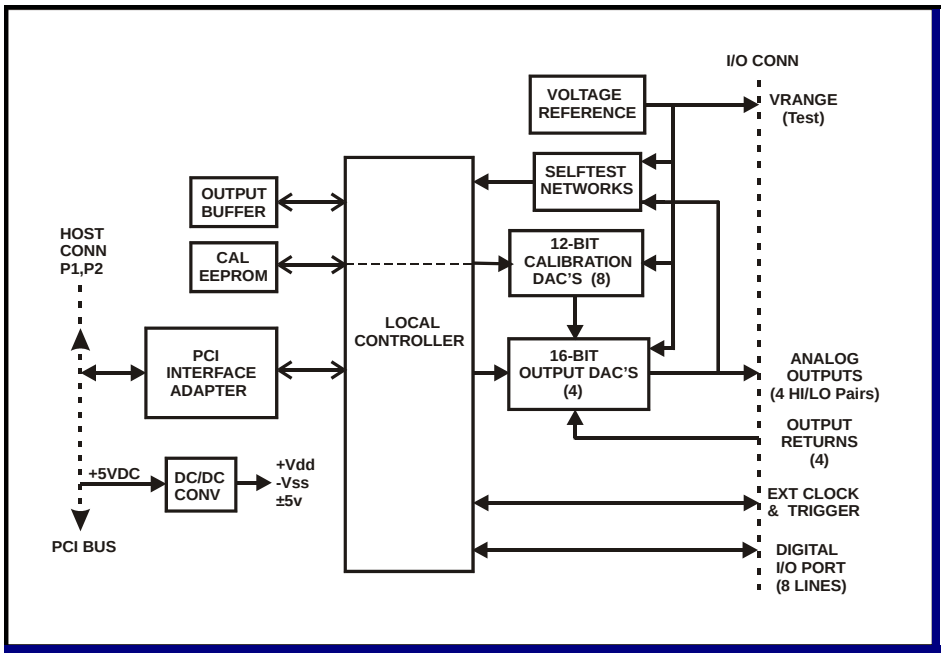

Figure 1.2-1. Functional Organization

Offset and gain trimming of the output D/A converters (DAC's) are performed by 12-bit calibration DAC's. Correction values for the calibration DAC's are determined during autocalibration, and are stored in nonvolatile EEprom for subsequent transfer to the calibration DAC's during board initialization. Autocalibration can be invoked at any time from the PCI bus.

SECTION 2.0

INSTALLATION AND MAINTENANCE

2.1 Board Configuration

This product has no field-alterable configuration features, and is completely configured at the factory for field use.

2.2 Installation

2.2.1 Physical Installation

To minimize the opportunity for accidental damage before installation, the board should be stored in the original protective shipping envelope. System power must be turned OFF before proceeding with the installation.

CAUTION: This product is susceptible to damage from electrostatic discharge (ESD). Before removing the board from the conductive shipping envelope, ensure that the work surface, the installer and the host board have been properly discharged to ground.

After removing the board from the shipping envelope, position the board with the shield and standoffs facing the host (carrier) board, and with the I/O connector oriented toward the front panel. Align the two PCI connectors located at the end of the board opposite the I/O connector with the mating connectors on the host board, and carefully press the board into position on the host. Verify that the PCI connectors have mated completely and that the four standoffs are seated against the host board.

Attach the board to the host with four 2.5 mm screws. Pass the screws through the back of the host into the four mounting holes on the board. Tighten the screws carefully to complete the installation. Do not overtighten.

2.2.2 Input/Output Cable Connections

System cable signal pin assignments are listed in Table 2.2.2-1. I/O connector P5 is designed to mate with a 64-pin dual-ribbon connector, equivalent to Robinson-Nugent #P50-068-DDSTG. This insulation displacement (IDC) cable connector accepts two 34-wire 0.050-inch ribbon cables, with the pin numbering shown in Table 2.2.2-1 and in Figure 2.2.2-1. Contact the factory if preassembled cables are required.

Table 2.2.2-1. System Connector Pin Functions

P5A		P5B	
PIN	SIGNAL	PIN	SIGNAL
1	ANA OUTPUT 00 LO	1	DIGITAL RTN
2	ANA OUTPUT 00 HI	2	DIGIO 00
3	OUTPUT RETURN	3	DIGITAL RTN
4	OUTPUT RETURN	4	DIGIO 01
5	ANA OUTPUT 01 LO	5	DIGITAL RTN
6	ANA OUTPUT 01 HI	6	DIGIO 02
7	OUTPUT RETURN	7	DIGITAL RTN
8	OUTPUT RETURN	8	DIGIO 03
9	VRANGE RETURN	9	DIGITAL RTN
10	VRANGE OUTPUT	10	DIGIO 04
11	VRANGE RETURN	11	DIGITAL RTN
12	OUTPUT RETURN	12	DIGIO 05
13	ANA OUTPUT 02 LO	13	DIGITAL RTN
14	ANA OUTPUT 02 HI	14	DIGIO 06
15	OUTPUT RETURN	15	DIGITAL RTN
16	OUTPUT RETURN	16	DIGIO 07
17	ANA OUTPUT 03 LO	17	DIGITAL RTN
18	ANA OUTPUT 03 HI	18	DIGITAL RTN
19	OUTPUT RETURN	19	DIGITAL RTN
20	OUTPUT RETURN	20	DIGITAL RTN
21	DIGITAL RTN	21	DIGITAL RTN
22	TTL SYNC INP L	22	TTL SYNC OUT L
23	DIGITAL RTN	23	DIGITAL RTN
24	TTL CLK INP L	24	TTL CLK OUT L
25	DIGITAL RTN	25	DIGITAL RTN
26	DIGITAL RTN	26	DIGITAL RTN
27	DIFF SYNC INP LO	27	DIFF SYNC OUT LO
28	DIFF SYNC INP HI	28	DIFF SYNC OUT HI
29	DIGITAL RTN	29	DIGITAL RTN
30	DIGITAL RTN	30	DIGITAL RTN
31	DIFF CLK INP LO	31	DIFF CLK OUT LO
32	DIFF CLK INP HI	32	DIFF CLK OUT HI
33	DIGITAL RTN	33	DIGITAL RTN
34	DIGITAL RTN	34	DIGITAL RTN

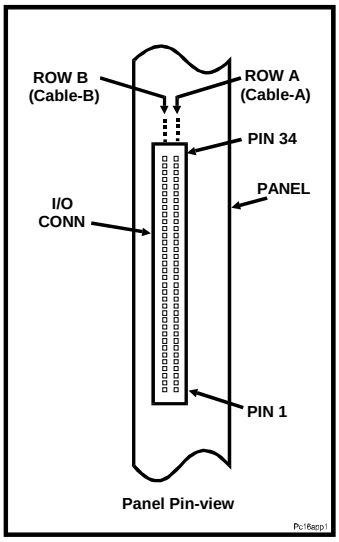

Figure 2.2.2-1. Input/Output Connector

2.3 System Configuration

2.3.1 Output Considerations

2.3.1.1 Line Losses

The voltage drop in ribbon cable can be a significant source of error in 16-bit systems, even with relatively short cables driving low-current loads. Figure 2.3.1-1 shows the effect of load current on the voltage drop in copper wire of various sizes. A 2.0 milliamp load for example, will insert a voltage drop of approximately 130 microvolts *per foot* in conventional #28 AWG ribbon cable; twice that if the return line also is considered. Several feet of ribbon cable therefore can produce significant errors in a 16-bit system, in which one LSB may represent only 153 microvolts (±5 Volt range). High impedance loads, however, generally will not produce significant DC line loss errors.

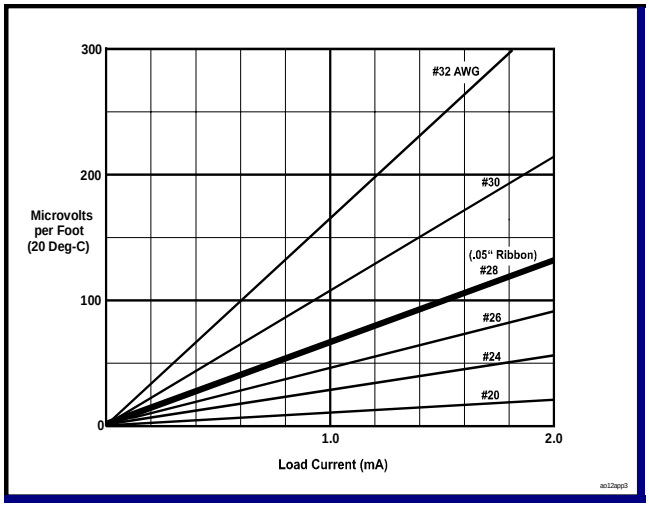

Figure 2.3.1-1. Line Loss versus Load Current

2.3.1.2 Output Configuration

Each output channel of the PMC-16AO4MFis configured as a balanced differential true/complement output triplet, as shown in Figure 2.3.1-2. The output signal appears between the HI and LO lines, and the two output levels are balanced around the output return. The sum of the two outputs is approximately zero, with the actual sum representing the common mode offset.

The load can be isolated from output return, as shown in the figure, or can be balanced around the output return. If an external connection to a remote ground is used, and if the remote ground is at a potential significantly different from that of output return, the resistance **Rgnd** of the connection must be high enough to prevent destructive currents **Ignd** from developing between the grounds.

Figure 2.3.1-2 shows the primary sources of error in a typical installation. The principal source of DC error usually is the voltage drop **Vline** that is present in both the HI and LO connections to the load. The two line resistances **Rline** form a voltage divider with the load resistance **Rload**, and the voltage delivered to the load is a result of the divider network.

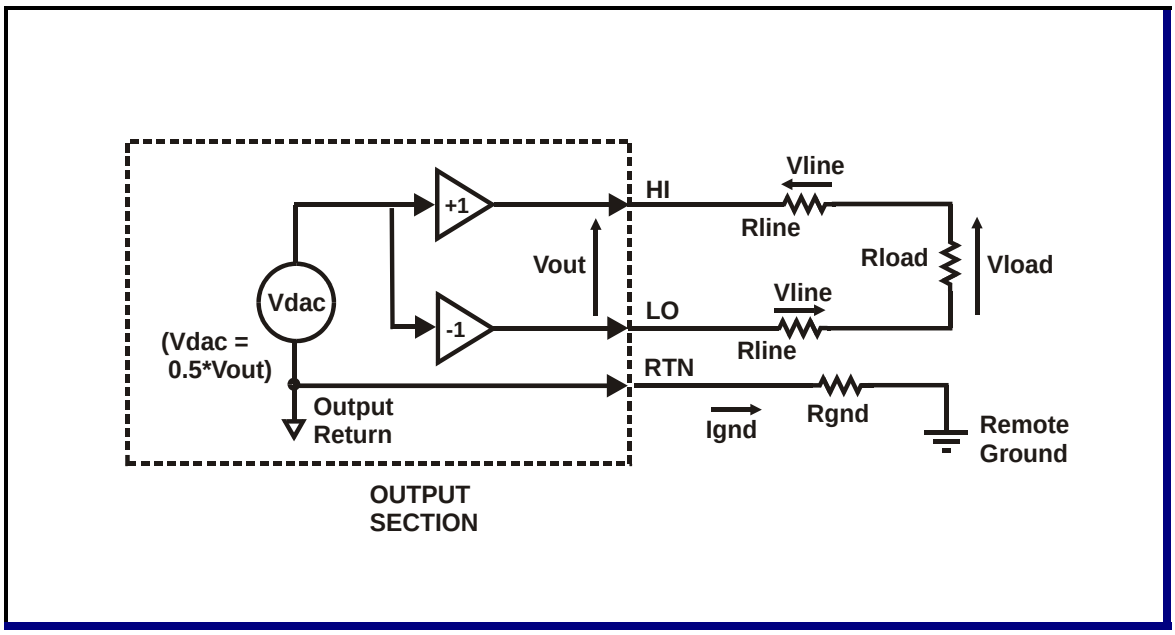

Figure 2.3.1-2. Output Configuration

2.3.2 Sample Clock Input

When external clocking is selected by the control software, the analog outputs are updated at the rate present at the TTL CLK INP L pin if TTL sync is software-selected, or at the DIFF CLK INP HI/LO pair if TTL sync is not selected. The clock input is active on a HIGH-to-LOW transition. The external clock frequency should not exceed the maximum sample rate that is specified for the board.

If the differential sync is selected (TTL sync deselected), the sync and clock inputs and outputs are Low Voltage Differential Signaling (LVDS) levels. Pins designated as "HI" in Table 2.2.2-1 are noninverted signals, and the "LO" inputs are inverted.

Sync and clock inputs are disabled if the board is software-configured as an initiator.

2.3.3 Burst Sync Input

If burst triggering is enabled by the control software, an external signal can initiate a data burst by applying a HIGH-to-LOW transition at the TTL SYNC INP L (TTL sync selected) or DIFF SYNC-INP-HI/LO (TTL sync deselected) pins in the I/O connector. In order for the sync input to be acknowledged by the board, the sync output signal must be HIGH. Sync output is LOW during a burst, and is HIGH between bursts.

2.3.4 Multiboard Synchronization

2.3.4.1 Synchronized Bursts

If multiple boards are to be burst-synchronized together, the SYNC OUT from one board, the *burst-initiator*, is connected to the associated TTL or LVDS SYNC INP pins of a group *of burst-targets* (Figure 2.3.4-1). Each burst-target, when operated in the triggered-burst mode, will initiate a single burst from its buffer each time the burst-initiator initiates a burst. The initiator can be configured for either continuous or burst operation.

2.3.4.2 Synchronized Clocks

To clock-synchronize multiple boards together, the CLOCK OUTPUT from one board, designated the *clock-initiator*, is connected to the CLOCK INPUT of one or *more clock-target* boards. The clock-targets are software-configured for external clocking, and the initiator is configured for internal clocking.

2.4 Digital I/O Port

Digital I/O lines DIGIO 00-07 comprise a byte-wide bidirectional port. The eight lines are software-configured as an input or output port, and are TTL-compatible. Source/sink capability is 20 ma. All digital lines are referred to DIGITAL RTN.

MCLK00 and MCLK01 are factory test outputs and should be left disconnected.

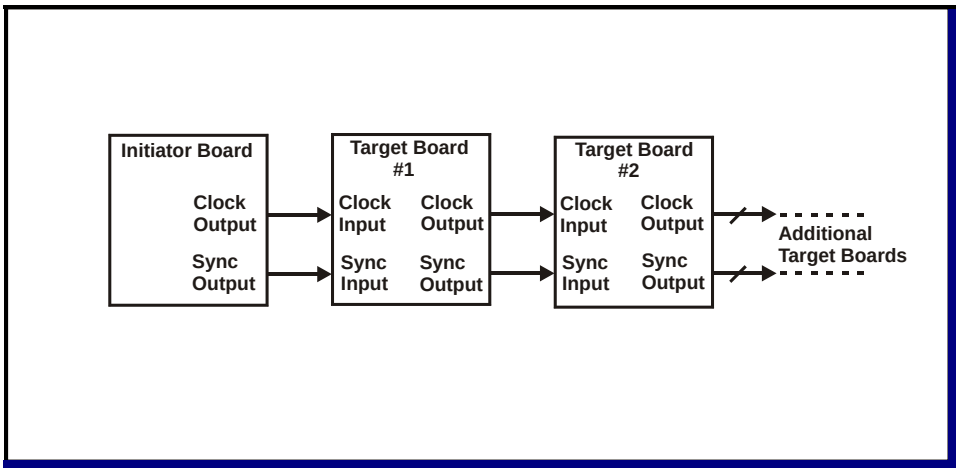

Figure 2.3.4-1. Multiboard Synchronization

2.5 Maintenance

This product requires no scheduled hardware maintenance other than periodic reference verification. The optimum verification interval will vary depending upon the specific application, but in most instances an interval of one year is sufficient.

In the event of a suspected malfunction, all associated system parameters, such as power voltages, control bus integrity, and input signal levels, should be evaluated before troubleshooting of the board itself is attempted. If surface-mount repair capability is not available, a board that is suspected to be defective should be returned to the factory for problem analysis and repair.

2.6 Reference Adjustment

All output channels are software-calibrated to an internal voltage reference (Vrange) by an embedded autocalibration software utility. The procedure presented here describes the adjustment of the reference. For applications in which the system must not be powered down, the board can be calibrated under normal operating conditions while installed on the existing host board.

2.6.1 Equipment Required

Table 2.6.1-1 lists the minimum equipment requirements for calibrating the PMC-16AO4MFboard. Alternative equivalent equipment may be used.

Table 2.6.1-1. Calibration Equipment

EQUIPMENT DESCRIPTION	MANUFACTURER	MODEL
Digital Multimeter, 5-1/2 digit, 0.005% accuracy for DC voltage measurements at ±10 Volts.	Hewlett Packard	34401A
Host board with single-width PMC adapter	(Existing host)	---

2.6.2 Adjustment Procedure

The following procedure describes the single adjustment that is necessary to ensure conformance to the product specification.

Adjustment of the internal reference (Vrange) is performed with an internal trimmer that is accessible as indicated in Figure 2.6.2-1. Any adjustment seal on the trimmer should be removed before beginning the procedure, and the trimmer should then be resealed with a suitable sealing agent after calibration has been completed.

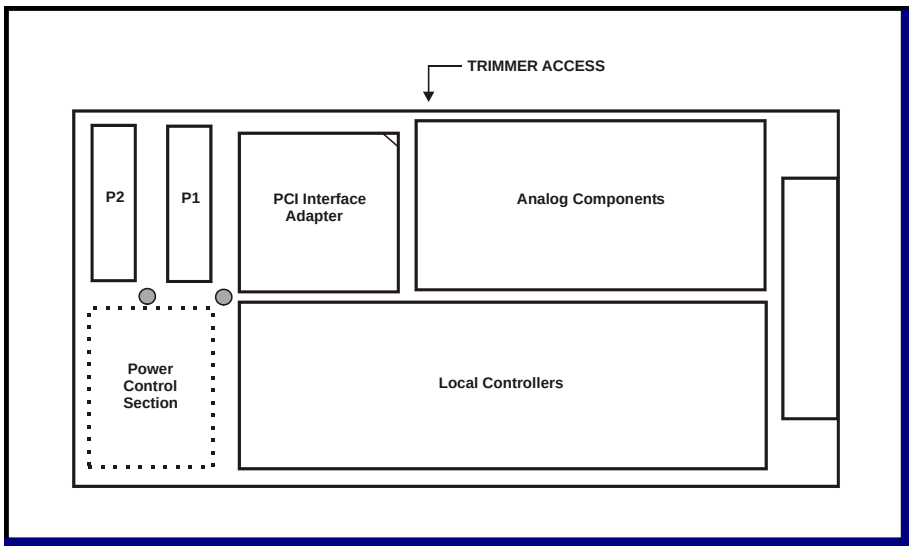

Figure 2.6.2-1. Trimmer Access

This procedure assumes that the board to be calibrated is installed on a host board, and that the host is installed in an operating system. The board can be operating in any mode when the adjustment is performed.

1. Connect the digital multimeter between the VRANGE OUTPUT (+) and VRANGE RETURN (-) pins in the system I/O connector. Refer to Table 2.2.2-1 for pin assignments.
2. If power has been removed from the board, apply power now and wait at least 15 minutes before proceeding.

3. Adjust the REFERENCE ADJUSTMENT trimmer until the digital multimeter indication is within the appropriate range listed in the following table:

OUTPUT VOLTAGE RANGE	MULTIMETER INDICATION (DC Volts)
±12 Volts	+5.9940 ±0.0011
±10 Volts	+4.9950 ±0.0009
± 5 Volts	+2.4975 ±0.0005

4. Calibration is complete. Remove all test connections.

SECTION 3.0

CONTROL SOFTWARE

3.1 Introduction

Each of the four analog PMC-16AO4MFoutput channels is controlled through a dedicated set of control registers, as shown in Tables 3.1-1 and 3.1-2. The four sets of registers are essentially identical, with the exception of the diagnostic and digital byte port control registers that are provided in Channel-00 space. Control of the PMC-16AO4MFis derived from that of the PMC-16AO12 board, and retains all of the register functions of that board with the following exceptions:

- The original Channel Selection register at offset 04h is now a reserved register for Channel-01, and the digital byte port in Channel-00 space,
- Three control bits in each BCR now have new or altered functions,
- An Alternate Rate Select register has been added for each channel,
- Definition of initiator and target has been modified (Section 3.4.5).

The register set for each output channel is referred to throughout this section as a virtual "board", in order to provide maximum similarity with existing PMC-16AO12 applications. Each channel is controlled independently of the other channel, including initialization, autocalibration and data buffer functions.

The PCI interface is controlled by a PLX^{TM} PCI-9080 I/O accelerator device. Configuration-space registers are initialized internally to support the location of the board on any 32-longword boundary in memory space. All data transfers are long-word D32, and only the lower 20 bits are active. Any of the predefined operational conditions identified throughout this section can invoke a single interrupt request from the board. DMA access is supported for data transfers to four independent analog output buffers.

3.2 Board Control Registers

As Tables 3.2-1 and 3.2-2 indicate, each BCR consists of 16 control bits and status flags. Specific control bits are cleared automatically after the associated operations have been completed. Control and monitoring functions of the BCR are described in detail throughout the remainder of this section.

3.3 Configuration and Initialization

3.3.1 Board Configuration

During *board configuration*, initial values for both the PCI configuration registers and the internal control logic are extracted from internal nonvolatile read-only memory. This process is initiated by a PCI bus reset, and is required only once after the initial application of power. While the PCI configuration registers are being loaded, the response to a PCI target access attempt is RETRY's. Configuration operations are executed in the sequence shown in Table 3.3.1-1.

Table 3.1-1. Channel-00 Control and Data Registers

OFFSET	REGISTER	ACCESS MODE*	DEFAULT	PRIMARY FUNCTION
00	BOARD CONTROL (BCR)	R/W	0 0810h	Channel-00 Board Control Register (BCR)
04	DIGITAL BYTE PORT	R/W	0 00XXh	Digital I/O lines control
08	SAMPLE RATE	R/W	0 005Ah	Channel-00 clocking rate divisor
0C	BUFFER OPERATIONS	R/W	0 340Dh	Channel-00 Buffer size selection
10	** Firmware Revision	RO	0 XXXXh	**
14	** Autocal Diagnostics	RO	0 0XXXh	**
18	OUTPUT DATA BUFFER	WO	X XXXXh	Channel-00 analog output FIFO buffer
1C	ADJUSTABLE CLOCK	R/W	0 0000h	Channel-00 adjustable clock.
20	INTERNAL CLOCK SOURCE	R/W	0 0000h	Channel-00 internal clock source
24	** Master clock freq trim	RO	0 09C4h	**
28-3F	(Reserved)	RO	X XXXXh	---

* Access mode is D32, with 17 active bits. R/W = Read/Write; RO= Read-only; WO = Write-only.
** Diagnostic/maintenance registers. Included here for reference only..

Table 3.1-2. Channel-01, 02, 03 Control and Data Registers

OFFSET						
Ch 1	Ch 2	Ch 3	REGISTER	ACCESS MODE*	DEFAULT	PRIMARY FUNCTION
40	80	C0	BOARD CONTROL (BCR)	R/W	0 0810h	Channel-01 Board Control Register
44	84	C4	(Reserved)	RO	0 0000h	---
48	88	C8	SAMPLE RATE	R/W	0 005Ah	Channel clocking rate divisor
4C	8C	CC	BUFFER OPERATIONS	R/W	0 340Dh	Channel Buffer size selection
50	90	D0	** Firmware Revision	RO	0 XXXXh	**
54	94	D4	** Autocal Diagnostics	RO	0 0XXXh	**
58	98	D8	OUTPUT DATA BUFFER	WO	X XXXXh	Channel analog output FIFO buffer
5C	9C	DC	ADJUSTABLE CLOCK	R/W	0 0000h	Channel adjustable clock.
60	A0	E0	INTERNAL CLOCK SOURCE	R/W	0 0000h	Channel internal clock source
64-7F	A4-BF	E4-FF	(Reserved)	RO	X XXXXh	---

* Access mode is D32, with 17 active bits. R/W = Read/Write; RO= Read-only; WO = Write-only.
** Diagnostic/maintenance registers. Included here for reference only.

Board configuration terminates with the PCI interrupts disabled. Attempts to access the local bus during configuration should be avoided until the PCI interrupts are enabled and the initialization-complete interrupt request is asserted as described in Section 3.6.

Loading of the PCI configuration registers is completed within 3 milliseconds or less after the assertion of a PCI bus reset, and should be required only once after the initial application of power. PCI register configuration terminates with the PCI interrupts disabled (Paragraph 3.6).

Table 3.2-1. Channel-00 Board Control Register

Offset: 0000h **Default: 0000 0810h**

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00	R/W	BURST ENABLED	0	Selects burst-mode if HIGH, continuous-mode if LOW. Default is LOW; i.e. continuous-mode.
D01	RO	BURST READY	0	If HIGH, indicates that a burst trigger (sync) will be accepted. If LOW, indicates that a burst is in progress, and that a trigger will not be accepted. Available as an interrupt condition.
D02	R/W	*BURST TRIGGER	0	Software burst trigger, asserted HIGH. Active only when BURST ENABLED control bit is asserted. Initialized LOW.
D03	RO	GLOBAL AUTOCAL FAIL	0	High if any channel fails autocalibration.
D04	R/W	OFFSET BINARY	1	Selects offset-binary data format when asserted HIGH, or two's complement when LOW.
D05	R/W	TTL SYNC I/O	0	Selects the external TTL clock and sync inputs when HIGH, or the differential clock and sync inputs when LOW.
D06	R/W	* GLOBAL AUTOCAL	0	Initiates autocalibration of all four channels.
D07	R/W	COMMON RATE GEN	0	Selects the Channel-01 rate generator for Channel-00 clocking when HIGH, or the Channel-00 rate generator when LOW. Active only in initiator mode.
D08	R/W	INTERRUPT A0	0	Interrupt source selection.
D09	R/W	INTERRUPT A1	0	
D10	R/W	INTERRUPT A2	0	
D11	R/W	INTERRUPT REQUEST FLAG	1	Set HIGH when Channel-00 asserts an interrupt request. Clears the request when cleared LOW by the bus.
D12	R/W	*CM0	0	Calibration mode. Defaults to normal operation.
D13	R/W	*CM1	0	Completion available as an interrupt condition.
D14	RO	BIT STATUS FLAG	0	Records the status of channel autocalibration; LOW for pass, HIGH for fail. Initializes LOW.
D15	R/W	*INITIALIZE	0	Initializes the board when set HIGH. Sets all defaults for all registers.

* Cleared automatically when operation is completed. R/W = Read/Write; RO=Read-Only.

Table 3.2-2. Channel-01, 02, 03 Board Control Registers

Offset: Chan-1: 0040h, Chan-2: 0080h, Chan-3: 00C0h
Default: 0000 0810h

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00	R/W	BURST ENABLED	0	Selects burst-mode if HIGH, continuous-mode if LOW. Default is LOW; i.e. continuous-mode.
D01	RO	BURST READY	0	If HIGH, indicates that a burst trigger (sync) will be accepted. If LOW, indicates that a burst is in progress, and that a trigger will not be accepted. Available as an interrupt condition.
D02	R/W	*BURST TRIGGER	0	Software burst trigger, asserted HIGH. Active only when BURST ENABLED control bit is asserted. Initialized LOW.
D03	RO	(Reserved)	0	---
D04	R/W	OFFSET BINARY	1	Selects offset-binary data format when asserted HIGH, or two's complement when LOW.
D05	R/W	TTL SYNC I/O	0	Selects the external TTL clock and sync inputs when HIGH, or the differential clock and sync inputs when LOW.
D06	R/W	(Reserved)	0	---
D07	R/W	COMMON RATE GEN	0	Selects the Channel-00 rate generator for Channel-X clocking when HIGH, or the Channel-X rate generator when LOW. Active only in initiator mode. ("X" is 1, 2 or 3).
D08	R/W	INTERRUPT A0	0	Interrupt source selection.
D09	R/W	INTERRUPT A1	0	
D10	R/W	INTERRUPT A2	0	
D11	R/W	INTERRUPT REQUEST FLAG	1	Set HIGH when Channel-01 board asserts an interrupt request. Clears the request when cleared LOW by the bus.
D12	R/W	*CM0	0	Calibration mode. Defaults to normal operation.
D13	R/W	*CM1	0	Completion available as an interrupt condition.
D14	RO	BIT STATUS FLAG	0	Records the status of channel autocalibration; LOW for pass, HIGH for fail. Initializes LOW.
D15	R/W	*INITIALIZE	0	Initializes the board when set HIGH. Sets all defaults for all registers.

* Cleared automatically when operation is completed. R/W = Read/Write; RO=Read-Only.

Table 3.3.1-1. Configuration Operations

Operation	Maximum Duration
PCI configuration registers are loaded from internal ROM	3 ms
Internal control logic is configured from internal ROM	300 ms
Internal control logic and rate generators are initialized	200 ms

3.3.2 Initialization

Internal control logic can be initialized without invoking PCI reconfiguration by setting the INITIALIZE control bit HIGH in the BCR. This action causes the internal logic to be initialized, but does not affect the PCI configuration registers and does not reconfigure the internal control logic. Initialization requires 200 milliseconds or less for completion, and produces the following default conditions:

- All four BCR's are initialized; all defaults are invoked
- Analog output buffers are reset to empty
- Analog output levels are set to zero (midrange)
- Buffer configuration is open, with maximum size selected
- Data coding format is offset binary
- Internal clocking is selected at 300 KSPS
- Clocking mode is continuous
- Clocking is disabled
- Adjustable clock generators are adjusted to 16 MHz
- Calibration D/A converters are initialized with correction values from internal EEproms
- The eight digital I/O lines are configured as an input port
- The local interrupt request is asserted (ignored unless PCI interrupts are enabled)

Upon completion of initialization, the INITIALIZE control bit is cleared automatically.

3.4 Analog Output Control

This section describes those operations that control the movement of data from the PCI bus through the analog output buffer. These functions include the organization of data within the buffer and the clocking of data from the buffer to the analog outputs. The principal parameters associated with controlling the analog output channels are summarized below in Table 3.4-1. Section 3.8 provides detailed examples of analog output operations.

Table 3.4-1. Summary of Output Control Parameters

Parameter	Mode	Description
Data Control	Data Frame	All sample values in an output function comprise a *Data Fr*ame.
	Data Coding	Output data can be coded either in offset-binary format or in two's complement format.
Active Buffer	Size Selection	The active buffer is a subset of the physical output data buffer. Active buffer size is determined by the SIZE[3..0] control-bit field in the buffer operations register.
	Status Flags	Status flags buffer-empty, buffer-low-quarter, buffer-high-quarter and buffer-full are provided for the active buffer.
Buffer Configuration	Open	Data read from the buffer is used and then discarded, until the buffer is empty.
	Circular (closed)	Data within the buffer is recirculated. Each value read from the output of the buffer FIFO is written back to the input of the FIFO. An end-of-frame (EOF) flag tracks the movement of data through the buffer.
Clock Source	External	External hardware provides the sample clock.
	Internal	The sample clock is provided by an internal rate generator.
Sampling Mode	Continuous	The contents of the output buffer are sampled continuously at the selected clock rate.
	Triggered Burst	A single data frame in the buffer is clocked to the outputs.

3.4.1 Data Organization

3.4.1.1 Data Loading

Analog output data is loaded into each output buffer as sequential values for the associated output channel. Loading can be accomplished either with direct single-writes to a buffer, or through a DMA transfer (Section 3.9).

3.4.1.2 Data Frame

A *data frame, or burst,* is a sequence of output values that has a tagged final value. The final value is identified as the *end-of-frame* (EOF) by setting the EOF flag (D16) HIGH when loading the last value into the buffer. Thereafter, the EOF flag accompanies the last value through the buffer.

Multiple data frames can be loaded contiguously into a buffer. If bursting is enabled, each sync command (trigger) initiates the clocking of a single data frame from the buffer.

3.4.1.3 Output Data Format

3.4.1.3.1 Output Data Buffer

Analog output data values for each channel are written in word-serial sequence from the PCI bus to the associated Output Data Buffer register shown in Table 3.4.1-2. Bits D15..0 represent the output data value. Bit D16 is set HIGH to indicate the last value in a data frame, and is the end-of-frame (EOF) flag. Bits D31..17 are inactive and have no effect. Access to the output buffer is supported for both single-longword transfers and single-address multiple-longword DMA transfers.

Table 3.4.1-2. Output Data Buffers

Offset: Chan-0: 0018h, Chan-1: 0058h, Chan-2: 0098h, Chan-3: 00D8h
Default: 000X XXXXh

DATA BIT	MODE*	DESIGNATION	DESCRIPTION
D00	WO	**DATA00**	Least significant data bit
D01-D14	WO	**DATA01 - DATE14**	Intermediate data bits
D15	WO	**DATA15**	Most significant data bit
D16	WO	**EOF FLAG**	End-of-frame (EOF) flag.
D17-D31	WO	**---**	(Inactive)

* WO indicates write-only access. Read-access returns an all-zero value.

3.4.1.3.2 Output Data Coding

Analog output data can be coded either in 16-bit offset binary format by asserting the OFFSET BINARY control bit HIGH in the BCR, or in two's complement format by clearing the control bit LOW (Table 3.4.1-3). Analog output data transactions are D32 (32 bits), but the data significance is 16 bits.

Table 3.4.1-3. Output Data Coding; D15..0

ANALOGOUTPUT LEVEL	DIGITAL VALUE (Hex)	
	OFFSET BINARY	TWO'S COMPLEMENT
Positive Full Scale minus 1 LSB	XXXX FFFF	XXXX 7FFF
Zero plus 1 LSB	XXXX 8001	XXXX 0001
Zero	XXXX 8000	XXXX 0000
Zero minus 1 LSB	XXXX 7FFF	XXXX FFFF
Negative Full Scale plus 1 LSB	XXXX 0001	XXXX 8001
Negative Full Scale	XXXX 0000	XXXX 8000

Positive Full Scale is a positive level that equals the range option defined for the board (e.g.: +5.000 Volts for the ±5V option). *Negative Full Scale* is the negative equivalent of positive full-scale. *Full-scale Range* (FSR) is the total voltage range for the output channel . One LSB equals the full-scale range divided by 65,536. (e.g.: 152.59 microvolts for the ±5V option).

3.4.2 Output Buffer

The *physical output buffer* for each output channel consists of a 17-bit wide FIFO that has a capacity of 32K output values. Each output value is 16 bits wide and occupies a single location within the FIFO. The 17th bit is an end-of-frame flag that is attached to the last value in a data frame. Data values are transferred from the PCI bus to the analog output channels through an *active buffer*, which is a subset of the physical buffer.

3.4.2.1 Buffer Operations Registers

The *buffer operations registers* (BOR) control the configurations of the four output buffers, as well as related functions such as clocking and loading. The BOR (Table 3.4.2-1) is 16 bits wide and resides at relative offset 0Ch for Channel-00, and at 4Ch for Channel-01.

3.4.2.2 Active Buffer

An *active buffer* is a virtual buffer that represents a subset of the physical buffer for one of the four output channels, and which is the working buffer through which all output data flows. The size of the active buffer is adjustable from a minimum of four samples up to the full size of the physical buffer. The buffer can be cleared to the empty state by setting the CLEAR BUFFER control bit HIGH in the buffer operations register. CLEAR BUFFER clears automatically after the reset operation has been completed.

Note: Data loss may occur if the buffer is allowed to fill completely.

The active buffer performs exactly like a physical buffer of the same size. That is, a full buffer will accept no further data from the bus, and an empty buffer indicates that all outputs are idle. Buffer status flags (empty, low-quarter, high-quarter and full) respond to the size of the *active buffer*, not to the size of the physical buffer.

Table 3.4.2-1. Buffer Operations Registers

Offset: Chan-0: 000Ch, Chan-1: 004Ch, Chan-2: 008Ch, Chan-3: 00CCh
Default: 0000 340Dh

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00	R/W	SIZE0	1	Size-selection bit field for the active buffer.
D01	R/W	SIZE1	0	Defaults to Dh (32K Samples).
D02	R/W	SIZE2	1	
D03	R/W	SIZE3	1	
D04	R/W	EXTERNAL CLOCK	0	Selects hardware or software clock source when HIGH, or the internal rate generator when LOW. Default is LOW (internal rate generator).
D05	R/W	ENABLE CLOCK	0	Enables output clocking when HIGH. Disables clocking when LOW. Default is LOW (clocking disabled).
D06	RO	CLOCK READY	0	If external clocking is selected, indicates when HIGH that a hardware or software clock will be accepted. If LOW, indicates that the output is not ready to accept a clock. Active only when external clocking is selected.
D07	R/W	*SW CLOCK	0	If external clocking is selected, produces a single output clock event when asserted. Clears LOW automatically when the clock event is completed. Active only when external clocking is selected.
D08	R/W	CIRCULAR BUFFER	0	Selects circular buffer configuration if HIGH, or open self-flushing buffer configuration if LOW. Access for loading new data into the circular buffer must be requested by asserting LOAD REQUEST. Default is LOW; i.e. open buffer.
D09	R/W	*LOAD REQUEST	0	When set HIGH, requests loading access to the circular buffer. Initializes LOW.
D10	RO	LOAD READY	1	Set HIGH when the frame index passes through zero, if both CIRCULAR BUFFER and LOAD REQUEST are HIGH. When HIGH, indicates that the circular buffer is ready to accept new data. Available as an interrupt condition. Defaults HIGH.
D11	R/W	*CLEAR BUFFER	0	Resets the buffer to empty.
D12	R/W	BUFFER EMPTY	1	Status flags for the active buffer. Empty, lo-quarter and
D13	RO	BUFFER LOW QUARTER	1	hi-quarter flags are available as conditions for an interrupt request.
D14	RO	BUFFER HIGH QUARTER	0	
D15	RO	BUFFER FULL	0	

R/W = Read/Write, RO = Read-only. * Clears LOW automatically when operation is completed.

The size of each virtual buffer is determined by the SIZE[3..0] control bit field in the associated buffer operations register. Available active buffer sizes are listed in Table 3.4.2-2.

Table 3.4.2-2. Active Buffer Size

SIZE[3:0]	BUFFER SIZE (Total Channel Values)	SIZE[3:0]	BUFFER SIZE (Total Channel Values)
0	4	8	1024
1	8	9	2048
2	16	A	4096
3	32	B	8192
4	64	C	16384
5	128	D	32768
6	256	E	(Reserved)
7	512	F	(Reserved)

3.4.2.3 Status Flags

Status flags for each buffer operate with respect to the active buffer, and can provide an interrupt request if the active buffer becomes empty, 3/4-full, or less than 1/4-full. The status flags for each buffer are located in the associated buffer operations register shown in Table 3.4.2-1.

3.4.2.4 Open Buffer

Data in an open buffer is discarded as it is clocked to the output DAC. Consequently, an open buffer is self-flushing, and will empty itself unless it is replenished from the bus. This mode of operation permits the continuous flow of data from the PCI bus to the analog outputs. The buffer status flags are useful in this situation, and provide an indication of whether a buffer is empty, less than 1/4 full (low-quarter), greater than 3/4 full (high-quarter), or full. A full buffer will discard additional data from the bus, while an empty buffer indicates that the outputs are idle. The low-quarter and high-quarter flags are used to control data flow through the buffer when generating continuous functions.

NOTE: Data loss may occur if the buffer is allowed to fill completely.

The open-buffer configuration also can be used to produce a one-shot waveform, provided the particular waveform is to be used only once. Figure 3.4.2-1 illustrates the movement of a single data frame through an open buffer.

3.4.2.5 Circular Buffer

Data in a circular (closed) buffer is retained indefinitely. This configuration generally is implemented to produce either periodic waveforms of constant frequency, or one-shot transient waveforms that will be used repeatedly but not necessarily periodically. While a buffer is closed, it is not accessible from the bus. (Example 3.8.3).

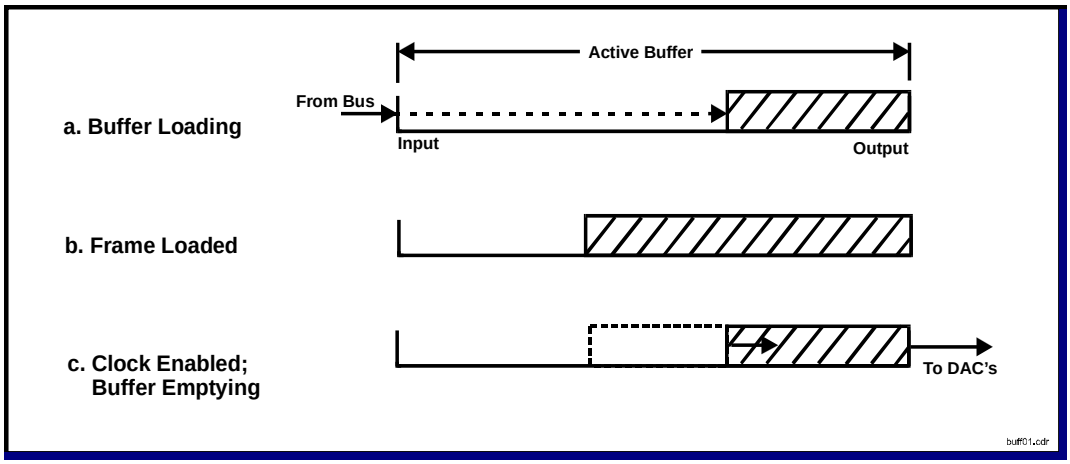

Figure 3.4.2-1. Open Buffer Data Flow

In Figure 3.4.2-2, a single data frame is loaded into a buffer. The buffer is then closed (CIRCULAR BUFFER set HIGH) and clocking is enabled. The data frame subsequently circulates in the buffer while passing data values to the output channels.

An end-of-frame (EOF) flag accompanies the end-point, or last value in a data frame. The EOF flag is D16 in each buffer, and is set HIGH when the last value in a data frame is loaded. The EOF flag is used during a triggered burst to define the last value in the burst. Multiple burst functions can reside in the buffer simultaneously.

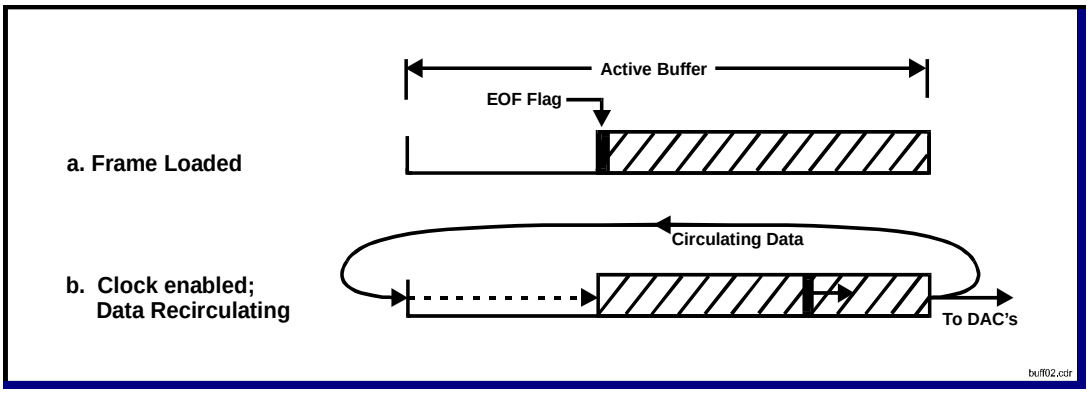

Figure 3.4.2-2. Circular Buffer Data Flow

3.4.3 Output Clocking

When the ENABLE CLOCK control bit in a buffer operations register is asserted HIGH, the associated analog output channel is updated at each occurrence of the sample clock. The sample clock can be generated internally by the rate generator, or can be supplied externally through the I/O connector.

Hardware output signal CLOCK OUT goes LOW momentarily when a sample clock occurs, Connecting this signal to the CLOCK INP pins of other boards permits synchronous clocking of multiple boards.

3.4.3.1 Clock Source

When buffer operations register bit EXTERNAL CLOCK is HIGH, the sample clock is supplied externally through the I/O connector as CLOCK INP. If the EXTERNAL CLOCK control bit is LOW, the sample clock is derived from the internal rate generator.

3.4.3.1.1 External Clock

The external clock source can have any frequency up to the maximum value specified for the sampling rate. When the external clock source is selected, sampling occurs on a HIGH-to-LOW transition of the CLOCK INP pin in the I/O connector.

Hardware output signal CLOCK OUT goes LOW momentarily when a sample clock occurs, Connecting this signal to the CLOCK INP pins of other boards permits synchronous clocking of multiple boards.

3.4.3.1.2 Sample Rate Control Registers

The internal rate generator provides a sample clock that is adjustable by the RATE[15..0] control bits in the SAMPLE RATE control register (Table 3.4.3-1).

Table 3.4.3-1. Sample Rate Control Registers

Offset: Chan-0: 0008h, Chan-1: 0048h, Chan-2: 0088h, Chan-3: 00C8h
Default: 0000 005Ah

DATA BIT	MODE	DESIGNATION	DESCRIPTION
D00	R/W	**RATE00**	Least significant rate bit
D01-D14	R/W	**RATE01 - RATE14**	Intermediate rate bits
D15	R/W	**RATE15**	Most significant rate bit
D16-D31	*R/W	**---**	(Inactive)

* Active in write-mode only. Read-access retrieves all-zero.

The sample rate Rs is calculated from the relationship:

Rs (Hz) = 27,000,000 / Nrate ,

where Nrate is the decimal equivalent of the value in the SAMPLE RATE control register, and the board's master clock frequency is 27 MHz. Table 3.4.3-2 illustrates the effect of Nrate on the sample rate. Sample clock rates greater than 400 KSPS (375KSPS for the adjustable rate clock) are not recommended.

NOTE: If the INITIATOR control bit is HIGH in the associated Adjustable Clock control register, the adjustable clock generator replaces the board's master clock, and the expression for the sample rate becomes:

Rs (Hz) = F-ADJ / Nrate ,

where F-ADJ is the frequency of the adjustable clock generator. Refer to Section 3.10 for information pertaining to the operation of the adjustable clock generator.

Table 3.4.3-2. Sample Rate Selection

Nrate (RATE[15..0])		SAMPLE RATE Rs *
(Dec)	(Hex)	(Samples per Second)
68	0044	397,059
69	0045	391,304
70	0046	385,714
---	---	Rs (Hz) = 27,000,000 / Nrate (or Rs (Hz) = F-ADJ/ Nrate)
---	---	
---	---	
65534	FFFE	412.00
65535	FFFF	411.99

3.4.4 Sampling Mode

3.4.4.1 Continuous Sampling

When the *continuous sampling* mode is selected, data is transferred continuously from the buffer to the analog outputs, assuming that the buffer is not empty and that a sample clock is present. In order for a sample clock to be present, the ENABLE CLOCK control bit in the buffer control register must be HIGH. Continuous sampling is selected when the BURST ENABLED control bit in the board control register is LOW. (Examples 3.8.2 and 3.8.3).

3.4.4.2 Data Bursts

During a *triggered burs*t, data is transferred continuously from the buffer to the analog outputs until either the buffer is empty, or the end-of-frame (EOF) flag is encountered. In the triggered-burst sampling mode, a software or hardware trigger, or sync, initiates the transfer of data from the output buffer to the output channels. A software trigger occurs when the BURST TRIGGER control bit in the board control register is set HIGH. The BURST TRIGGER bit is cleared automatically when the burst is completed.

Note: The terms "trigger" and "sync" are used interchangeably in this text.

A hardware burst trigger occurs upon a HIGH-to-LOW transition of the SYNC INP signal at the I/O connector, *if* the BURST ENABLED control bit in the BCR is HIGH, *and* if the BURST READY flag in the BCR is also HIGH. The BURST READY flag is LOW during a burst, and is HIGH if no burst is in progress.

When bursting is enabled in the BCR, hardware output signal SYNC OUT is LOW during a burst, and is HIGH when the burst is completed. Connecting this signal to the SYNC INP pins of other boards permits synchronous burst triggering of multiple boards.

Multiple burst functions can exist simultaneously within the buffer if the end-of-frame (EOF) flag is used (Paragraph 3.4.1.2). The EOF flag defines the last output value in each data burst. After a burst is triggered, data values from the buffer are clocked to the analog outputs at the selected sample rate until the EOF flag is encountered. The burst then terminates, and clocking of the buffer ceases until a subsequent trigger occurs.

3.4.5 Multiboard Synchronization

Boards that are configured for *synchronous clocking* update their outputs simultaneously in response to a common *clock* signal. Boards that are configured for *synchronous burst triggering* initiate data bursts simultaneously in response to a common *trigger* signal. Multiple boards can be arranged to operate with:

a. Independent clocking and burst triggering
b. Synchronous burst triggering
c. Synchronous clocking
d. Synchronous clocking and burst triggering.

The number of boards that can be synchronized together is limited only by the latency of approximately 80ns introduced by each board in the synchronization chain.

3.4.5.1 Synchronous Bursts

To burst-synchronize a group of boards, the TRIGGER OUT from one board, the *burst-initiator*, is connected to the TRIGGER INP pins of the first *burst-target* board in a chain of targets. Each burst-target, when operated in the triggered-burst mode (BURST ENABLED set HIGH in the board control register), initiates a single burst from its buffer each time the burst-initiator initiates a burst. A board is designated as a sync target by setting the BURST ENABLED control bit HIGH in the BCR.

3.4.5.2 Synchronous Clocking

To clock-synchronize multiple boards together, the CLOCK OUT from one board, designated the *clock-initiator*, is connected to the CLOCK INP of the first *clock-target* board in a chain of targets. The clock-targets are configured for external clocking (EXTERNAL CLOCK set HIGH in the buffer control register). A board is designated as a clock target by setting the EXTERNAL CLOCK control bit HIGH in the Buffer Operations control register.

3.4.6 Function Generation

3.4.6.1 Periodic and One-Shot Functions

Periodic waveforms are produced when the buffer is configured for continuous sampling and circular (closed) operation. In this mode, the contents of the buffer are scanned continuously as long as clocking is enabled and a clock is present. The data frame is recirculated through the buffer repeatedly. Clocking is enabled when the ENABLE CLOCK control bit in the buffer operations register is HIGH. (Example 3.8.3).

If triggered-burst sampling is used in conjunction with a circular buffer, a *one-shot waveform* is produced that contains all values within a single data frame. The triggered burst is initiated by a software or hardware trigger (sync), and terminates automatically when the end-of-frame (EOF) flag is encountered. Because the buffer is circular, the waveform values are retained in the buffer, and the waveform can be produced again by a subsequent trigger. (Example 3.8.4).

3.4.6.2 Multiple Functions

When multiple functions are loaded into the buffer as contiguous data frames, and if triggered-burst sampling is selected, the functions will be generated sequentially in response to a series

of burst triggers. If the buffer is open, the functions will be flushed from the buffer as they are clocked to the analog outputs. However, if the buffer is closed (circular), the functions will be retained in the buffer, and the series of functions can be repeated indefinitely. (Example 3.8.4).

3.4.6.3 Function Sequencing

A new function (data frame) can be concatenated to the end of an existing function in a circular buffer while the existing function is being flushed from the buffer. During this operation, the existing function is flushed from the buffer as it is clocked to the outputs, and is replaced by the new function. When the last value of the existing function is clocked out of the buffer, the buffer closes and the new function seamlessly begins circulating in the buffer and producing an output. (Example 3.8.5).

The introduction of the new function commences by setting the LOAD REQUEST flag HIGH in the buffer operations register, and by then waiting for the LOAD READY flag to be asserted. (In effect, LOAD REQUEST is an "interrupt request" to the buffer). The LOAD READY flag indicates that the buffer has been opened, and that the existing function is being flushed from the buffer, beginning with the first value in the function's data frame. The board's interrupt request will respond to the assertion of LOAD READY, if Load Ready is selected in the INT[] control field of the board control register.

After LOAD READY goes HIGH, the new function is written to the buffer and is terminated with an EOF flag (D16 set HIGH). The EOF flag causes the buffer to close, and clears both the LOAD READY flag and the LOAD REQUEST control bit. Notice that the loading of the new function into the buffer must be completed before the existing function terminates. The board's interrupt request will respond to the HIGH-to-LOW transition of LOAD READY if End Load Ready is selected in the INT[] control field of the board control register.

In Figure 3.4.6-1, an existing function is replaced by a new function while the existing ('old') function is flushed from the buffer.

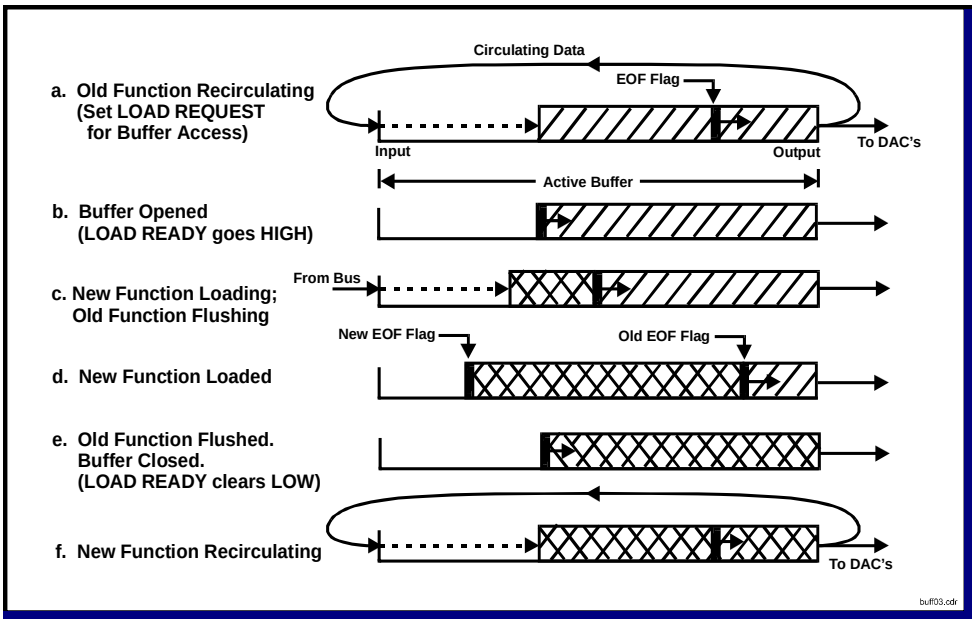

Figure 3.4.6-1. Function Sequencing

3.5 Autocalibration

Autocalibration is invoked for each output channel individually with control bits CM[1..0] in the associated BCR, or for all four channels simultaneously with the GLOBAL AUTOCAL control bit in the Channel-00 BCR. Autocalibration is initiated by setting CM[1] HIGH (CM[1..0]=2), as shown in Table 3.5-1, or by setting the GLOBAL AUTOCAL control bit HIGH in the Channel-00 BCR. CM[1..0] or GLOBAL-AUTOCAL returns to zero (normal operation) automatically at the end of autocalibration.

Table 3.5-1. Calibration Mode Selection

BCR Bits D13..12 **Default: 0h**

CM[1:0]	FUNCTION
0	Normal operation. No calibration activity. Default state.
1	(Reserved).
2	Invoke Autocalibration
3	(Reserved)

Autocalibration has a duration of approximately 1-3 seconds for a single channel, or 3-7 seconds for all four channels. Completion of a single-channel autocalibration can be detected by selecting the 'Calibration-mode operation completed' interrupt condition (paragraph 3.6) and waiting for the interrupt request. Completion of global autocalibration is indicated by a Channel-03 calibration-mode interrupt. Alternatively, a timed interval can be used to ensure that autocalibration has been completed. Write-accesses from the PCI bus should be avoided during autocalibration, and the board should be initialized after autocalibration is completed.

To compensate for component aging, and to minimize the effects of temperature on accuracy, the autocalibration function determines the optimum calibration values for current conditions, and stores the new values in both the EEprom and the calibration DAC's. Autocalibration can be invoked at any time, but should not be implemented while the system is experiencing a major environmental transition such as that which usually occurs directly after power is applied. The analog outputs are active during autocalibration. Calibration values are transferred automatically from the EEprom to the calibration DAC's during board initialization.

If a board is defective, the autocalibration process may be unable to successfully calibrate the output channels. If this situation occurs, the BIT STATUS FLAG bit in the associated BCR, and the GLOBAL AUTOCAL FAIL flag in the Channel-00 BCR, will be set HIGH at the end of the autocalibration interval, and will remain HIGH until a subsequent initialization occurs.

3.6 Interrupt Control

In order for the board to generate a PCI interrupt, *both* of the following conditions must occur:

a. The internal controller for one or more channels must generate a Local Interrupt Request
b. The *PCI interrupt* must be enabled.

A PCI bus interrupt will not occur unless the PCI interrupt has been enabled as described in Paragraph 3.6.2.

3.6.1 Local Interrupt Request

The single local interrupt request line is controlled by the INTERRUPT A[2:0] and INTERRUPT REQUEST FLAG control bits in all four BCR's. Each channel can generate a local interrupt request independently of the other channels.

NOTE: The local interrupt requests from all four channels are logically OR'd to produce the single PCI interrupt (INT A) for the board.

The source condition for the request is selected as shown in Table 3.6.1-1, and each output channel can have a condition selected that differs from that of the other channel. When the selected condition occurs for either channel, a local interrupt request is generated and the INTERRUPT REQUEST FLAG bit is set in the associated BCR. The request remains asserted until the PCI bus clears the associated BCR request flag. Local interrupt requests from all output channels are generated automatically at the end of initialization.

Table 3.6.1-1. Interrupt Source Selection

BCR Bits D10..D08 **Default: 0h**

INTERRUPT A[2:0]	INTERRUPT CONDITION
0	Idle. Interrupt disabled unless initializing. Default state.
1	Calibration-mode operation completed
2	Output buffer empty
3	Output buffer low-quarter (buffer less than 1/4-full)
4	Output buffer high-quarter (buffer 3/4-full)
5	Burst Trigger Ready
6	Load Ready (LOW-to-HIGH transition)
7	End Load Ready (HIGH-to-LOW transition of Load Ready)

Detection of an interrupt condition or event is *edge-sensitive*. An interrupt request is generated if, and only if, a specific interrupt condition undergoes a *transition* from 'false' (not-true) to 'true' while that condition is selected.

3.6.2 Enabling the PCI Interrupt

A local interrupt request will not produce an interrupt on the PCI bus unless the PCI interrupt is enabled. The PCI interrupt is enabled by setting the *PCI Interrupt Enable* and *PCI Local Interrupt Enable* control bits HIGH in the runtime *Interrupt Control/Status Register* described in Section 4 of the PLX™ PCI-9080 reference manual.

3.7 (Reserved Section).

3.8 Application Examples

Specific operating modes and procedures will vary widely according to the unique requirements of each application. The examples presented in this section (Table 3.8-1) illustrate several basic operating modes, and can be modified or combined for operations that are more complex. All examples apply independently to each of the four output channels.

Table 3.8-1. Summary of Operation Examples

Operation Example	Description
Direct Outputs	A special case of continuous operation, in which the output buffer is allowed to become empty, and in which the output function is not continuous. Each value written to the buffer appears at the output when the next output clock occurs.
Continuous Function	Identical to Direct Outputs, except that the buffer is not allowed to become either empty or full, and the output is a continuous function.
Periodic Function	A single function is generated repeatedly.
Function Burst	One or more functions are generated as discrete data bursts. The burst cycle is repeated indefinitely if the circular-buffer mode is selected.
Function Sequencing	An existing active function is replaced seamlessly by a new function.

Each of the examples in this section assumes that the initial operations listed in Table 3.8-2 have already been performed.

Table 3.8-2. Initial Operations

Operation	Default Value	Applicable Paragraph
The board has been reset or initialized.	---	3.3
The required output coding has been selected.	Offset binary	3.4.1.3.2
Active buffer size has been selected.	Maximum buffer size	3.4.2.2

The remaining operational parameters are assumed to be in the following *default* states:

Buffer mode:	Open	Sample rate:	300 KSPS
Buffer status:	Empty	Sampling mode:	Continuous
Clock source:	Internal	Interrupt selected:	0 (Idle)
Clock status:	Disabled		

3.8.1 Direct Outputs

Table 3.8.1-1. Direct Outputs Example

Operation	PCI Bus Action	Board Response
Enable clocking	Set ENABLE CLOCK (D05) HIGH in the buffer operations register.	Clocking is enabled at 300 KSPS.
Write a 16-Bit value to the output buffer.	Write the first value to the output data buffer.	Output value appears at the analog output within 3-6 us.
Write successive values to the output buffer at a rate of less than 300K values per second.	Write additional values to the output buffer.	Each value appears at the output within 3-6us.

Note: Data written to the buffer at rates above 300KSPS will accumulate in the buffer.

3.8.2 Continuous Function

Table 3.8.2-1. Continuous Function Example

Operation	PCI Bus Action	Board Response
If the internal rate generator is to be used, select the sample rate. (Skip this step if external clocking will be used).	Write the required sample clocking rate to the sample rate control register.	The frequency of the internal rate generator is selected if internal clocking is used.
Note: The following two operations can be performed simultaneously with a single write-transaction to the buffer operations register:	---	---
If external clocking is required, select external clocking.	To select external clocking, set EXTERNAL CLOCK (D04) HIGH in the buffer operations register.	External clocking is selected, if required.
Enable clocking	Set ENABLE CLOCK (D05) HIGH in the buffer operations register.	Clocking is enabled.
Select the buffer lo-quarter interrupt.	Set the INT[] bit field to 3 in the board control register.	The interrupt will respond when the buffer becomes less than 1/4 full.
Write a block of values to the output buffer. Total block size should be between 1/4 and 3/4 of the buffer size. (Note 1). To avoid discontinuities in the output function, the loading rate must be greater than the sample (clocking) rate. Maximum loading rate is 13MSPS during DMA transfers.	Write function values to the output data buffer.	The analog output generates the buffer function at the selected clocking rate.
Wait for the lo-quarter interrupt. (Note 2).	Other, nonrelated activities can occur on the PCI bus.	The output buffer empties to less than 1/4-full status.
Repeat the previous two steps to sustain function generation.		The output function continues.

Notes:
1. The size of a data block must be at least 1/4 the size of the buffer to ensure that the lo-quarter interrupt will occur, and no greater than 3/4 the size of the buffer to avoid data loss by forcing the buffer to full-status.
2. Response to the interrupt must be fast enough to prevent the buffer from going empty.

3.8.3 Periodic Function

Table 3.8.3-1. Periodic Function Example

Operation	PCI Bus Action	Board Response
Write all function values to the output buffer.	Write the function to the output buffer.	The function loads into the buffer.
If the internal rate generator is to be used, select the sample rate. (Skip this step if external clocking is required).	Write the required sample rate to the sample rate control register.	The frequency of the internal rate generator is selected if internal clocking is required.
Note: The remaining operations may be performed simultaneously with a single write-transaction to the buffer operations register:	---	---
Select the circular buffer mode.	Set CIRCULAR BUFFER (D08) HIGH in the buffer operations register.	The output buffer is closed (circular). Subsequent data written to the buffer will be discarded..
If external clocking is required, select external clocking.	To select external clocking, set EXTERNAL CLOCK (D04) HIGH in the buffer operations register.	External clocking is selected, if required.
Enable the sample clock.	Set ENABLE CLOCK (D05) HIGH in the buffer operations register.	Clocking is enabled. The analog output channel produces the function repeatedly at the selected clocking rate until the clock is disabled or the operating mode is changed.

3.8.4 Function Burst

Table 3.8.4-1. Function Burst Example

Operation	PCI Bus Action	Board Response
Clear the data buffer and disable clocking.	Set the CLEAR BUFFER bit (D11) and clear the ENABLE CLOCK bit (D05) in the buffer operations Register.	The buffer is cleared and clocking is disabled.
Write the burst function to the output buffer. Set the EOF (Bit-16) with the last value.	Write the values for the first active group to the output data buffer. Identify the last value.	The function loads into the buffer.
If more than one burst-function is required, repeat the previous operation for each additional function.	---	If required, additional burst functions accumulate in the output buffer.
If the internal rate generator is to be used, select the sample rate.	Write the required sample rate to the sample rate control register.	The frequency of the internal rate generator is selected if internal clocking is required.
Select triggered-burst mode.	Set BURST ENABLED (D00) HIGH in the board control register.	The triggered-burst sampling mode is selected.
Prepare the buffer operations register for burst mode:	Write a single value to the buffer operations register:	---
If the burst functions will be used repeatedly, select the circular buffer mode.	To select the circular buffer mode, set CIRCULAR BUFFER (D08) HIGH.	If required, the output buffer is closed (circular), and all functions will be retained in the buffer indefinitely.
If external clocking is required, select external clocking.	To select external clocking, set EXTERNAL CLOCK (D04) HIGH.	External clocking is selected, if required.
Enable the sample clock.	Set ENABLE CLOCK (D05) HIGH.	Clocking is enabled. The board is awaiting a burst trigger (sync).
For software burst triggering, generate a software trigger to produce a single burst.	Set BURST TRIGGER (D02) HIGH in the board control register. (BURST TRIGGER is cleared automatically when the burst is completed).	The analog output channel produces a single burst in response to a software trigger. (Use Interrupt-5 to detect the burst-ready condition).
For external burst triggering, no further bus activity is required.	---	The analog output channel produces a single burst in response to each HIGH-to-LOW transition of SYNC INP at the I/O connector.

3.8.5 Function Sequencing

Table 3.8.5-1. Function Sequencing Example

Operation	PCI Bus Action	Board Response
Establish a periodic function as described in Paragraph 3.8.3. The following operations will replace the original ('old') function with a new function.	---	The analog output channel is producing a specific output function or waveform. The output buffer is circular (closed), and is not accessible from the bus.
Request access to the output data buffer.	Select the load-ready interrupt by setting INT[]=6 in the board control register. Set LOAD REQUEST (D09) HIGH in the buffer operations register.	The load-ready interrupt is selected. The board will assert the LOAD READY flag (D10) when the EOF flag in the original function occurs.
Wait for the buffer to open.	Wait for the load-ready interrupt request (Buffer Operations register Bit D10 HIGH). Then clear D11..08 in the board control register.	The EOF flag in the existing function set causes the LOAD READY bit in the buffer operations register to be asserted. A load-ready interrupt request is generated. The buffer is now open, and the original function is being flushed from the buffer.
Write the new function to the buffer. Set the end-of-frame (EOF) flag.	Write the new-function values to the output buffer. Set the EOF flag (D16 in the output buffer) HIGH when writing the data value for the last channel in the last group.	New-function values now reside in the buffer. The EOF flag is set HIGH in the buffer location that contains the last channel value. The original function is still active, and the remaining values are flushed from the buffer as they are sent to the output.
(None required)	No further attention is required from the PCI bus.	The buffer returns to circular (closed) mode when the last data value in the original function moves out of the buffer. The new function then commences seamlessly and circulates within the buffer. Both the Load Request control bit and the Load Ready flag are cleared automatically when the buffer closes. The End Load Ready interrupt condition can be used to detect completion of the flushing sequence.

3.9 DMA Operation

DMA transfers to either of the four analog output FIFO buffers are supported with the board operating as bus master. Table 3.9-1 illustrates a typical PCI register configuration that would control a non-chaining, non-incrementing, DMA block-transfer, in which a PCI interrupt is generated when the transfer has been completed. Bit 02 in the PCI Command register (04h) must be set HIGH to select the bus mastering mode. Refer to the PCI-9080 product guide for a detailed description of these registers.

Table 3.9-1. Typical DMA Register Configuration

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial (constant) local address	Ch.00: 0000 0018h Ch.01: 0000 0058h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction (PCI bus to Local bus)	0000 0000h
A8h	DMA Command Status	Command and Status Register	0000 0001h 0000 0003h (See Text)

* Determined by specific transfer requirements.

For most applications, the DMA Command Status Register (A8h) should be initialized to the value 0000 0001h, and then changed to 0000 0003h to initiate a transfer.

3.10 Alternate Clocking Sources

Section 3.4.3 describes a method of deriving the clocking rate for each output channel from the board's master clock. For applications that require more precise adjustment of the clocking rates however, the following two additional clock sources are available to each channel.

- Adjustable clock generator,
- Fixed-frequency generators.

3.10.1 Adjustable Clock Generators

Each output channel has access to a dedicated phase-locked loop (PLL) oscillator that can be adjusted from 16 MHz to 32 MHz with 0.2-percent adjustment resolution. This adjustable clock generator is activated by setting the SELECT ADJUSTABLE CLOCK control bit HIGH in the associated Adjustable Clock control register shown in Table 3.10.1-1. When activated for either channel, an adjustable clock generator replaces the board's master clock as the frequency source for that channel, and the expression for the output clocking rate **Rs** is modified to:

Rs (Hz) = F-ADJ / Nrate,

where **F-ADJ** is the frequency of the adjustable clock, in Hertz, and **Nrate** is a 16-bit integer in the Sample Rate control register (See Paragraph 3.4.3.1.2).

3.10.1.1 Adjustable Clock Frequency Control

The frequency of the adjustable clock is controlled by a 9-bit field D08:00 in the Adjustable Clock control register, as shown in Table 3.10.1-1.

Table 3.10.1-1. Adjustable Clock Control Registers

Offset: Chan-0: 001Ch, Chan-1: 005Ch, Chan-2: 009Ch, Chan-3: 00DCh
Default: 0000 0000h

REGISTER BITS	ACCESS MODE	DESIGNATION	DESCRIPTION
D[08:00]	R/W	CLOCK RATE (**Nclk**)	Controls the frequency of the adjustable clock.
D[09]	R/W	SELECT ADJUSTABLE CLOCK	Replaces the master clock with the adjustable clock when HIGH.
D[31:10]	RO	(Reserved, read-only)	(Reserved)

The frequency **F-ADJ** of the adjustable clock is controlled from 16 MHz to 32 MHz by the 9-bit value **Nclk,** according to the relationship:

$$\textbf{F-ADJ} = 16 * (1 + \textbf{Nclk} / 511),$$

where **F-ADJ** is in Megahertz, and **Nclk** is an integer with a value from zero to 511. For example, a value of 100 for **Nclk** would produce an adjustable clock frequency of 19.131MHz.

3.10.1.2 Adjustable Clock Selection

When the SELECT ADJUSTABLE CLOCK control bit is HIGH, the adjustable clock frequency replaces the master clock frequency of 27MHz referred to in Section 3.4.3.1.2. When the control bit is LOW (default), the sample rate is the master clock frequency (27 MHz), divided by the value contained in the Sample Rate control register.

In *all* configurations, the CLOCK OUT signal at the I/O connector is the analog output sampling clock for Channel-00, and produces a single clock pulse each time the Channel-00 output is updated.

3.10.2 Fixed-Frequency Clock Generators

As many as eight fixed frequencies can be selected as the clock generator for each output channel. Any one of these frequencies can be selected with the Internal Clocking Source control register shown in Table 3.10.2-1. Unlike the master and adjustable clock generators, the fixed frequency clocks are unaffected by the Sample Rate control register (Table 3.4.3-1) and represent the actual output clocking frequencies.

Table 3.10.2-1. Internal Clock Source Control Register

Offset: Chan-0: 0020h, Chan-1: 0060h, Chan-2: 00A0h, Chan-3: 00E0h
Default: 0000 0000h

REGISTER BITS	ACCESS MODE	DESIGNATION	DESCRIPTION
D[03:00]	R/W	INTERNAL CLOCK SOURCE	Selects the divided output of the master or adjustable clock generators, or one of eight custom fixed clocking frequencies: CODE CLOCKING SOURCE 0 Divided Master or Adjustable clock 1 Fixed Frequency-1 2 Fixed Frequency-2 3 Fixed Frequency-3 4 Fixed Frequency-4 5 Fixed Frequency-5 6 Fixed Frequency-6 7 Fixed Frequency-7 8 Fixed Frequency-8
D[31:04]	RO	(Reserved, read-only)	(Reserved)

In the initial release of this product, the fixed frequencies were defined as listed in Table 3.10.2-2. The fixed frequencies are derived from a precision master clock, and exhibit a maximum error of ±10 PPM plus the master clock error (Typically 20 PPM).

Table 3.10.2-2. Initial-Release Fixed Frequencies

FIXED-FREQUENCY CODE	OUTPUT CLOCKING FREQUENCY (Samples per second)
1	224,000.00
2	60,000.00
3	27,304.00
4	22,500.00
5	10,000.00
6	10,000.00
7	10,000.00
8	10,000.00

3.11 Digital I/O Port

Eight bidirectional digital I/O lines provide a byte-wide digital port. The port is accessed by direct register read or write through the Digital I/O Port control register shown in Table 3.11-1. The lines are configured as an output port when the DIGITAL DIRECTION OUT control line is HIGH, or as an input port when the control bit is LOW.

When configured as an input port, the lower eight bits in the register (DIGITAL I/O D00-07) follow the I/O lines. When configured as an output port, the I/O lines follow the value written to the lower eight bits. Each bit position in the register corresponds to the same numbered I/O line, with no logic inversion.

Table 3.11-1. Digital I/O Port Control Register

Offset: 0004h **Default: 0000 00XXh**

DATA BIT	MODE	DESIGNATION	DEFAULT	DESCRIPTION
D00-D07	R/W	**DIGITAL I/O D00-D07**	XXh	Bidirectional digital I/O data field. Follows the digital I/O data lines when configured as an input port. Drives the I/O lines when configured as an output port.
D08:	R/W	**DIGITAL DIRECTION OUT**	0	When HIGH, configures the digital I/O lines as an output port. When LOW, configures the lines as an input port.
D09-31	RO	(Reserved)	0000 0h	---

SECTION 4.0

PRINCIPLES OF OPERATION

4.1 General Description

Each of the four analog output channels contains a primary 16-bit output DAC, two 12-bit calibration DAC's, a data buffer and an adjustable rate clock. As Figure 4.1-1 illustrates, a PCI interface adapter provides an interface between the controlling PCI bus and an internal local controller through a 20-bit local bus. The local controller performs all internal configuration and data manipulation functions, including autocalibration.

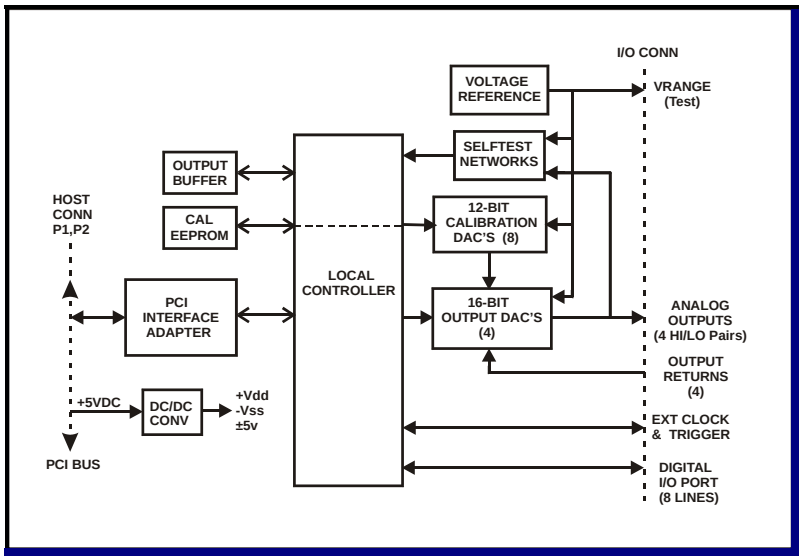

Figure 4.1-1. Functional Block Diagram

During normal operation, analog output data values are written from the PCI bus to the data buffer of one or more output channels. The data values subsequently are serialized and transferred to the respective analog output DAC's. All output channels are configured as 3-wire balanced differential outputs.

External control inputs and outputs accept burst-sync and sample-clock inputs, and provide the digital signals necessary for multiboard synchronization.

Selftest networks allow the controller to compare the analog levels from all output channels against the internal voltage reference, and are used to establish the internal connections necessary during autocalibration. All channels are calibrated with respect to the single precision voltage reference.

The offset and gain corrections for each output channel are adjusted with a pair of 12-bit Calibration DAC's, the values for which are stored in nonvolatile electrically erasable programmable read-only memory (EEprom). The calibration EEprom and calibration DAC's provide the adjustment functions that otherwise would be associated with eight trimmers in conventional analog configurations. Calibration control values are determined and stored in EEprom during autocalibration.

4.2 Analog Outputs

Each analog output channel consists of a 16-bit output DAC and two 12-bit calibration DAC's. The local controller reads the 16-bit channel data value for each channel from the analog output buffer, and sends the value serially to the associated output DAC. The output DAC deserializes the data to obtain the original 16-bit data word, and holds that word in an internal buffer until commanded to transfer the data to the output register that drives the DAC output.

The two calibration DAC's in each output channel provide offset and gain trimming of the associated 16-bit output DAC, using trim values that are determined during autocalibration.

4.3 Autocalibration

Autocalibration is an embedded firmware utility that calibrates the output channels to a single internal voltage reference. The utility can be invoked at any time by the control software.

An internal voltage reference is adjusted during the adjustment procedure described in Section 2 to equal approximately 99.9 percent of the output voltage range. This voltage reference is compared with actual channel output values to calibrate the gain of each analog output channel. Calibration values for channel offsets are determined by comparing channel outputs with the potential on the internal analog ground bus.

Each of the four calibration DAC's is adjusted in a successive approximation sequence that commences with the DAC in an all-zero state. The most significant bit initially is set to "1", and the resulting effect on the channel is measured. Depending upon the measured response, the bit either is cleared or is left in the "1" state. The next lower significant bit is then tested in the same manner, and this process continues until all 12 bits have been tested and adjusted. The final value in the calibration DAC is stored in the nonvolatile calibration EEprom for subsequent retrieval by the local controller during initialization.

4.4 Power Control

Regulated supply voltages of +5 VDC and ±15 VDC are required by the analog networks, and are derived from the +5 VDC input from the PCI bus through a DC/DC converter. To obtain optimum performance from the internal supplies, all analog power voltages are series post-regulated.

APPENDIX A

LOCAL REGISTER QUICK REFERENCE

APPENDIX A
LOCAL REGISTER QUICK REFERENCE

This appendix summarizes all local registers and principal control-bit fields that appear in Section 3.

Table 3.1-1. Channel-00 Control and Data Registers

OFFSET	REGISTER	ACCESS MODE*	DEFAULT	PRIMARY FUNCTION
00	BOARD CONTROL (BCR)	R/W	0 0810h	Channel-00 Board Control Register (BCR)
04	DIGITAL BYTE PORT	R/W	0 00XXh	Digital I/O lines control
08	SAMPLE RATE	R/W	0 005Ah	Channel-00 clocking rate divisor
0C	BUFFER OPERATIONS	R/W	0 340Dh	Channel-00 Buffer size selection
10	** Firmware Revision	RO	0 XXXXh	**
14	** Autocal Diagnostics	RO	0 0XXXh	**
18	OUTPUT DATA BUFFER	WO	X XXXXh	Channel-00 analog output FIFO buffer
1C	ADJUSTABLE CLOCK	R/W	0 0000h	Channel-00 adjustable clock.
20	INTERNAL CLOCK SOURCE	R/W	0 0000h	Channel-00 internal clock source
24	** Master clock freq trim	RO	0 09C4h	**
28-3F	(Reserved)	RO	X XXXXh	---

* Access mode is D32, with 17 active bits. R/W = Read/Write; RO= Read-only; WO = Write-only.
** Diagnostic/maintenance registers. Included here for reference only..

Table 3.1-2. Channel-01, 02, 03 Control and Data Registers

OFFSET						
Ch 1	Ch 2	Ch 3	REGISTER	ACCESS MODE*	DEFAULT	PRIMARY FUNCTION
40	80	C0	BOARD CONTROL (BCR)	R/W	0 0810h	Channel-01 Board Control Register
44	84	C4	(Reserved)	RO	0 0000h	---
48	88	C8	SAMPLE RATE	R/W	0 005Ah	Channel clocking rate divisor
4C	8C	CC	BUFFER OPERATIONS	R/W	0 340Dh	Channel Buffer size selection
50	90	D0	** Firmware Revision	RO	0 XXXXh	**
54	94	D4	** Autocal Diagnostics	RO	0 0XXXh	**
58	98	D8	OUTPUT DATA BUFFER	WO	X XXXXh	Channel analog output FIFO buffer
5C	9C	DC	ADJUSTABLE CLOCK	R/W	0 0000h	Channel adjustable clock.
60	A0	E0	INTERNAL CLOCK SOURCE	R/W	0 0000h	Channel internal clock source
64-7F	A4-BF	E4-FF	(Reserved)	RO	X XXXXh	---

* Access mode is D32, with 17 active bits. R/W = Read/Write; RO= Read-only; WO = Write-only.
** Diagnostic/maintenance registers. Included here for reference only.

Table 3.2-1. Channel-00 Board Control Register

Offset: 0000h **Default: 0000 0810h**

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00	R/W	BURST ENABLED	0	Selects burst-mode if HIGH, continuous-mode if LOW. Default is LOW; i.e. continuous-mode.
D01	RO	BURST READY	0	If HIGH, indicates that a burst trigger (sync) will be accepted. If LOW, indicates that a burst is in progress, and that a trigger will not be accepted. Available as an interrupt condition.
D02	R/W	*BURST TRIGGER	0	Software burst trigger, asserted HIGH. Active only when BURST ENABLED control bit is asserted. Initialized LOW.
D03	RO	GLOBAL AUTOCAL FAIL	0	High if any channel fails autocalibration.
D04	R/W	OFFSET BINARY	1	Selects offset-binary data format when asserted HIGH, or two's complement when LOW.
D05	R/W	TTL SYNC I/O	0	Selects the external TTL clock and sync inputs when HIGH, or the differential clock and sync inputs when LOW.
D06	R/W	* GLOBAL AUTOCAL	0	Initiates autocalibration of all four channels.
D07	R/W	COMMON RATE GEN	0	Selects the Channel-01 rate generator for Channel-00 clocking when HIGH, or the Channel-00 rate generator when LOW. Active only in initiator mode.
D08	R/W	INTERRUPT A0	0	Interrupt source selection.
D09	R/W	INTERRUPT A1	0	
D10	R/W	INTERRUPT A2	0	
D11	R/W	INTERRUPT REQUEST FLAG	1	Set HIGH when Channel-00 asserts an interrupt request. Clears the request when cleared LOW by the bus.
D12	R/W	*CM0	0	Calibration mode. Defaults to normal operation.
D13	R/W	*CM1	0	Completion available as an interrupt condition.
D14	RO	BIT STATUS FLAG	0	Records the status of channel autocalibration; LOW for pass, HIGH for fail. Initializes LOW.
D15	R/W	*INITIALIZE	0	Initializes the board when set HIGH. Sets all defaults for all registers.

* Cleared automatically when operation is completed. R/W = Read/Write; RO=Read-Only.

Table 3.2-2. Channel-01, 02, 03 Board Control Registers

Offset: Chan-1: 0040h, Chan-2: 0080h, Chan-3: 00C0h
Default: 0000 0810h

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00	R/W	BURST ENABLED	0	Selects burst-mode if HIGH, continuous-mode if LOW. Default is LOW; i.e. continuous-mode.
D01	RO	BURST READY	0	If HIGH, indicates that a burst trigger (sync) will be accepted. If LOW, indicates that a burst is in progress, and that a trigger will not be accepted. Available as an interrupt condition.
D02	R/W	*BURST TRIGGER	0	Software burst trigger, asserted HIGH. Active only when BURST ENABLED control bit is asserted. Initialized LOW.
D03	RO	(Reserved)	0	---
D04	R/W	OFFSET BINARY	1	Selects offset-binary data format when asserted HIGH, or two's complement when LOW.
D05	R/W	TTL SYNC I/O	0	Selects the external TTL clock and sync inputs when HIGH, or the differential clock and sync inputs when LOW.
D06	R/W	(Reserved)	0	---
D07	R/W	COMMON RATE GEN	0	Selects the Channel-00 rate generator for Channel-X clocking when HIGH, or the Channel-X rate generator when LOW. Active only in initiator mode. ("X" is 1, 2 or 3).
D08	R/W	INTERRUPT A0	0	Interrupt source selection.
D09	R/W	INTERRUPT A1	0	
D10	R/W	INTERRUPT A2	0	
D11	R/W	INTERRUPT REQUEST FLAG	1	Set HIGH when Channel-01 board asserts an interrupt request. Clears the request when cleared LOW by the bus.
D12	R/W	*CM0	0	Calibration mode. Defaults to normal operation.
D13	R/W	*CM1	0	Completion available as an interrupt condition.
D14	RO	BIT STATUS FLAG	0	Records the status of channel autocalibration; LOW for pass, HIGH for fail. Initializes LOW.
D15	R/W	*INITIALIZE	0	Initializes the board when set HIGH. Sets all defaults for all registers.

* Cleared automatically when operation is completed. R/W = Read/Write; RO=Read-Only.

Table 3.4.1-2. Output Data Buffers

Offset: Chan-0: 0018h, Chan-1: 0058h, Chan-2: 0098h, Chan-3: 00D8h
Default: 000X XXXXh

DATA BIT	MODE*	DESIGNATION	DESCRIPTION
D00	WO	**DATA00**	Least significant data bit
D01-D14	WO	**DATA01 - DATE14**	Intermediate data bits
D15	WO	**DATA15**	Most significant data bit
D16	WO	**EOF FLAG**	End-of-frame (EOF) flag.
D17-D31	WO	**---**	(Inactive)

* WO indicates write-only access. Read-access returns an all-zero value.

Table 3.4.2-1. Buffer Operations Registers

Offset: Chan-0: 000Ch, Chan-1: 004Ch, Chan-2: 008Ch, Chan-3: 00CCh
Default: 0000 340Dh

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00	R/W	SIZE0	1	Size-selection bit field for the active buffer. Defaults to Dh (32K Samples).
D01	R/W	SIZE1	0	
D02	R/W	SIZE2	1	
D03	R/W	SIZE3	1	
D04	R/W	EXTERNAL CLOCK	0	Selects hardware or software clock source when HIGH, or the internal rate generator when LOW. Default is LOW (internal rate generator).
D05	R/W	ENABLE CLOCK	0	Enables output clocking when HIGH. Disables clocking when LOW. Default is LOW (clocking disabled).
D06	RO	CLOCK READY	0	If external clocking is selected, indicates when HIGH that a hardware or software clock will be accepted. If LOW, indicates that the output is not ready to accept a clock. Active only when external clocking is selected.
D07	R/W	*SW CLOCK	0	If external clocking is selected, produces a single output clock event when asserted. Clears LOW automatically when the clock event is completed. Active only when external clocking is selected.
D08	R/W	CIRCULAR BUFFER	0	Selects circular buffer configuration if HIGH, or open self-flushing buffer configuration if LOW. Access for loading new data into the circular buffer must be requested by asserting LOAD REQUEST. Default is LOW; i.e. open buffer.
D09	R/W	*LOAD REQUEST	0	When set HIGH, requests loading access to the circular buffer. Initializes LOW.
D10	RO	LOAD READY	1	Set HIGH when the frame index passes through zero, if both CIRCULAR BUFFER and LOAD REQUEST are HIGH. When HIGH, indicates that the circular buffer is ready to accept new data. Available as an interrupt condition. Defaults HIGH.
D11	R/W	*CLEAR BUFFER	0	Resets the buffer to empty.
D12	R/W	BUFFER EMPTY	1	Status flags for the active buffer. Empty, lo-quarter and hi-quarter flags are available as conditions for an interrupt request.
D13	RO	BUFFER LOW QUARTER	1	
D14	RO	BUFFER HIGH QUARTER	0	
D15	RO	BUFFER FULL	0	

R/W = Read/Write, RO = Read-only. * Clears LOW automatically when operation is completed.

Table 3.4.2-2. Active Buffer Size

SIZE[3:0]	BUFFER SIZE (Total Channel Values)
0	4
1	8
2	16
3	32
4	64
5	128
6	256
7	512

SIZE[3:0]	BUFFER SIZE (Total Channel Values)
8	1024
9	2048
A	4096
B	8192
C	16384
D	32768
E	(Reserved)
F	(Reserved)

Table 3.4.3-1. Sample Rate Control Registers

Offset: Chan-0: 0008h, Chan-1: 0048h, Chan-2: 0088h, Chan-3: 00C8h
Default: 0000 005Ah

DATA BIT	MODE	DESIGNATION	DESCRIPTION
D00	R/W	**RATE00**	Least significant rate bit
D01-D14	R/W	**RATE01 - RATE14**	Intermediate rate bits
D15	R/W	**RATE15**	Most significant rate bit
D16-D31	*R/W	**---**	(Inactive)

* Active in write-mode only. Read-access retrieves all-zero.

Table 3.4.3-2. Sample Rate Selection

Nrate (RATE[15..0])		SAMPLE RATE Rs *
(Dec)	(Hex)	(Samples per Second)
68	0044	397,059
69	0045	391,304
70	0046	385,714
---	---	Rs (Hz) = 27,000,000 / Nrate (or Rs (Hz) = F-ADJ/ Nrate)
---	---	
---	---	
65534	FFFE	412.00
65535	FFFF	411.99

Table 3.5-1. Calibration Mode Selection

BCR Bits D13..12 **Default: 0h**

CM[1:0]	FUNCTION
0	Normal operation. No calibration activity. Default state.
1	(Reserved).
2	Invoke Autocalibration
3	(Reserved)

Table 3.6.1-1. Interrupt Source Selection

BCR Bits D10..D08 **Default: 0h**

INTERRUPT A[2:0]	INTERRUPT CONDITION
0	Idle. Interrupt disabled unless initializing. Default state.
1	Calibration-mode operation completed
2	Output buffer empty
3	Output buffer low-quarter (buffer less than 1/4-full)
4	Output buffer high-quarter (buffer 3/4-full)
5	Burst Trigger Ready
6	Load Ready (LOW-to-HIGH transition)
7	End Load Ready (HIGH-to-LOW transition of Load Ready)

Table 3.10.1-1. Adjustable Clock Control Registers

Offset: Chan-0: 001Ch, Chan-1: 005Ch, Chan-2: 009Ch, Chan-3: 00DCh
Default: 0000 0000h

REGISTER BITS	ACCESS MODE	DESIGNATION	DESCRIPTION
D[08:00]	R/W	CLOCK RATE (**Nclk**)	Controls the frequency of the adjustable clock.
D[09]	R/W	SELECT ADJUSTABLE CLOCK	Replaces the master clock with the adjustable clock when HIGH.
D[31:10]	RO	(Reserved, read-only)	(Reserved)

Table 3.10.2-1. Internal Clock Source Control Register

Offset: Chan-0: 0020h, Chan-1: 0060h, Chan-2: 00A0h, Chan-3: 00E0h
Default: 0000 0000h

REGISTER BITS	ACCESS MODE	DESIGNATION	DESCRIPTION
D[03:00]	R/W	INTERNAL CLOCK SOURCE	Selects the divided output of the master or adjustable clock generators, or one of eight custom fixed clocking frequencies: CODE CLOCKING SOURCE 0 Divided Master or Adjustable clock 1 Fixed Frequency-1 2 Fixed Frequency-2 3 Fixed Frequency-3 4 Fixed Frequency-4 5 Fixed Frequency-5 6 Fixed Frequency-6 7 Fixed Frequency-7 8 Fixed Frequency-8
D[31:04]	RO	(Reserved, read-only)	(Reserved)

Table 3.10.2-2. Initial-Release Fixed Frequencies

FIXED-FREQUENCY CODE	OUTPUT CLOCKING FREQUENCY (Samples per second)
1	224,000.00
2	60,000.00
3	27,304.00
4	22,500.00
5	10,000.00
6	10,000.00
7	10,000.00
8	10,000.00

Table 3.11-1. Digital I/O Port Control Register

Offset: 0004h **Default: 0000 00XXh**

DATA BIT	MODE	DESIGNATION	DEFAULT	DESCRIPTION
D00-D07	R/W	**DIGITAL I/O D00-D07**	XXh	Bidirectional digital I/O data field. Follows the digital I/O data lines when configured as an input port. Drives the I/O lines when configured as an output port.
D08:	R/W	**DIGITAL DIRECTION OUT**	0	When HIGH, configures the digital I/O lines as an output port. When LOW, configures the lines as an input port.
D09-31	RO	(Reserved)	0000 0h	---

APPENDIX B

MIGRATION FROM PMC-16AO2MF

APPENDIX-B

MIGRATION FROM PMC-16AO2MF

Operation of the PMC-16AO4MFS is similar to that of the PMC-16AO2MF. This appendix summarizes the primary issues involved in migrating an application from the PMC-16AO2MF to the PMC-16AO4MFS.

****

FUNCTIONAL CHANGES:

Number of Channels:

The number of output channels has increased from two to four.

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APPLICATION CONTROL SOFTWARE ISSUES:

1. Channel-02 and Channel-03 Control Register Sets: (Table 3.1-2):

Two additional sets of control registers have been added on offset boundaries 0x00A0 and 0x00C0.

2. Channel-00 Board Control Register (Table 3.2-1 and Paragraph 3.5):

A new control bit GLOBAL AUTOCAL (D06) initiates autocalibration of all four channels. An associated status flag GLOBAL AUTOCAL FAIL (D03) indicates the autocalibration failure of any channel.

3. Channel-01 Oscillator-Trim register (Table 3.1-1):

The Channel-01 Oscillator-Trim register has never been used, and has been eliminated.

4. Common Rate Generator Selection (Table 3.2-1):

The definition of the COMMON RATE GEN control bit has been modified to accommodate two additional channels, and permits Channels 01, 02 and 03 to be synchronized to the Channel-00 output clock. The COMMON RATE GEN control bit in the Channel-00 BCR remains as defined for the PMC-16AO2MF to minimize possible impact on existing application software.

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