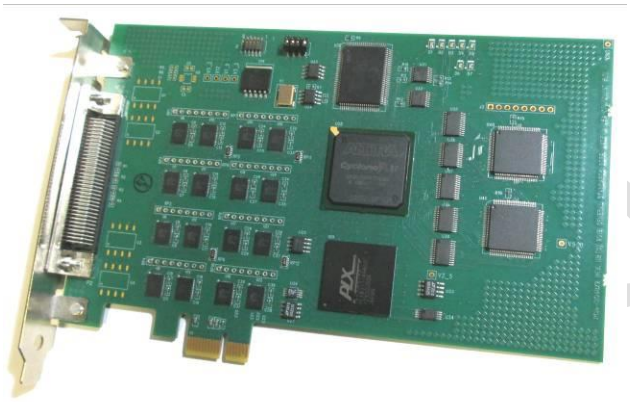
PCIe-DIO32A

User's Manual



32 Port PCIe Digital I/O

With RS422/RS485 Transceivers

RS-422/ RS-485

General Standards Corporation
8302A Whitesburg Drive
Huntsville, AL 35802
Phone: (256) 880-8787
Fax: (256) 880-8788
URL: www.generalstandards.com
E-mail: techsupport@generalstandards.com

Revision NR

PREFACE

Revision History

1. Rev NR – Aug 2015 – Original rev.

Additional copies of this manual or other **General Standards Corporation** literature may be obtained from:

General Standards Corporation
8302A Whitesburg Drive
Huntsville, Alabama 35802
Telephone: (256) 880-8787
Fax: (256) 880-8788
URL: www.generalstandards.com

The information in this document is subject to change without notice.

General Standards Corporation makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. Although extensive editing and reviews are performed before release to ECO control, **General Standards Corporation** assumes no responsibility for any errors that may exist in this document. No commitment is made to update or keep current the information contained in this document.

General Standards Corporation does not assume any liability arising out of the application or use of any product or circuit described herein, nor is any license conveyed under any patent right of any rights of others.

General Standards Corporation assumes no responsibility resulting from omissions or errors in this manual, or from the use of information contained herein.

General Standards Corporation reserves the right to make any changes, without notice, to this product to improve reliability, performance, function, or design.

RELATED PUBLICATIONS

PLX PCI 9056 Data Book

PLX Technology Inc.
390 Potrero Avenue
Sunnyvale, CA 4085
(408) 774-3735
http://www.plxtech.com/

EIA-422-A – Electrical Characteristics of Balanced Voltage Digital Interface Circuits
(EIA order number EIA-RS-422A)

EIA-485 – Standard for Electrical Characteristics of Generators and Receivers for Use in Balanced Digital Multipoint Systems
(EIA order number EIA-RS-485)

EIA Standards and Publications can be purchased from:

GLOBAL ENGINEERING DOCUMENTS
15 Inverness Way East
Englewood, CO 80112
Phone: (800) 854-7179
http://global.ihs.com/

TABLE OF CONTENTS

CHAPTER 1: INTRODUCTION

1.0 General Description

The PCIe-DIO32A-S is digital IO card which provides 32 general purpose IO signals for RS422/RS485 applications.

Features:

- One Lane PCI Express (PCIe) Interface
- RS422/RS485 Differential Transceivers
- 32 IO Bits individually configurable as Inputs or Outputs
- Outputs can be individually tri-stated
- Programmable de-glitch control for Inputs
- Inputs can be programmed to trigger an interrupt on Change of State (H-L and L-H)
- Interrupts can be individually programmed to trigger an output change on any or all Outputs
- SCSI type 68 pin front edge I/O Connector
- Breakout Board available
- Programmable 120Ω for each block of four signals
- User changeable Termination Resistors – blocks of four signals (SIPS)
- Available drivers include VxWorks, WinNT, Win2k, WinXP, Linux, and Labview
- Industrial Temperature Option Available

CHAPTER 2: LOCAL SPACE REGISTERS

2.0 Register Map

The DIO32 is accessed through two sets of registers – PCI/PCIe Registers, and GSC Firmware Registers. The GSC Firmware Registers are referred to as Local Space Registers and are described below. The PCIe registers are discussed in Chapter 3.

2.1 GSC Firmware Registers

The GSC Firmware Registers provide the primary control/status for the DIO32A board. The following table shows the GSC Firmware Registers.

Offset Address	Size	Access*	Register Name	Default Value (Hex)
0x0000	D32	Read Only	Firmware Revision	E51001XX
0x0004	D32	Read Only	Features Register	00000000
0x0008	D32	Read/Write	Board Control	00000000
0x000C	D32	Read Only	Board Status	0020000X
0x0010	D32	Read Only	Interrupt Type Register	00000000
0x0014-0x002C	---	--	RESERVED	--------
0x0030	D32	Read/Write	Termination Control	00000000
0x0034-0x003C	---	--	RESERVED	--------
0x0040	D32	Read/Write	IO Direction Register	00000000
0x044	D32	Read Only	Pin Input	XXXXXXXX
0x0048	D32	Read Only	De-Glitch Input	XXXXXXXX
0x004C	---	--	RESERVED	--------
0x0050	D32	Read/Write	Output Tri-State Register	00000000
0x0054	D32	Read/Write	Output Value Register	00000000
0x0058	D32	Read/Write	Output Clock Register	00000000
0x005C-0x006C	---	--	RESERVED	--------
0x070	D32	Read/Write	De-Glitch Control	00000000
0x0074-0x007C	---	--	RESERVED	--------
0x0080	D32	Read/Write	Prog Clock 1 Register	00000000
0x0084	D32	Read/Write	Prog Clock 1 PWM Divider	00000000
0x0088	D32	Read Only	Prog Clock 1 Frequency	00000000
0x008C	---	--	RESERVED	--------
0x0090	D32	Read/Write	Prog Clock 2 Register	00000000
0x0094	D32	Read/Write	Prog Clock 2 PWM Divider	00000000
0x0098	D32	Read Only	Prog Clock 2 Frequency	00000000
0x009C	---	--	RESERVED	--------
0x00A0	D32	Read/Write	Prog Clock 3 Register	00000000
0x00A4	D32	Read/Write	Prog Clock 3 PWM Divider	00000000
0x00A8	D32	Read Only	Prog Clock 3 Frequency	00000000
0x00AC-0x017C	---	--	RESERVED	--------
0x0180	D32	Read/Write	Lo-Hi Interrupt Enable	00000000
0x0184	D32	Read/Write	Lo-Hi Interrupt Status / Clear	00000000
0x0188	D32	Read/Write	Hi-Lo Interrupt Enable	00000000
0x018C	D32	Read/Write	Hi-Lo Interrupt Status / Clear	00000000

0x0190-0x01FC	---	--	RESERVED	--------
0x0200	D32	Read/Write	D0 Lo-Hi Output Mask	00000000
0x0204	D32	Read/Write	D0 Lo-Hi Output Tri-State	00000000
0x0208	D32	Read/Write	D0 Lo-Hi Output Value	00000000
0x020C	---	--	RESERVED	--------
0x0210	D32	Read/Write	D0 Hi-Lo Output Mask	00000000
0x0214	D32	Read/Write	D0 Hi-Lo Output Tri-State	00000000
0x0218	D32	Read/Write	D0 Hi-Lo Output Value	00000000
0x021C	---	--	RESERVED	--------
0x0220	D32	Read/Write	D1 Lo-Hi Output Mask	00000000
0x0224	D32	Read/Write	D1 Lo-Hi Output Tri-State	00000000
0x0228	D32	Read/Write	D1 Lo-Hi Output Value	00000000
0x022C	---	--	RESERVED	--------
0x0230	D32	Read/Write	D1 Hi-Lo Output Mask	00000000
0x0234	D32	Read/Write	D1 Hi-Lo Output Tri-State	00000000
0x0238	D32	Read/Write	D1 Hi-Lo Output Value	00000000
0x023C	---	--	RESERVED	--------
0x0240	D32	Read/Write	D2 Lo-Hi Output Mask	00000000
0x0244	D32	Read/Write	D2 Lo-Hi Output Tri-State	00000000
0x0248	D32	Read/Write	D2 Lo-Hi Output Value	00000000
0x024C	---	--	RESERVED	--------
0x0250	D32	Read/Write	D2 Hi-Lo Output Mask	00000000
0x0254	D32	Read/Write	D2 Hi-Lo Output Tri-State	00000000
0x0258	D32	Read/Write	D2 Hi-Lo Output Value	00000000
0x025C	---	--	RESERVED	--------
0x0260	D32	Read/Write	D3 Lo-Hi Output Mask	00000000
0x0264	D32	Read/Write	D3 Lo-Hi Output Tri-State	00000000
0x0268	D32	Read/Write	D3 Lo-Hi Output Value	00000000
0x026C	---	--	RESERVED	--------
0x0270	D32	Read/Write	D3 Hi-Lo Output Mask	00000000
0x0274	D32	Read/Write	D3 Hi-Lo Output Tri-State	00000000
0x0278	D32	Read/Write	D3 Hi-Lo Output Value	00000000
0x027C	---	--	RESERVED	--------
0x0280	D32	Read/Write	D4 Lo-Hi Output Mask	00000000
0x0284	D32	Read/Write	D4 Lo-Hi Output Tri-State	00000000
0x0288	D32	Read/Write	D4 Lo-Hi Output Value	00000000
0x028C	---	--	RESERVED	--------
0x0290	D32	Read/Write	D4Hi-Lo Output Mask	00000000
0x0294	D32	Read/Write	D4 Hi-Lo Output Tri-State	00000000
0x0298	D32	Read/Write	D4 Hi-Lo Output Value	00000000
0x029C	---	--	RESERVED	--------
0x02A0	D32	Read/Write	D5 Lo-Hi Output Mask	00000000
0x02A4	D32	Read/Write	D5 Lo-Hi Output Tri-State	00000000
0x02A8	D32	Read/Write	D5 Lo-Hi Output Value	00000000
0x02AC	---	--	RESERVED	--------
0x02B0	D32	Read/Write	D5 Hi-Lo Output Mask	00000000
0x02B4	D32	Read/Write	D5 Hi-Lo Output Tri-State	00000000
0x02B8	D32	Read/Write	D5 Hi-Lo Output Value	00000000
0x02BC	---	--	RESERVED	--------

0x02C0	D32	Read/Write	D6 Lo-Hi Output Mask	00000000
0x02C4	D32	Read/Write	D6 Lo-Hi Output Tri-State	00000000
0x02C8	D32	Read/Write	D6 Lo-Hi Output Value	00000000
0x02CC	---	--	RESERVED	--------
0x02D0	D32	Read/Write	D6 Hi-Lo Output Mask	00000000
0x02D4	D32	Read/Write	D6 Hi-Lo Output Tri-State	00000000
0x02D8	D32	Read/Write	D6 Hi-Lo Output Value	00000000
0x02DC	---	--	RESERVED	--------
0x02E0	D32	Read/Write	D7 Lo-Hi Output Mask	00000000
0x02E4	D32	Read/Write	D7 Lo-Hi Output Tri-State	00000000
0x02E8	D32	Read/Write	D7 Lo-Hi Output Value	00000000
0x02EC	---	--	RESERVED	--------
0x02F0	D32	Read/Write	D7 Hi-Lo Output Mask	00000000
0x02F4	D32	Read/Write	D7 Hi-Lo Output Tri-State	00000000
0x02F8	D32	Read/Write	D7 Hi-Lo Output Value	00000000
0x02FC	---	--	RESERVED	--------
0x0300	D32	Read/Write	D8 Lo-Hi Output Mask	00000000
0x0304	D32	Read/Write	D8 Lo-Hi Output Tri-State	00000000
0x0308	D32	Read/Write	D8 Lo-Hi Output Value	00000000
0x030C	---	--	RESERVED	--------
0x0310	D32	Read/Write	D8 Hi-Lo Output Mask	00000000
0x0314	D32	Read/Write	D8 Hi-Lo Output Tri-State	00000000
0x0318	D32	Read/Write	D8 Hi-Lo Output Value	00000000
0x031C	---	--	RESERVED	--------
0x0320	D32	Read/Write	D9 Lo-Hi Output Mask	00000000
0x0324	D32	Read/Write	D9 Lo-Hi Output Tri-State	00000000
0x0328	D32	Read/Write	D9 Lo-Hi Output Value	00000000
0x032C	---	--	RESERVED	--------
0x0330	D32	Read/Write	D9 Hi-Lo Output Mask	00000000
0x0334	D32	Read/Write	D9 Hi-Lo Output Tri-State	00000000
0x0338	D32	Read/Write	D9 Hi-Lo Output Value	00000000
0x033C	---	--	RESERVED	--------
0x0340	D32	Read/Write	D10 Lo-Hi Output Mask	00000000
0x0344	D32	Read/Write	D10 Lo-Hi Output Tri-State	00000000
0x0348	D32	Read/Write	D10 Lo-Hi Output Value	00000000
0x034C	---	--	RESERVED	--------
0x0350	D32	Read/Write	D10 Hi-Lo Output Mask	00000000
0x0354	D32	Read/Write	D10 Hi-Lo Output Tri-State	00000000
0x0358	D32	Read/Write	D10 Hi-Lo Output Value	00000000
0x035C	---	--	RESERVED	--------
0x0360	D32	Read/Write	D11 Lo-Hi Output Mask	00000000
0x0364	D32	Read/Write	D11 Lo-Hi Output Tri-State	00000000
0x0368	D32	Read/Write	D11 Lo-Hi Output Value	00000000
0x036C	---	--	RESERVED	--------
0x0370	D32	Read/Write	D11 Hi-Lo Output Mask	00000000
0x0374	D32	Read/Write	D11 Hi-Lo Output Tri-State	00000000
0x0378	D32	Read/Write	D11 Hi-Lo Output Value	00000000
0x037C	---	--	RESERVED	--------
0x0380	D32	Read/Write	D12 Lo-Hi Output Mask	00000000

0x0384	D32	Read/Write	D12 Lo-Hi Output Tri-State	00000000
0x0388	D32	Read/Write	D12 Lo-Hi Output Value	00000000
0x038C	---	--	RESERVED	--------
0x0390	D32	Read/Write	D12 Hi-Lo Output Mask	00000000
0x0394	D32	Read/Write	D12 Hi-Lo Output Tri-State	00000000
0x0398	D32	Read/Write	D12 Hi-Lo Output Value	00000000
0x039C	---	--	RESERVED	--------
0x03A0	D32	Read/Write	D13 Lo-Hi Output Mask	00000000
0x03A4	D32	Read/Write	D13 Lo-Hi Output Tri-State	00000000
0x03A8	D32	Read/Write	D13 Lo-Hi Output Value	00000000
0x03AC	---	--	RESERVED	--------
0x03B0	D32	Read/Write	D13 Hi-Lo Output Mask	00000000
0x03B4	D32	Read/Write	D13 Hi-Lo Output Tri-State	00000000
0x03B8	D32	Read/Write	D13 Hi-Lo Output Value	00000000
0x03BC	---	--	RESERVED	--------
0x03C0	D32	Read/Write	D14 Lo-Hi Output Mask	00000000
0x03C4	D32	Read/Write	D14 Lo-Hi Output Tri-State	00000000
0x03C8	D32	Read/Write	D14 Lo-Hi Output Value	00000000
0x03CC	---	--	RESERVED	--------
0x03D0	D32	Read/Write	D14 Hi-Lo Output Mask	00000000
0x03D4	D32	Read/Write	D14 Hi-Lo Output Tri-State	00000000
0x03D8	D32	Read/Write	D14 Hi-Lo Output Value	00000000
0x03DC	---	--	RESERVED	--------
0x03E0	D32	Read/Write	D15 Lo-Hi Output Mask	00000000
0x03E4	D32	Read/Write	D15 Lo-Hi Output Tri-State	00000000
0x03E8	D32	Read/Write	D15 Lo-Hi Output Value	00000000
0x03EC	---	--	RESERVED	--------
0x03F0	D32	Read/Write	D15 Hi-Lo Output Mask	00000000
0x03F4	D32	Read/Write	D15 Hi-Lo Output Tri-State	00000000
0x03F8	D32	Read/Write	D15 Hi-Lo Output Value	00000000
0x03FC	---	--	RESERVED	--------
0x0400	D32	Read/Write	D16 Lo-Hi Output Mask	00000000
0x0404	D32	Read/Write	D16 Lo-Hi Output Tri-State	00000000
0x0408	D32	Read/Write	D16 Lo-Hi Output Value	00000000
0x040C	---	--	RESERVED	--------
0x0410	D32	Read/Write	D16 Hi-Lo Output Mask	00000000
0x0414	D32	Read/Write	D16 Hi-Lo Output Tri-State	00000000
0x0418	D32	Read/Write	D16 Hi-Lo Output Value	00000000
0x041C	---	--	RESERVED	--------
0x0420	D32	Read/Write	D17 Lo-Hi Output Mask	00000000
0x0424	D32	Read/Write	D17 Lo-Hi Output Tri-State	00000000
0x0428	D32	Read/Write	D17 Lo-Hi Output Value	00000000
0x042C	---	--	RESERVED	--------
0x0430	D32	Read/Write	D17 Hi-Lo Output Mask	00000000
0x0434	D32	Read/Write	D17 Hi-Lo Output Tri-State	00000000
0x0438	D32	Read/Write	D17 Hi-Lo Output Value	00000000
0x043C	---	--	RESERVED	--------
0x0440	D32	Read/Write	D18 Lo-Hi Output Mask	00000000
0x0444	D32	Read/Write	D18 Lo-Hi Output Tri-State	00000000

0x0448	D32	Read/Write	D18 Lo-Hi Output Value	00000000
0x044C	---	--	RESERVED	--------
0x0450	D32	Read/Write	D18 Hi-Lo Output Mask	00000000
0x0454	D32	Read/Write	D18 Hi-Lo Output Tri-State	00000000
0x0458	D32	Read/Write	D18 Hi-Lo Output Value	00000000
0x045C	---	--	RESERVED	--------
0x0460	D32	Read/Write	D19 Lo-Hi Output Mask	00000000
0x0464	D32	Read/Write	D19 Lo-Hi Output Tri-State	00000000
0x0468	D32	Read/Write	D19 Lo-Hi Output Value	00000000
0x046C	---	--	RESERVED	--------
0x0470	D32	Read/Write	D19 Hi-Lo Output Mask	00000000
0x0474	D32	Read/Write	D19 Hi-Lo Output Tri-State	00000000
0x0478	D32	Read/Write	D19 Hi-Lo Output Value	00000000
0x047C	---	--	RESERVED	--------
0x0480	D32	Read/Write	D20 Lo-Hi Output Mask	00000000
0x0484	D32	Read/Write	D20 Lo-Hi Output Tri-State	00000000
0x0488	D32	Read/Write	D20 Lo-Hi Output Value	00000000
0x048C	---	--	RESERVED	--------
0x0490	D32	Read/Write	D20 Hi-Lo Output Mask	00000000
0x0494	D32	Read/Write	D20 Hi-Lo Output Tri-State	00000000
0x0498	D32	Read/Write	D20 Hi-Lo Output Value	00000000
0x049C	---	--	RESERVED	--------
0x04A0	D32	Read/Write	D21 Lo-Hi Output Mask	00000000
0x04A4	D32	Read/Write	D21 Lo-Hi Output Tri-State	00000000
0x04A8	D32	Read/Write	D21 Lo-Hi Output Value	00000000
0x04AC	---	--	RESERVED	--------
0x04B0	D32	Read/Write	D21 Hi-Lo Output Mask	00000000
0x04B4	D32	Read/Write	D21 Hi-Lo Output Tri-State	00000000
0x04B8	D32	Read/Write	D21 Hi-Lo Output Value	00000000
0x04BC	---	--	RESERVED	--------
0x04C0	D32	Read/Write	D22 Lo-Hi Output Mask	00000000
0x04C4	D32	Read/Write	D22 Lo-Hi Output Tri-State	00000000
0x04C8	D32	Read/Write	D22 Lo-Hi Output Value	00000000
0x04CC	---	--	RESERVED	--------
0x04D0	D32	Read/Write	D22 Hi-Lo Output Mask	00000000
0x04D4	D32	Read/Write	D22 Hi-Lo Output Tri-State	00000000
0x04D8	D32	Read/Write	D22 Hi-Lo Output Value	00000000
0x04DC	---	--	RESERVED	--------
0x04E0	D32	Read/Write	D23 Lo-Hi Output Mask	00000000
0x04E4	D32	Read/Write	D23 Lo-Hi Output Tri-State	00000000
0x04E8	D32	Read/Write	D23 Lo-Hi Output Value	00000000
0x04EC	---	--	RESERVED	--------
0x04F0	D32	Read/Write	D23 Hi-Lo Output Mask	00000000
0x04F4	D32	Read/Write	D23 Hi-Lo Output Tri-State	00000000
0x04F8	D32	Read/Write	D23 Hi-Lo Output Value	00000000
0x04FC	---	--	RESERVED	--------
0x0500	D32	Read/Write	D24 Lo-Hi Output Mask	00000000
0x0504	D32	Read/Write	D24 Lo-Hi Output Tri-State	00000000
0x0508	D32	Read/Write	D24 Lo-Hi Output Value	00000000

0x050C	---	--	RESERVED	--------
0x0510	D32	Read/Write	D24 Hi-Lo Output Mask	00000000
0x0514	D32	Read/Write	D24 Hi-Lo Output Tri-State	00000000
0x0518	D32	Read/Write	D24 Hi-Lo Output Value	00000000
0x051C	---	--	RESERVED	--------
0x0520	D32	Read/Write	D25 Lo-Hi Output Mask	00000000
0x0524	D32	Read/Write	D25 Lo-Hi Output Tri-State	00000000
0x0528	D32	Read/Write	D25 Lo-Hi Output Value	00000000
0x052C	---	--	RESERVED	--------
0x0530	D32	Read/Write	D25 Hi-Lo Output Mask	00000000
0x0534	D32	Read/Write	D25 Hi-Lo Output Tri-State	00000000
0x0538	D32	Read/Write	D25 Hi-Lo Output Value	00000000
0x053C	---	--	RESERVED	--------
0x0540	D32	Read/Write	D26 Lo-Hi Output Mask	00000000
0x0544	D32	Read/Write	D26 Lo-Hi Output Tri-State	00000000
0x0548	D32	Read/Write	D26 Lo-Hi Output Value	00000000
0x054C	---	--	RESERVED	--------
0x0550	D32	Read/Write	D26 Hi-Lo Output Mask	00000000
0x0554	D32	Read/Write	D26 Hi-Lo Output Tri-State	00000000
0x0558	D32	Read/Write	D26 Hi-Lo Output Value	00000000
0x055C	---	--	RESERVED	--------
0x0560	D32	Read/Write	D27 Lo-Hi Output Mask	00000000
0x0564	D32	Read/Write	D27 Lo-Hi Output Tri-State	00000000
0x0568	D32	Read/Write	D27 Lo-Hi Output Value	00000000
0x056C	---	--	RESERVED	--------
0x0570	D32	Read/Write	D27 Hi-Lo Output Mask	00000000
0x0574	D32	Read/Write	D27 Hi-Lo Output Tri-State	00000000
0x0578	D32	Read/Write	D27 Hi-Lo Output Value	00000000
0x057C	---	--	RESERVED	--------
0x0580	D32	Read/Write	D28 Lo-Hi Output Mask	00000000
0x0584	D32	Read/Write	D28 Lo-Hi Output Tri-State	00000000
0x0588	D32	Read/Write	D28 Lo-Hi Output Value	00000000
0x058C	---	--	RESERVED	--------
0x0590	D32	Read/Write	D28 Hi-Lo Output Mask	00000000
0x0594	D32	Read/Write	D28 Hi-Lo Output Tri-State	00000000
0x0598	D32	Read/Write	D28 Hi-Lo Output Value	00000000
0x059C	---	--	RESERVED	--------
0x05A0	D32	Read/Write	D29 Lo-Hi Output Mask	00000000
0x05A4	D32	Read/Write	D29 Lo-Hi Output Tri-State	00000000
0x05A8	D32	Read/Write	D29 Lo-Hi Output Value	00000000
0x05AC	---	--	RESERVED	--------
0x05B0	D32	Read/Write	D29 Hi-Lo Output Mask	00000000
0x05B4	D32	Read/Write	D29 Hi-Lo Output Tri-State	00000000
0x05B8	D32	Read/Write	D29 Hi-Lo Output Value	00000000
0x05BC	---	--	RESERVED	--------
0x05C0	D32	Read/Write	D30 Lo-Hi Output Mask	00000000
0x05C4	D32	Read/Write	D30 Lo-Hi Output Tri-State	00000000
0x05C8	D32	Read/Write	D30 Lo-Hi Output Value	00000000
0x05CC	---	--	RESERVED	--------

0x05D0	D32	Read/Write	D30 Hi-Lo Output Mask	00000000
0x05D4	D32	Read/Write	D30 Hi-Lo Output Tri-State	00000000
0x05D8	D32	Read/Write	D30 Hi-Lo Output Value	00000000
0x05DC	---	--	RESERVED	--------
0x05E0	D32	Read/Write	D31 Lo-Hi Output Mask	00000000
0x05E4	D32	Read/Write	D31 Lo-Hi Output Tri-State	00000000
0x05E8	D32	Read/Write	D31 Lo-Hi Output Value	00000000
0x05EC	---	--	RESERVED	--------
0x05F0	D32	Read/Write	D31 Hi-Lo Output Mask	00000000
0x05F4	D32	Read/Write	D31 Hi-Lo Output Tri-State	00000000
0x05F8	D32	Read/Write	D31 Hi-Lo Output Value	00000000
0x05FC-0x0FFC	---	--	RESERVED	--------
0x1000-0x17FC	D32	Read/Write	Re-Configuration Registers	--------

2.1.1 Firmware Revision: Local Offset 0x0000

The Firmware ID register provides version information about the firmware on the board. This is useful for technical support to identify the firmware version. See Appendix B for more detailed information.

D31:16	HW Board Rev	E511 = PCIe-DIO32A Rev A
D15:8	Firmware Type ID	00 = DIO32A Standard
D7:0	Firmware Revision	Firmware Version

2.1.1 Features Revision: Local Offset 0x0004

The Features Register allows software to account for added features in the firmware versions. Bits will be assigned as new features are added. See Appendix B for more details.

D31:D0	RESERVED

2.1.2 Board Control: Local Offset 0x0008

The Board Control Register defines the general control functions for the board.

D31	Board Reset 1 = Reset all Local Registers to their default values **Notes:** This bit will automatically clear to 0 following the board reset. Board Reset will NOT reset programmable oscillator. Following a Board Reset, Reset-In-Progress bit (D31) of the Board Status Register will remain set until the Board reset is complete;
D30	Test Mode (Allows interrupts to be triggered via Outputs)
D29	Test Mode (Disables Irq)
D28:D12	RESERVED
D11	LED D5 1 = Turn on Red LED
D10	LED D5 1 = Turn on Green LED
D9	LED D4 1 = Turn on Red LED
D8	LED D4 1 = Turn on Green LED
D7	LED D3 1 = Turn on Red LED
D6	LED D3 1 = Turn on Green LED
D5	LED D2 1 = Turn on Red LED
D4	LED D2 1 = Turn on Green LED
D3	LED D1 1 = Turn on Red LED
D2	LED D1 1 = Turn on Green LED
D1	LED D0 1 = Turn on Red LED
D0	LED D0 1 = Turn on Green LED

2.1.3 Board Status: Local Offset 0x000C

The Board Status Register gives general overall status for a board. The Board Jumpers (D1:D0) are physical jumpers which can be used to distinguish between boards if multiple DIO32A boards are present in a system.

D31:D16	0x0020 = Number of IO bits
D15:D14	RESERVED
D13:D4	Configuration ID (Reserved)
D3:D0	Board Jumper (J2)
D3	Board ID4 0=J2:7-J2:8 jumper installed
D2	Board ID3 0=J2:5-J2:6 jumper installed
D1	Board ID2 0=J2:3-J2:4 jumper installed
D0	Board ID1 0=J2:1-J2:2 jumper installed

2.1.4 Interrupt Type : Local Offset 0x0010

Defines Interrupt Type Currently Asserted.

D31:D2	RESERVED
D1	Hi-Lo Interrupt asserted
D0	Lo-Hi Interrupt asserted

2.1.5 Termination Control : Local Offset 0x0030

This register controls the 120 Ohm termination in the transceiver. The termination is in groups of 4 – if any terminator in a block is enabled, all will be enabled.

D31:D0	1 = Enable 120 Ohm termination

2.1.6 IO Direction : Local Offset 0x0040

Defines IO signals as Input or Output

D31:D0	0 = Input / 1 = Output

2.1.7 Pin Input : Local Offset 0x0044

This register reads the instantaneous IO value at the pin (inputs and outputs)

D31:D0	Pin IO Values

2.1.8 De-Glitched Input : Local Offset 0x0048

This register reads the input value after the de-glitch filter

D31:D0	Deglitched Iinput Values

2.1.9 Output Tri-State : Local Offset 0x0050

If a signal is defined as output, the register will determine if the output is tri-stated

D31:D0 0 = Driven/ 1 = Tri-state

2.1.10 Output Value : Local Offset 0x0054

If a signal is defined as output, the register will define the output value. Note if an output is defined as clock, repeat, or tristate, this value will be ignored.

D31:D0 0 = Low / 1 = High

2.1.11 Output Clock : Local Offset 0x0058

This register allows 16 of the outputs to be sourced from one of 3 programmable clocks. Only D0:D3, D8:D11, D16:D19, and D24:D27 may be set as clock outputs.

For each Output;
00=No Clock
01=Clock 1
10=Clock 2
11 = Clock 3.

D31:D30	Reserved
D29:D28	D28 Clock Select
D27:D26	Reserved
D24:D25	D24 Clock Select
D22:D23	Reserved
D20:D21	D20 Clock Select
D18:D19	Reserved
D16:D17	D16 Clock Select
D14:D15	Reserved
D12:D13	D12 Clock Select
D10:D11	Reserved
D8:D9	D8 Clock Select
D6:D7	Reserved
D4:D5	D4 Clock Select
D2:D3	Reserved
D1:D0	D0 Clock Select

2.1.12 De-Glitch Control : Local Offset 0x0070

This register sets up the de-glitch filter

D31:D8	Sample rate – min 100ns Defines the sample increment – number of 100ns clocks
D7:D0	Glitch filter Defines the number of samples an input must be stable before it is latched

2.1.13 Programmable Clock x : Local Offset 0x0080 / 0x0090 / 0x00A0

Defines Programmable PLL Clock setup

D31:D0 TBD

2.1.14 Programmable Clock x PWM Divider : Local Offset 0x0084 / 0x0094 / 0x00A4

Defines Programmable PLL Clock Post Divider

D31:D0 TBD

2.1.15 Programmable Clock x Frequency : Local Offset 0x0088 / 0x0098 / 0x00A8

Defines Programmable Clock Frequency

D31:D0 Programmable Clock Frequency

2.1.16 Lo-Hi Interrupt Enable: Local Offset 0x0180

D31:D0 Interrupt on Lo-Hi transition of deglitched input signal

2.1.17 Lo-Hi Interrupt Status / Clear: Local Offset 0x0184

Read:
D31:D0 0 = No Interrupt / 1 = Interrupt Latched

Write:
D31:D0 1 = Clear Latched Interrupt

2.1.18 Hi-Lo Interrupt Enable: Local Offset 0x0188

D31:D0 Interrupt on Hi-Lo transition of deglitched input signal

2.1.19 Hi-Lo Interrupt Status / Clear: Local Offset 0x018C

Read:
D31:D0 0 = No Interrupt / 1 = Interrupt Latched

Write:
D31:D0 1 = Clear Latched Interrupt

2.1.20 Lo-Hi Dx Output Mask: Local Offset 0x0200 – 0x05E0

D31:D0 Defines output signals to be set/cleared on Dx Lo-Hi de-glitched transition

2.1.21 Lo-Hi Dx Output Tristate: Local Offset 0x0204 - 0x05E4

D31:D0 Defines outputs to be Tri-Stated on Dx Lo-Hi de-glitched transition

2.1.22 Lo-Hi Dx Output Value: Local Offset 0x0208 – 0x05E8

D31:D0 Defines output values to be set/cleared on Dx Lo-Hi de-glitched transition

2.1.23 Hi-Lo Dx Output Mask: Local Offset 0x0210 – 0x05F0

D31:D0 Defines output signals to be set/cleared on Dx Hi-Lo de-glitched transition

2.1.24 Hi-Lo Dx Output Tristate: Local Offset 0x0214 - 0x05F4

D31:D0 Defines outputs to be Tri-Stated on Dx Hi-Lo de-glitched transition

2.1.25 Hi-Lo Dx Output Value: Local Offset 0x0218 – 0x05F8

D31:D0 Defines output values to be set/cleared on Dx Hi-Lo de-glitched transition

CHAPTER 3: PROGRAMMING

3.0 Introduction

CHAPTER 4: PCI INTERFACE

4.0 PCI Interface Registers

The PMC/PCI interface is handled by a PCI9056 I/O Accelerator from PLX Technology. The PCI interface is compliant with the 5V, 66MHz 32-bit PCI Specification 2.2. The PCI9056 provides dual DMA controllers for fast data transfers to and from the on-board FIFOs. Fast DMA burst accesses provide for a maximum burst throughput of 264MB/s to the PCI interface.

Since many features of the PCI9056 are not utilized in this design, it is beyond the scope of this document to duplicate the PCI9056 User's Manual. Only those features, which will clarify areas specific to the PCIe-DIO32Aare detailed here. Please refer to the PCI9056 User's Manual (See Related Publications) for more detailed information. Note that the BIOS configuration and software driver will handle most of the PCI9056 interface. Unless the user is writing a device driver, the details of this PCI Interface Chapter may be skipped.

4.1 PCI Registers

The PLX 9056 contains many registers, many of which have no effect on the DIO32A performance. The following section attempts to filter the information from the PCI9056 manual to provide the necessary information for a DIO32A specific driver.

The DIO32A uses an on-board serial EEPROM to initialize many of the PCI9056 registers after a PCI Reset. This allows board specific information to be preconfigured correctly.

4.1.1 PCI Configuration Registers

The PCI Configuration Registers allow the PCI controller to identify and control the cards in a system.

PCI device identification is provided by the Vendor ID/Device ID (Addr 0x0000) and Sub-Vendor ID/Sub-Device ID Registers (0x002C). The following definitions are unique to the General Standards DIO323A boards. All drivers should verify the ID/Sub-ID information before attaching to this card. These values are fixed via the Serial EEPROM load following a PCI Reset, and cannot be changed by software.

Vendor ID	0x10B5	PLX Technology
Device ID	0x9056	PCI9056
Sub-Vendor ID	0x10B5	PLX Technology
Sub-Device ID	0x3198	GSC SIO4B

The configuration registers also setup the PCI IO and Memory mapping for the DIO32A. The PCI9056 is setup to use PCIBAR0 and PCIBAR1 to map the internal PLX registers into PCI Memory and IO space respectively. PCIBAR2 will map the Local Space Registers into PCI memory space, and PCIBAR3 is unused. Typically, the OS will configure the PCI configuration space.

For further information of the PCI configuration registers, please consult the PLX Technology PCI9056 Manual.

4.1.2 Local Configuration Registers

The Local Configuration registers give information on the Local side implementation. These include the required memory size. The DIO32A memory size is initialized to 32k Bytes. All other Local Registers initialize to the default values described in the PCI9056 Manual.

4.1.3 Runtime Registers

The Runtime registers consist of mailbox registers, doorbell registers, and a general-purpose control register. The mailbox and doorbell registers are not used and serve no purpose on the DIO32A. All other Runtime Registers initialize to the default values described in the PCI9056 Manual.

4.1.4 DMA Registers

The Local DMA registers are not used on the DIO32A.

CHAPTER 5: HARDWARE CONFIGURATION

5.0 Board Layout

The following figure is a drawing of the physical components of the PCIe-DIO32A:

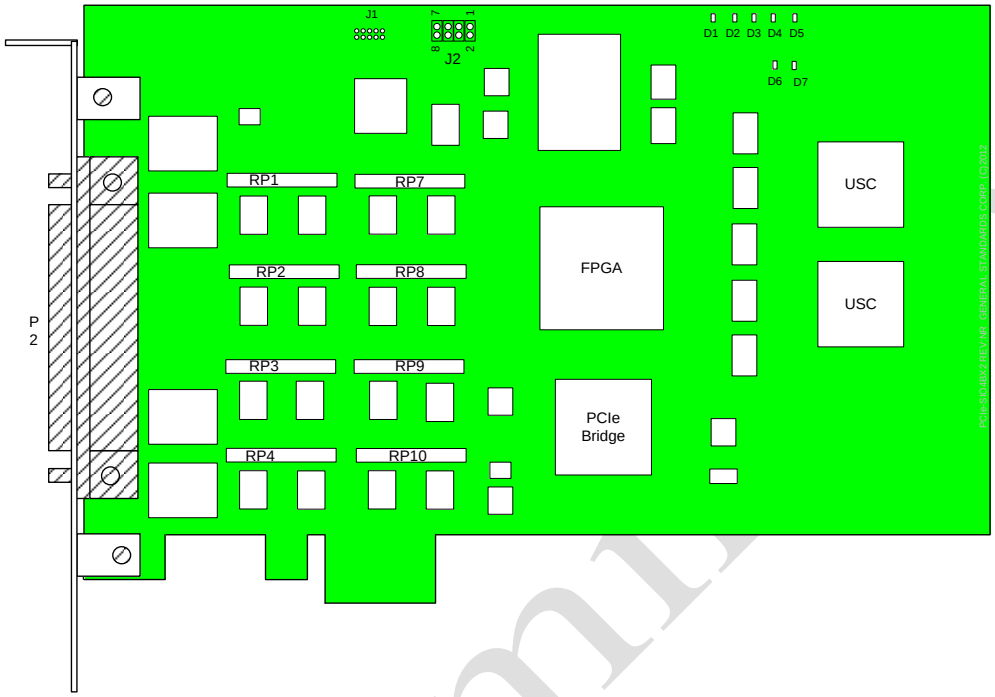


Figure 5-1: Board Layout – Top

5.1 Board ID Jumper J2

Jumper J2 allows the user to set the Board ID in the Board Status Register (See Section 2.1.3). This is useful to uniquely identify a board if more than one DIO32A card is in a system. When the Board ID jumper is installed, it will read '1' in the Board Status Register. The Board Status Register bit will report '0' when the jumper is removed. Refer to Figure 5-1 for Jumper J2 location.

J2 Jumper	Description	Notes
1 - 2	Board ID 1	Board ID 1 in Board Status Register (D0)
3 - 4	Board ID 2	Board ID 2 in Board Status Register (D1)
5 - 6	Board ID 3	Board ID 3 in Board Status Register (D2)
7 - 8	Board ID 4	Board ID 4 in Board Status Register (D3)

5.2 Termination Resistors

The PCIe-DIO32 transceivers have built in 120 Ohm parallel termination resistors for the RS-422/RS485 mode. If desired, the internal termination resistors may be disabled by setting bit D30 in the Pin Source Register.

The board is designed with socketed external parallel termination (if a different value than the internal termination is required). The external termination resistors are 8 pin SIPs. There are 8 termination SIPs – RP1-RP4, RP7-RP10. The external parallel resistors are for RS422/RS485 termination only. Refer to Figure 5-1 for resistor pack locations.

Please contact quotes@generalstandards.com if a different termination value is required.

5.3 LEDs

Five bicolor LEDs (D1-D5) are accessible via software. Refer to Figure 5-1 for these LED locations.

LED D1 is controlled from the Board Control Register. LED_D1 Red is controlled by D25, and LED_D1 Green is controlled D24

The remaining 4 LEDs are controlled from D23:D20 of the four Channel Control Registers. Each Channel Control Register controls 1 LED. If D23:D22="10", the Red LED will turn off. Likewise, if D23:D22="11", the Red LED will turn on. D21:D20 controls the Green LED in the pair.

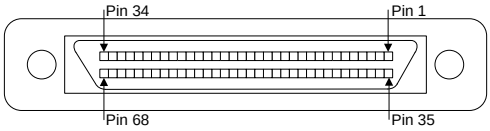
LED_D2 is controlled by Ch 4
LED_D3 is controlled by Ch 3
LED_D4 is controlled by Ch 2
LED_D5 is controlled by Ch 1

.Additionally, if all the LED controls are set to 0 in all four of the Channel Control Registers (power up default), the LEDs will display the lower 4 bits of the firmware revision in Green LED_D2 to LED_D5.

The remaining LED (D6) display the firmware status. This LED should flash at power up or after a PCIe reset, then will turn off. The LED should be off during normal operation.

5.4 Interface Connector

User I/O Connector: 68-pin SCSI connector (female) (P2)
Part Number: AMP/TYCO 787170-7
Mating Connector: AMP/TYCO 749111-6 (or equivalent)



Pin #	RS422/RS485	Pin #	RS422/RS485
1	D0p	35	D16p
2	D0n	36	D16n
3	D1p	37	D17p
4	D1n	38	D17n
5	D2p	39	D18p
6	D2n	40	D18n
7	D3p	41	D19p
8	D3n	42	D19n
9	D4p	43	D20p
10	D4n	44	D20n
11	D5p	45	D21p
12	D5n	46	D21n
13	D6p	47	D22p
14	D6n	48	D22n
15	D7p	49	D23p
16	D7n	50	D23n
17	GND1	51	GND3
18	GND2	52	GND4
19	D8p	53	D24p
20	D8n	54	D24n
21	D9p	55	D25p
22	D9n	56	D25n
23	D10p	57	D26p
24	D10n	58	D26n
25	D11p	59	D27p
26	D11n	60	D27n
27	D12p	61	D28p
28	D12n	62	D28n
29	D13p	63	D29p
30	D13n	64	D29n
31	D14p	65	D30p
32	D14n	66	D30n
33	D15p	67	D31p
34	D15n	68	D31n

Table 1- Front Panel (P2) IO Connections

CHAPTER 6: ORDERING OPTIONS

6.0 Ordering Information

PCIe – DIO32A - S - <*Temperature*>

Option	Valid Selections	Description
Temperature	<blank>	0°C to +70°C – Commercial (Standard)
	I	-40°C to +85°C – Industrial

6.1 Interface Cable

General Standards Corporation can provide an interface cable for the DIO32Aboard. This standard cable is a twisted pair cable for increased noise immunity. Several standard cable lengths are offered, or the cable length can be custom ordered to the user's needs. Versions of the cable are available with connectors on both ends, or the cable may be ordered with a single connector to allow the user to adapt the other end for a specific application. A standard cable is available which will breakout the serial channels into eight DB25 connectors. Shielded cable options are also available. Please consult our sales department for more information on cabling options and pricing.

6.2 Device Drivers

General Standards has developed many device drivers for The DIO32A boards, including VxWorks, Windows, Linux, and LabView. As new drivers are always being added, please consult our website (www.generalstandards.com) or consult our sales department for a complete list of available drivers and pricing.

6.3 Custom Applications

Although the DIO32A board provides extensive flexibility to accommodate most user applications, a user application may require modifications to conform to a specialized user interface. General Standards Corporation has worked with many customers to provide customized versions based on the DIO32A boards. Please consult our sales department with your specifications to inquire about a custom application

APPENDIX A: PROGRAMMABLE OSCILLATOR PROGRAMMING

Channel Clock Post-Dividers:

The Control Word defines 4 fields for Channel Clock Post-dividers. These post-dividers will further divide down the input clock from the programmable oscillator to provide for slow baud rates. Each 4 bit field will allow a post divider of 2^n. For example, if the post-divider value=0, the input clock is not post-divided. A value of 2 will provide a post-divide of 4 (2^2). This will allow for a post-divide value of up to 32768 (2^15) for each input clock. Bit D7 of the Control word qualifies writes to the post-divide registers. This allows other bits in the command register to be set while the post-divide values are maintained.

Channel Clock Measurement:

The Control Word defines 4 bits which will select one of the 4 channel clocks (input clock + post-divide) for a measurement. This will allow the user feedback as to whether the programmable oscillator was programmed correctly. To measure a clock, select the clock to measure in the Control word, and also clear Bit D6 to allow for readback of the result. Read back the Status Word until D2 is set. Status Word D31-D8 should contain a value representing 1/10 the measured clock frequency (Value * 10 = Measured Frequency in MHz). Keep in mind that this value will not be exactly the programmed frequency due to the 100ppm (0.01%) accuracy of the on-board reference.

The Internal RAM is defined as follows: RAM Address 0x08–0x57 correspond directly to the CY22393 registers.

Address	Description	Default Value
0x00 – 0x05	Reserved (Unused)	0x00
0x06	Reserved	0xD2
0x07	Reserved	0x08
0x08	ClkA Divisor (Setup0)	0x01
0x09	ClkA Divisor (Setup1)	0x01
0x0A	ClkB Divisor (Setup0)	0x01
0x0B	ClkB Divisor (Setup1)	0x01
0x0C	ClkC Divisor	0x01
0x0D	ClkD Divisor	0x01
0x0E	Source Select	0x00
0x0F	Bank Select	0x50
0x10	Drive Setting	0x55
0x11	PLL2 Q	0x00
0x12	PLL2 P Lo	0x00
0x13	PLL2 Enable/PLL2 P Hi	0x00
0x14	PLL3 Q	0x00
0x15	PLL3 P Lo	0x00
0x16	PLL3 Enable/PLL3 P Hi	0x00
0x17	OSC Setting	0x00
0x18	Reserved	0x00
0x19	Reserved	0x00
0x1A	Reserved	0xE9
0x1B	Reserved	0x08
0x1C-0x3F	Reserved (Unused)	0x00
0x40	PLL1 Q (Setup0)	0x00
0x41	PLL1 P Lo 0 (Setup0)	0x00
0x41	PLL1 Enable/PLL1 P Hi (Setup0)	0x00
0x43	PLL1 Q (Setup1)	0x00
0x44	PLL1 P Lo 0 (Setup1)	0x00
0x45	PLL1 Enable/PLL1 P Hi (Setup1)	0x00
0x46	PLL1 Q (Setup2)	0x00
0x47	PLL1 P Lo 0 (Setup2)	0x00
0x48	PLL1 Enable/PLL1 P Hi (Setup2)	0x00
0x49	PLL1 Q (Setup3)	0x00
0x4A	PLL1 P Lo 0 (Setup3)	0x00
0x4B	PLL1 Enable/PLL1 P Hi (Setup3)	0x00
0x4C	PLL1 Q (Setup4)	0x00
0x4D	PLL1 P Lo 0 (Setup4)	0x00
0x4E	PLL1 Enable/PLL1 P Hi (Setup4)	0x00
0x4F	PLL1 Q (Setup5)	0x00
0x50	PLL1 P Lo 0 (Setup5)	0x00
0x51	PLL1 Enable/PLL1 P Hi (Setup5)	0x00
0x52	PLL1 Q (Setup6)	0x00
0x53	PLL1 P Lo 0 (Setup6)	0x00
0x54	PLL1 Enable/PLL1 P Hi (Setup6)	0x00
0x55	PLL1 Q (Setup7)	0x00
0x56	PLL1 P Lo 0 (Setup7)	0x00
0x57	PLL1 Enable/PLL1 P Hi (Setup7)	0x00
0x58-0xFF	Reserved (Unused)	0x00

APPENDIX B: FIRMWARE REVISIONS / FEATURES REGISTER

Since DIO32A boards can exist across multiple form factors and with various hardware features, the firmware/features registers attempt to help identify the exact version of a DIO32A board. This appendix provides a more detailed breakdown of what the firmware and features registers, and detail differences between the firmware revisions.

Firmware Register - Local Offset 0x00 (0xE5110000)

D31:16 HW Board Rev 0xE511 PCIe-SIO4BX2 Rev A

- D31 **1** = Features Register Present
- D30 **1** = Complies with this standard
- D29 **1** = 66MHz PCI bus interface
  0 = 33MHz PCI bus interface
- D28 1 = 64 bit PCI bus interface
  0 = 32 bit bus interface
- D27:D24 Form Factor
  0 = Reserved
  1 = PCI
  2 = PMC
  3 = cPCI
  4 = PC104P
  5 = PCIe
  6 = XMC
- D23:D20 HW Board (sub-field of form factor)
  0 = PCIe-SIO4BX2
- D19:D16 HW Board Rev (lowest rev for firmware version)
  1 = A

D15:8 Firmware Type ID **0x00** DIO32A Firmware default

D7:0 Firmware Revision XX Firmware Version

0x00 – Initial release

Feature Register - Local Offset 0xFC (0x00197AF4)

D31:D0	Unused