PCI-DMI32

User Manual

Preliminary

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PREFACE

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Preliminary, Revised: December 1997

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This user's manual provides information on the specifications, theory of operation, register level programming, installation of the board and information required for customized hardware/software development.

RELATED PUBLICATIONS

The following manuals and specifications provide the necessary information for in depth understanding of the specialized parts used on this board.

EIA Standard for the RS-422A Interface (EIA order number EIA-RS-422A)

PCI Local Bus Specification Revision 2.1 June 1, 1995. Questions regarding the PCI specification be forwarded to:

PCI Special Interest Group
P.O. Box 14070
Portland, OR 97214
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PCI-DMI32 DOCUMENTATION HISTORY

1) 03/20/2000: Converted PCI-HPDI32A Manual to PCI-HPDI32A-PRINT
2) 05/23/2001: Document Updates

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CHAPTER 1: INTRODUCTION

2.4.2 FUNCTIONAL DESCRIPTION

The PCI-DMI32 Board provides a large on-board memory storage and high-speed, 32-bit parallel interface. It is capable of transmitting or receiving data transfers of up to 200 Mbytes per second on the cable. The PCI-DMI32 Board includes up to 2GB of DRAM, a cable input/output controller, cable transceivers (differential, LVDS), and a DMA controller. The onboard memory can be configured to be accessed either from the PCI bus, or dedicated to the cable transfer. The on-board DRAM does not provide real-time access to the data from the PCI while a transfer is in progress. The DRAM should be initialized via the PCI bus prior to the cable data transfer. When the transfer is enabled,

the cable data will be either continuously transmitted from the on-board DRAM, or continuously received into the DRAM. Once the transfer is complete, the DRAM may be again accessed from the PCI bus.

The transfer controller is designed to allow several different transfer modes. In single transfer mode, a single buffer of data is transferred across the cable and then DRAM control is returned to the PCI bus. The single buffer may start at any address offset within the full 2GB DRAM space, and the transfer buffer size is also defined. In multi-buffer mode, multiple buffers may be transferred across the cable. In this manner, the user can define multiple buffers in the DRAM, which will then be transferred continuously to the cable when the transfer is enabled. On-board interrupts are defined to allow the user to update the start buffer address and buffer transfer size as soon as the transfer of one buffer begins. In this manner, the user can dynamically receive or transmit multiple buffers to/from the DRAM in one continuous transfer.
Likewise, a single buffer can be transmitted continuously to the cable simply by not updating the start buffer address and buffer transfer size. This allows a continuous buffer of up to 2GB to be transmitted indefinitely on the cable.

Note: The PCI-DMI32 is a long card and electrically compliant with PCI 2.1. Due to the height of the DRAM modules, the card requires three PCI slots.

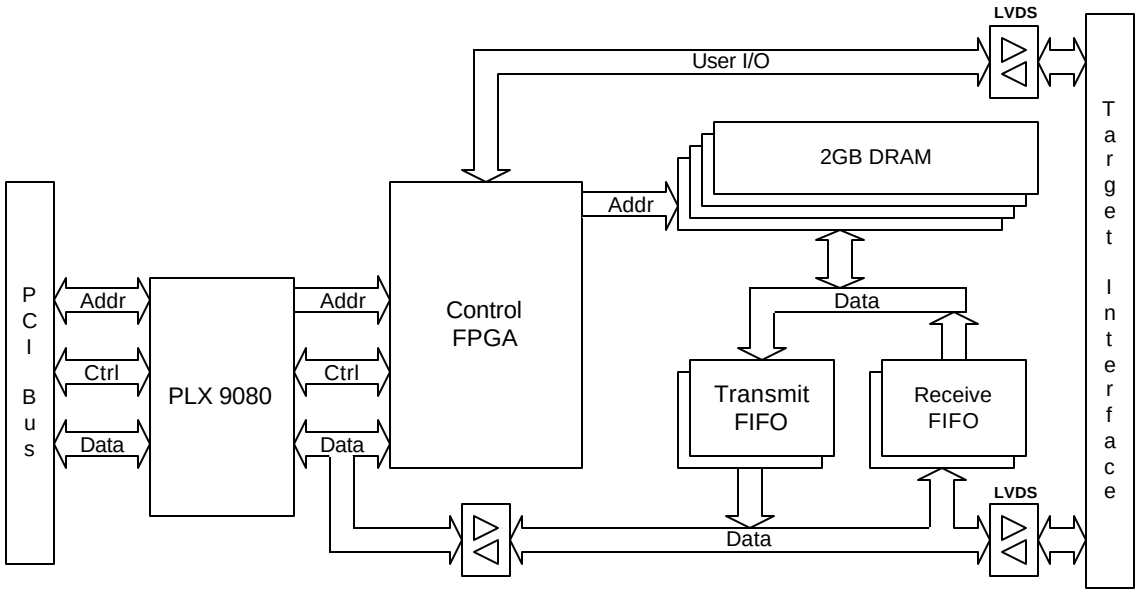


Figure 1.0-2: Functional Block Diagram

2.4.3 1.1 CABLE INTERFACE

The cable interface consists of 32 bits of data, two clocks, and 14 user definable bi-directional signals. All of which employ differential LVDS. Refer to cable pin-out Table 4.2-1.

2.4.4 1.2 DIMMS

The PCI-DIM32 board may be populated with up to four DIMMs for a total of 2 GB of memory. Currently, the PCI-DMI32 supports 512MB SDRAM modules for a total of 512MB, 1GB, 1.5GB or 2GB of memory storage. General Standards Corporation is looking into the possibility to migrate up/down using different density DIMMs. Please contact the factory for more information and availability.

2.4.5 2.0 INITIALIZATION

Several functions on the PCI-DMI32 board will generally be unchanged in a given application. These include interrupt setup and Users I/O direction setup. Therefore, initializing these functions board will generally need to be done only once by the software. However, if a Board Reset is performed, all registers will return to their default values. Software must reinitialize the board following a Board Reset. After a board reset is performed, the following will be true:

a. all cable transceivers will be turned off;
b. all interrupts will be disabled;
c. the SDRAM modules will be empty;
d. all RW registers will be set to 0 (Board Control Register bits are set to 0 on system reset)

2.4.6 RESETS

The Board Control Register contains a bit which are used to reset the local logic functions. This bit performs a reset when the software writes a '1'. The reset bit is also self-clearing, meaning software will not need to clear the bit following the reset.

Board Reset	Board Control Register D0 – Setting this bit will reset the local logic, reset (clear) the FIFOs and SDRAM modules and place all registers into a known state.

2.4.7 INTERRUPTS

The PCI-DMI32 can generate 4 interrupts in response to the following conditions.

a. Data transfer on 32 bit data I/O started. Buffer has started to transmit.
b. Data transfer on 32 bit I/O done. Buffer has finished transmitting.
c. I/O user bit 6,13 when low, indicates new data on the user I/O input register. This bit will be cleared upon reading the register.
d. PLX-DMA transfers done. Indicates the DMA has completed a transfer to or from the host memory.
All interrupts will drive the PCI INT_A interrupt line.

2.4.8 DMA

Although the 33MHz PMC/PCI bus is capable of burst transfers up to 132Mbytes per sec, actual sustained throughput on the PCI bus will be much lower. This is due to many factors such as bus overhead, operating system overhead, application overhead, and possibly data storage overhead such as hard disk drive accesses.

Since sustained PCI data rates will be typically slower than the maximum cable interface rate, DMA on the PCI bus is supported to make the PCI data transfers as fast as possible.

There are 3 methods the software application can move data to and from the PCI-DMI32 board: PIO mode, Non-Demand DMA, and Demand Mode DMA. The two DMA modes are only supported to the on-board SDRAM modules (DMA accesses to local registers are not supported).

2.4.9 PIO MODE

In PIO mode, the user accesses the memory through single register reads and writes to the board. This is the slowest data transfer mode.

2.4.10 NON-DEMAND DMA

In Non-Demand DMA mode, the user specifies a DMA transfer size and initiates the transfer.

2.4.11 DEMAND MODE DMA

Demand Mode DMA is similar to Non-Demand DMA, except the local logic will request the transfer based on FIFO status. After the user specifies a DMA transfer size and initiates the transfer, the local logic will request the data transfer if the Tx FIFO is not Full (transmit) or the Rx FIFO is not empty (Rx FIFO). For transmit, the logic will burst data into the FIFO until the Almost Full Flag is reached. The logic will then switch into a single transfer mode until the FIFO is filled (or transfer is complete). When the Tx FIFO becomes full, the logic will cease requesting data. When data is transmitted out of the FIFO (Tx FIFO no longer full), the request will again be asserted to re-fill the FIFO. This will resume until the transfer completes. When receive Demand DMA is initiated, the DMA is requested whenever data is in the Rx FIFO. On-board logic will run in burst mode until the Rx FIFO reaches the Almost Empty level, at which time the logic will switch into single word mode, where single words will be transferred until the FIFO goes empty. Once the Rx FIFO is empty, the logic ceases to request data until more data is received. The request is again asserted to empty the FIFO. This will continue until the transfer completes. Demand Mode DMA is the preferred DMA method.

2.4.12 DMA DATA PACKING

DMA also provides a means to pack 16-bit or 8-bit data into 32bit transfers. This is useful if only a 16-bit or 8-bit cable interface is used. In such cases, each data word uses the full 32-bit FIFO width (data is not packed in FIFO), but is packed for the PCI bus transfer. This will increase the effective PCI data throughput.

2.4.13 CABLE INTERFACE SIGNALS

Cable data is transferred to and from the PCI-DMI32 board via a 100-pin cable interface consisting of 50 differential signals – 1 Clock, 14 user I/O lines and 32 Data bits. The User I /O bits are divided into 2 logical blocks of 7 bits each. Each block can be configured for input or output.

Data is transferred using the Cable Clock. All transmit data and user I/O signals are clocked on the rising edge of the CLK signal. The transmit clock on the PCI-DMI32 is supplied by an on-board oscillator. This oscillator is installed in sockets so the user can customize the clock interface speed. The board is shipped with a 50MHz oscillator standard. To ensure maximum setup and hold times, all receive data and user I/O signals are clocked on the falling edge of the CLK signal. Figure 2.1 shows the data setup and hold times.

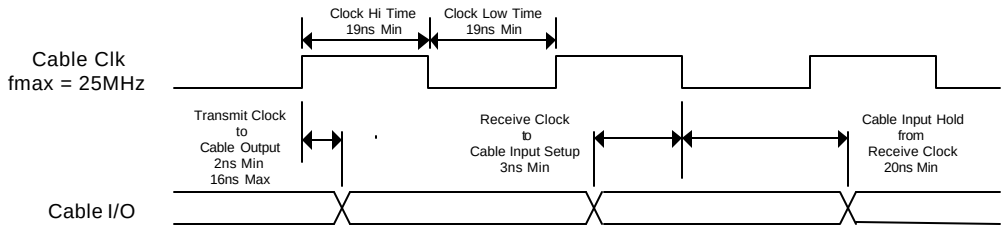


FIGURE 2.1: CABLE INTERFACE TIMING

2.4.14 USER I/O SIGNALS

The 14 user I/O lines may be used as discrete I/O. This allows users to control cable outputs, read cable inputs, or receive cable interrupts via simple software control. The user I/O bits are controlled from the Board Control register. If a bit is set as output, the Board Control register defines the output value. If a bit is setup as an input, the state of the bit may be read through the Board Status register. To set a user I/O signal as an interrupt source, set the signal as a input, and setup the interrupt source via the interrupt registers.

2.4.15 TEST MODE

Test mode (D6) in the Board Control Register is intended for Board-to-Board testing of two DMI cards. In normal mode, the DMI is connected to the SRI, and the SRI provides the transfer clock. When in test mode, a DMI card will emulate the SRI and provide the transfer clock to the second DMI card.

In test mode, the on board oscillator (50Mhz) is used as the transfer clock. The DMI card in test mode will drive the test clock on the CLKIN signal and receive

the CLKOUT signal. Control Register bit D22 may be used to switch the test clock to 25Mhz.

To simplify test mode, a jumper JP1 (J5: 7 to J5:8) has been dedicated to default the DMI card to test mode. When jumper JP1 is removed from the card the Board Control Register will reset to 0x00000050. This sets the test mode bit and sets User port A to input, and User port B to output. Therefore, the two DMI cards should each reset to the correct state for cable communication

2.4.16 DATA TRANSFERS

The DMI will transfer up to 2GB of unique data continuously at up to 50 Mhz. The data transfer may be transmitted or received, depending on the direction set in the BCR. Buffers may be transmitted or received indefinitely if the card is in multi buffer mode.

To initiate a transfer from the DMI card, the user should first initialize the on board memory, set the DRAM start address and ram transfer count. This will define the buffer to be transmitted or received. The user should then set the transfer direction and multi/single buffer mode in the BCR. (It's assumed the User I/O port directions have been previously set). Once the transfer is setup, setting the start transfer bit D7 in the BCR will initiate the transfer. At this point, the cable transceivers will be enabled. If the DMI is in normal mode, the DMI will then transmit the Start Word from the Start Word Register. Once the start word has been transmitted the DMI will began transmitting or receiving the buffer. If in single buffer mode, the buffer will be transferred and the start transfer bit will be cleared. If in multi buffer mode, the buffers will be transmitted until the software clears the start transfer bit. After the first buffer has begun to transfer, the start buffer interrupt will be asserted, and the user can update the DRAM start address and transfer count for the next buffer. If the transfer count has not been updated before the next buffer begins, the under run bit in the status register will indicate the under run condition.

2.4.17 LOCAL REGISTERS

The Local Space registers control the transmission and reception of data to and from the board

Table 3.0:

Offset Address	Size	Access*	Register Name	Value after Reset
0x00000000- x7FFFFFFF	D32	RW	Dram	N/A
0x80000000	D32	RO	Firmware Revision	0xXXXXXXXX
0x80000004	D32	RW	Board Control	0x00000000
0x80000008	D32	RO	Board Status	0xXXXXXCXX
0x8000000C	D32	RW	Dram Base Address	0x00000000
0x80000010	D32	RW	Dram Transfer Count	0x00000000
0x80000014	D32	RW	Interrupt Control	0x00000000
0x80000018	D32	RW	Interrupt Status	0x00000000
0x8000001C	D8	RW	Start Word	0x78

RO - read only
RW - read/write capability

2.4.18 PCI-DMI32 LOCAL REGISTERS, BIT MAP & BIT DESCRIPTIONS

Note: All bits labeled “Reserved” are unused in this implementation. To avoid unpredictable results a “0” should be written to these bits. The value of these “Reserved” bits is indeterminate when read.

2.4.19 FIRMWARE REVISION: (OFFSET 0X800000000)

This Register is used to determine the version of firmware that is programmed into the board. If the logic is changed to accommodate a modification for any reason then the value in this register is incremented.

Revision 104: Original version after debug and final release. (0x00000104)

2.4.20 BOARD CONTROL: (OFFSET 0X800000004)

The Board Control Register is strictly under software control and provides the following functions:

D0 Board Reset
Writing a 1 to this bit will generate a self-timed pulse that is used to reset the on-board logic.

There is no need for the software to clear this bit, the bit will always read 0.

D1 CLKIN Check
Writing a 1 to this bit will check for a clock on the CLKIN signal of the cable.
There bit will automatically clear after the SYS. The results of the clock check operation are reported in the Board Status Register.

D2 Transmit/Receive Direction
Writing a 1 to this bit will set the cable transfer direction to transmit.
Writing a 0 to this bit will set the cable transfer direction to receive.

D3 User I/O A Direction
Writing a 1 to this bit will set User I/O A port as an output port.
Writing a 0 to this bit will set User I/O A port as an input port.

D4 User I/O B Direction
Writing a 1 to this bit will set User I/O B port as an output port.
Writing a 0 to this bit will set User I/O B port as an input port.

Note: User I/O B port must be set to the opposite direction of the User I/O A port. If both ports are set the same, only User I/O A will be enabled.

D5 Multi Buffer Mode
Writing a 1 to this bit will set the cable transfer to multi buffer mode. During transfers, new buffers will continuously be loaded as the previous buffer completes.
Writing a 0 to this bit will set the cable transfer to single buffer mode. During the transfer a single buffer will be transmitted and the transfer will automatically stop.

D6 Test Mode
Note: Test mode is intended for loop back testing between two DMI Cards.
Writing a 1 to this bit will enable DMI test mode. When in test mode, the DMI card will generate the clock to the CLKIN Signal and receive the clock from the CLKOUT signal (opposite of normal DMI mode). The clock will be generated from an on-board 50Mhz oscillator.
Writing a 0 to this bit will set the DMI in normal mode. This bit should be cleared if the DMI is connected to the SRI or when connected to another DMI in test mode.

D7 Start Transfer
Writing a 1 to this bit will start data transferring on the cable. All other bits associated with the data transfer should be set before (or at the same time) as the start transfer bit. In Single Buffer Mode, this bit will clear automatically at the end of a transfer.
Writing a 0 to this bit will immediately terminate a transfer in progress, both multi buffer mode and single mode.

D8..14 User I/O A Output

If user I/O A port is setup as output, these bits will be transmitted to the cable. These bits will be output directly to the cable regardless of the start transfer mode bit. Bit D14 is defined as the valid bit for the output word.

D15..21 User I/O B Output
If user I/O B port is setup as output, these bits will be transmitted to the cable. These bits will be output directly to the cable regardless of the start transfer mode bit. Bit D21 is defined as the valid bit for the output word.

D22 Internal Clock Speed
While in test mode (D5=1), this bit determines whether the transfer clock is 50Mhz or 25Mhz. Writing a 0 to this bit will set the internal test clock to 50Mhz, while a 1 will set the internal test clock to 25Mhz.

D23..31 Reserved

2.4.21 BOARD STATUS: (OFFSET 0X800000008)

The Board Status Register is used to return information to the software about the most current status of the board, at the time of the reading. Listed below is the information that this register contains:

D0 CLKIN Present
A 1 indicates the CLKIN signal was detected during the CLKIN test (D1 of Board Control Register). A 0 indicates no CLKIN present

D1 CLKIN Valid
A 1 indicates the “CLKIN present” (D0) bit is valid. A 0 indicates the CLKIN check test is in progress.

D2..3 Reserved

D4 JP0
A 1 indicates the jumper JP0 has been removed.

D5 JP1
A 1 indicates the jumper JP1 has been removed.

D6..7 Reserved

D8..14 User I/O A Input
If User I/O A direction is set to input, these bits will show the last valid command received. If User I/O A is set to output, these bits will show the current state of the output port.
If User I/O A set to input, Bit D14 will indicate a new command has been received. (a low-to-hi transition on User I/o bit 6). After the Board Status Register has been read, this bit will clear until the next valid command is received.

D21..15 User I/O B Input
If User I/O B direction is set to input, these bits will show the last valid command received. If User I/O B is set to output, these bits will show the current state of the output port.
If User I/O B set to input, Bit D14 will indicate a new command has been received. (a low-to-hi transition on User I/o bit 6). After the Board Status Register has been read, this bit will clear until the next valid command is received.

D31..22 CLKIN Frequency Counter
Following a CLKIN test (D1 of the Board Control Register), this field contains the number of CLKIN clocks during a 5us period. Using this count the CLKIN frequency MHz can be determined using the following formula: **Freq(MHz)=Count/5**

2.4.22 DRAM BASE ADDRESS: (OFFSET 0X80000000C)
Starting Address of buffer for data transfer.

DRAMM TRANSFER COUNT: (Offset 0x800000010)

Number of bytes in buffer for data transfer.

Note: The DRAM BASE ADDRESS and DRAM TRANSFER COUNT must not exceed the total memory size.

2.4.23 INTERRUPT CONTROL: (OFFSET 0X800000014)

D0	Enable Buffer Start Interrupt
D1	Enable Buffer End Interrupt
D2	Enable User I/O A Input Interrupt
D3	Enable User I/O B Input Interrupt
D4..31	Reserved

2.4.24 INTERRUPT STATUS: (OFFSET 0X800000018)

The Interrupt Status Register serves as a dual-purpose register. Each bit in this register operates independently of each other. If an interrupt condition is enabled in the Interrupt Control Register, the appropriate bit in the Interrupt Status Register will indicate if an interrupt has occurred or not. When an interrupt occurs the status bit will latch the interrupt condition until software resets it by writing a "1" to the appropriate bit. If an interrupt is not enabled in the Interrupt Control Register, then the appropriate bit in the Interrupt Status Register will indicate whether or not the condition currently exists for an interrupt request. In this case, the interrupt condition is not latched and does not need to be cleared by software.

D0 Enable Buffer Start Interrupt
D1 Enable Buffer End Interrupt
D2 Enable User I/O A Input Interrupt
D3 Enable User I/O B Input Interrupt
D4 Under run status
This bit will be set in multibuffer mode when a new buffer was started before the DRAM Transfer count register was reloaded.

D5..31 Reserved

2.4.25 START WORD: (OFFSET 0X80000001C)

D0..6 This register contains the start command word to be transmitted when a data transfer is initiated. This register defaults to 0x78 at reset, but may be changed by the user if necessary.

D31..7 Reserved

2.4.26 4.0 PCI INTERFACE REGISTERS

A PCI9080 I/O Accelerator from PLX Technology handles the PCI Interface. The PCI interface is compliant with the 5V, 33MHz PCI Specification 2.1. The PCI9080 provides dual DMA controllers for fast data transfers to and from the on-board FIFOs. Fast DMA burst accesses provide for a maximum burst throughput of 132MB/s to the PCI interface. To reduce CPU overhead during DMA transfers, the controller also implements Chained (Scatter/Gather) DMA, as well as Demand Mode DMA.

Since many features of the PCI9080 are not utilized in this design, it is beyond the scope of this document to duplicate the PCI9080 User's Manual. Only those features, which will clarify areas specific to the PCI/PMC-HPDI32, are detailed here. Please refer to the PCI9080 User's Manual (See Related Publications) for more detailed information. Note that the BIOS configuration and software driver will handle most of the PCI9080 interface. Unless the user is writing a device driver, the details of the PCI interface (Chapter 2) may be skipped.

2.4.27 4.1 PCI CONFIGURATION REGISTERS

The PCI device configuration for the PCI-DMI32 is fully PCI 2.1 compliant. Table 4.1 contains a list of the PCI configuration registers present in the PCI9080. An on-board configuration serial EEPROM initializes many of these registers.

Table 4.1: PCI Configuration Registers

PCI CFG Addr	Local Offset Addr	PCI/Local Writable	Register Name	Value after Reset
0x00	0x00	Local	Device ID/Vendor ID	0x908010B5
0x04	0x04	Y	Status/Command	0x02800017
0x08	0x08	Local	Class Code/Revision ID	0x0680003
0x0C	0x0C	Y[15:0], Local	BIST (Unused)/Header Type/Latency Timer/Cache Line Size	0x00002008
0x10	0x10	Y	PCI Base Addr 0 for Memory Mapped Local/Runtime/DMA Registers (PCIBAR0)	0x00000000
0x14	0x14	Y	PCI Base Addr 1 for I/O Mapped Local/Runtime/DMA Registers (PCIBAR1)	0x00000001
0x18	0x18	Y	PCI Base Addr 2 for Local Addr Space 0 (PCIBAR2)	0x00000000
0x1C	0x1C	Y	PCI Base Addr 3 for Local Addr Space 1 (PCIBAR3) (Unused)	0x00000000

0x2C	0x2C	Local	Subsystem ID/Subsystem Vendor ID	0x90802400
0x30	0x30	Y	PCI Base Address to Local Expansion ROM (Unused)	0x00000000
0x3C	0x3C	Y[7:0], Local	Max_Lat/Min_Gnt/Interrupt Pin/Interrupt Line	0x00000100

Note: The Local Base Address for the PCI Configuration registers in Local Address Space is 0xC0000000. However, there should be no need for the user to access the PCI Configuration registers through Local Address Space.

2.4.28 PCI CONFIGURATION ID REGISTER
(Offset 0x00, Reset 0x908010B5)

D15:0 Vendor ID –– 0x10B5 = PLX Technology
D31:16 Device ID –– 0x9080 = PCI9080

2.4.29 PCI COMMAND REGISTER
(Offset 0x04, Reset 0x0017)

D0 I/O Space
A '1' allows the device to respond to I/O space accesses.

D1 Memory Space
A '1' allows the device to respond to memory space accesses.

D2 PCI Master Enable.
A '1' allows the device to behave as a PCI bus master.
Note: *This bit must be set for the PCI 9080 to perform DMA cycles.*

D3 Special Cycle. (*Not Supported.*)

D4 Memory Write/Invalidate.
A '1' enables memory write/invalidate.

D5 VGA Palette Snoop. (*Not Supported.*)

D6 Parity Error Response
A '0' indicates that a parity error is ignored and operation continues.
A '1' indicates that parity checking is enabled.

D7 Wait Cycle Control. Controls whether the device does address/data stepping.
A '0' indicates the device never does address/data stepping.
Note: *Hardcoded to 0.*

D8 SERR# Enable
A '1' allows the device to drive the SERR# line.

D9 Fast Back-to-Back Enable. Indicates what type of fast back-to-back transfers a Master can perform on the bus.
A '1' indicates fast back-to-back transfers can occur to any agent on the bus.

A '0' indicates fast back-to-back transfers can only occur to the same agent as the previous cycle.

D15:10 Reserved

2.4.30 4.1.3 PCI STATUS REGISTER
(Offset 0x06, Reset 0x0280)

D5:0 Reserved

D6 User Definable Features Supported
A '1' indicates UDF are supported.
Note: *User Definable Features are Not Implemented*

D7 Fast Back-to-Back Capable.
A '1' indicates the adapter can accept fast back-to-back transactions.

D8 Master Data Parity Error Detected
A '1 indicates the following three conditions are met:
1. PCI9080 asserted PERR# itself or observed PERR# asserted.
2. PCI9080 was bus master for the operation in which the error occurred.
3. Parity Error Response bit in the Command Register is set.
Writing a '1' to this bit clears the bit.

D10:9 DEVSEL Timing. Indicates timing for DEVSEL# assertion.
A value of '01' indicates a medium decode.
Note: *Hardcode to 01.*

D11 Target Abort
A '1' indicates the PCI9080 has signaled a target abort.
Writing a '1' to this bit clears the bit.

D12 Received Target Abort
A '1' indicates the PCI9080 has received a target abort.
Writing a '1' to this bit clears the bit.

D13 Master Abort
A '1' indicates the PCI9080 has generated a master abort signal.
Writing a '1' to this bit clears the bit.

D14 Signal System Error
A '1' indicates the PCI9080 has reported a system error on the SERR# signal.
Writing a '1' to this bit clears the bit.

D15 Detected Parity Error
A '1' indicates the PCI9080 has detected a PCI bus parity error, even if parity error handling is disabled (the Parity Error Response bit in the Command Register is clear).
One of three conditions can cause this bit to be set:
1. PCI9080 detected a parity error during a PCI address phase.
2. PCI9080 detected a data parity error when it was the target of a write.

3. PCI9080 detected a data parity error when performing a master read.

Writing a '1' to this bit clears the bit.

2.4.31 4.1.4 PCI REVISION ID REGISTER
(Offset 0x08)

D7:0 Revision ID - The silicon revision of the PCI9080.

2.4.32 PCI CLASS CODE REGISTER
(Offset 0x09-0B, Reset=0x068000)

D7:0 Register level programming interface
0x00 = Queue Ports at 0x40 and 0x44.
0x01 = Queue Ports at 0x40 and 0x44, Int Status and Int Mask at 0x30 and 0x34
D15:8 Sub-class Code - 0x80 = Other bridge device.
D23:16 Base Class Code. - 0x06 = Bridge Device

2.4.33 PCI CACHE LINE SIZE REGISTER
(Offset 0x0C, Reset 0x00)

D7:0 System cache line size in units of 32-bit words.

2.4.34 PCI LATENCY TIMER REGISTER
(Offset 0x0D, Reset 0x00)

D7:0 PCI Latency Timer. Units of PCI bus clocks, the amount of time the PCI9080, as a bus master, can burst data on the PCI bus.

2.4.35 PCI HEADER TYPE REGISTER
(Offset 0x0E, Reset 0x00)

D6:0 Configuration Layout Type = 0
D7 Header Type = 0.

2.4.36 PCI BASE ADDRESS REGISTER FOR MEMORY ACCESS TO LOCAL/RUNTIME/DMA REGISTERS
(Offset 0x010, Reset 0x00000000)

D0 Memory Space Indicator
A '0' indicates register maps into Memory space.
Note: *Hardcoded to 0.*
D2:1 Location of Register:
00 - Locate anywhere in 32-bit memory address space

Note: *Hardcoded to 0.*

D3 Prefetchable.
Note: *Hardcoded to 0.*

D7:4 Memory Base Address.
Default Size = 256 bytes.
Note: *Hardcoded to 0.*

D31:8 Memory Base Address.
Memory base address for access to Local, Runtime, and DMA registers.

Note: *PCIBAR0 is Memory Mapped Base Address of PCI9080 Registers*

2.4.37 PCI BASE ADDRESS REGISTER FOR I/O ACCESS TO LOCAL/RUNTIME/DMA REGISTERS
(Offset 0x14, Reset 0x00000001)

D0 Memory Space Indicator
A '1' indicates the register maps into I/O space.
Note: *Hardcoded to 1.*

D1 Reserved

D7:2 I/O Base Address.
Default Size = 256 bytes.
Note: *Hardcoded to 0.*

D31:8 I/O Base Address.
Base Address for I/O access to Local, Runtime, and DMA Registers.

Note: *PCIBAR1 is I/O Mapped Base Address of PCI9080 Registers*

2.4.38 4.1.11 PCI BASE ADDRESS REGISTER FOR MEMORY ACCESS TO LOCAL ADDRESS SPACE 0
(Offset 0x18, Reset 0x00000000)

D0 Memory Space Indicator
A '0' indicates register maps into Memory space.
(Specified in Local Address Space 0 Range Register - LAS0RR.)

D2:1 Location of register (if memory space). Location values:
00 - Locate anywhere in 32-bit memory address space
(Specified in Local Address Space 0 Range Register - LAS0RR.)

D3 Prefetchable
A '0' indicates reads are not prefetchable.
(Specified in Local Address Space 0 Range Register - LAS0RR

D31:4 Memory Base Address
Memory base address for access to Local Address Space 0.

2.4.39 PCI SUBSYSTEM DEVICE/VENDOR ID REGISTER
(Offset 0x2C, Reset 0x908010B5)

D15:0 Subsystem Vendor ID – 0x10B5 = PLX Technology

D31:16 Subsystem Device ID – 0x2400 = General Standards Corporation HPDI32).

2.4.40 PCI INTERRUPT LINE REGISTER
(Offset 0x3C, Reset 0x00)

D7:0 Interrupt Line Routing Value.
Indicates which input of the system interrupt controller(s) to which the interrupt line of the device is connected.

2.4.41 PCI INTERRUPT PIN REGISTER
(Offset 0x3D, Reset 0x01)

D7:0 Interrupt Pin register. Indicates which interrupt pin the device uses.

01=INTA#

Note: *PCI 9080 supports only one PCI interrupt pin (INTA#).*

2.4.42 PCI MIN_GNT REGISTER
(Offset 0x3E, Reset 0x00)

D7:0 Minimum Grant
Specifies the minimum burst period the device needs assuming a clock rate of 33 MHz. Value is in 250 nsec increments. A '0' indicates no stringent requirement.

2.4.43 PCI MAX_LAT REGISTER
(Offset 0x3F, Reset 0x00)

D7:0 Maximum Latency
Specifies the maximum burst period the device needs assuming a clock rate of 33 MHz. Value is in 250 nsec increments. A '0' indicates no stringent requirement.

2.4.44 LOCAL CONFIGURATION REGISTERS

The Local Configuration registers give information on the Local side implementation. Since Local Expansion ROM, Local Address Space 1, and Direct Master accesses are not implemented on the PCI/PMC-HPDI32, the descriptions of these registers have been omitted. Most of the Local Configuration Registers are preloaded from the configuration Serial EEPROM at system reset.

Table 4.2: Local Configuration Registers

PCI CFG Addr	Local Offset Addr	PCI/Local Writable	Register Name	Value after Reset
0x00	0x80	Y	Range for PCI to Local Address Space 0	0xFFFFF000
0x04	0x84	Y	Local Base Address (Remap) for PCI to Local Address Space 0 (Unused)	0x00000000
0x08	0x88	Y	Mode/Arbitration Register	0x00000000
0x0C	0x8C	Y	Big/Little Endian Descriptor	0x00000000
0x10	0x90	Y	Range for PCI to Local Expansion ROM (Unused)	0x00000000
0x14	0x94	Y	Local Base Address (Re-map) for PCI to Local Expansion ROM and BREQo control (Unused)	0x00000000
0x18	0x98	Y	Local Bus Region Descriptions for PCI Local Accesses	0x00000000
0x1C	0x9C	Y	Range for Direct Master to PCI (Unused)	0x00000000
0x20	0xA0	Y	Local Base Address for Direct Master to PCI Memory (Unused)	0x00000000
0x24	0xA4	Y	Local Base Address for Direct Master to PCI Memory IO/CFG (Unused)	0x00000000
0x28	0xA8	Y	PCI Base Address (Re-map) for Direct Master to PCI (Unused)	0x00000000
0x2C	0xAC	Y	PCI Configuration Address Register for Direct Master to PCI IO/CFG (Unused)	0x00000000
0xF0	0x170	Y	Range for PCI to Local Address Space 1 (Unused)	0x00000000
0xF4	0x174	Y	Local Base Address (Remap) for PCI to Local Address Space 1 (Unused)	0x00000000
0xF8	0x178	Y	Local Bus Region Descriptor (Space 1) for PCI to Local Accesses (Unused)	0x00000000

2.4.45 LOCAL ADDRESS SPACE 0 RANGE REGISTER FOR PCI TO LOCAL BUS (PCI 0x00, Reset 0xFFFFF000)

D0 Memory Space Indicator
A '0' indicates register maps into Memory space.

D2:1 Location of register (if memory space). Location values:
00 - Locate anywhere in 32-bit memory address space

D3 Prefetchable
A '0' indicates reads are not prefetchable.

D31:4 Specifies which PCI address bits will be used to decode a PCI access to Local Address Space 0. A '1' indicates bit is included in address decode.

Local Address Space 0 value 0xFFFFF000 maps a 4kbyte range.

Since entire Local Address Space can be mapped into 4kb range, the remap register is not used.

2.4.46 MODE/ARBITRATION REGISTER
(PCI 0x08)

D7:0 Local bus Latency Timer (Unused)

D8:15 Local bus Pause Timer (Unused)

D16 Local bus Latency Timer Enable (Unused)

D17 Local bus Pause Timer Enable (Unused)

D18 Local bus BREQ Enable (Unused)

D20:19 DMA Channel Priority
00 = Rotational priority
01 = Channel 2 priority
10 = Channel 1 priority
11 = Reserved

D21 Local bus direct slave give up bus mode
A value of 1 indicates local bus will be released when PCI9080 write FIFO empty or read FIFO full.

D22 Direct slave LLOCKo# Enable (Unused)

D23 PCI Request Mode

D24 PCI Rev 2.1 Mode

D25 PCI Read No Write Mode

D26 PCI Read with Write Flush Mode

D27 Gate the Local Bus Latency Timer with BREQ (Unused)

D28 PCI Read No Flush Mode

D29 Reads Device/Vendor ID or SubDevice/SubVendor ID

D31:30 Reserved

2.4.47 BIG/LITTLE ENDIAN DESCRIPTOR REGISTER
(PCI 0x0C)

Since local bus is little endian, all bits should be left zero

2.4.48 LOCAL ADDRESS SPACE 0/EXPANSION ROM BUS REGION DESCRIPTOR REGISTER
(PCI 0x18, Reset 0x40030143)

D1:0 Memory Space 0 Local Bus Width
11 indicates 32-bit local bus
D5:2 Memory Space 0 Internal Wait States
A '0' indicates no wait states required
D6 Memory Space 0 Ready Input Enable
A '1' indicates Local Ready input enabled.
D7 Memory Space 0 Bterm Input Enable (Unused)
D8 Memory Space 0 Prefetch Disable (Unused)
D9 Expansion ROM Space Prefetch Disable (Unused)
D10 Read Prefetch Count Enable (Unused)
D14:11 Prefetch Counter (Unused)
D15 Reserved
D17:16 Expansion ROM Space Local Bus Width (Unused)
D21:18 Expansion ROM Space Internal Wait States (Unused)
D22 Expansion ROM Space Ready Input Enable (Unused)
D23 Expansion ROM Space Bterm Input Enable (Unused)
D24 Memory Space 0 Burst Enable
D25 Extra Long Load from Serial Enable
D26 Expansion ROM Space Burst Enable (Unused)
D27 Direct Slave PCI Write Mode
D28:31 PCI Target Retry Delay Clocks

2.4.49 4.3 RUNTIME REGISTERS

The Runtime registers consist of mailbox registers, doorbell registers, and a general-purpose control register. The mailbox and doorbell registers serve no purpose on the PCI/PMC-HPDI32.

Table 4.3: Runtime Registers

PCI CFG Addr	Local Offset Addr	PCI/Local Writable	Register Name	Value after Reset
0x40	0xC0	Y	Mailbox Register 0 (Unused)	0x00000000
0x44	0xC4	Y	Mailbox Register 1 (Unused)	0x00000000
0x48	0xC8	Y	Mailbox Register 2 (Unused)	0x00000000
0x4C	0xCC	Y	Mailbox Register 3 (Unused)	0x00000000
0x50	0xD0	Y	Mailbox Register 4 (Unused)	0x00000000
0x54	0xD4	Y	Mailbox Register 5 (Unused)	0x00000000
0x58	0xD8	Y	Mailbox Register 6 (Unused)	0x00000000
0x5C	0xDC	Y	Mailbox Register 7 (Unused)	0x00000000
0x60	0xE0	Y	PCI to Local Doorbell Register (Unused)	0x00000000
0x64	0xE4	Y	Local to PCI Doorbell Register (Unused)	0x00000000
0x68	0xE8	Y	Interrupt Control/Status	0x00000000

0x6C	0xEC	Y	General Purpose Control	0x00000000
0x70	0xF0	N	Permanent Device ID/ Permanent Vendor ID	0x10B59080
0x74	0xF4	N	Permanent Revision ID	0x0000000X
0x78	0xC0	Y	Mailbox Register 0 (Unused)	0x00000000
0x7C	0xC4	Y	Mailbox Register 1 (Unused)	0x00000000

2.4.50 INTERRUPT CONTROL /STATUS
(PCI 0x68, Reset 0x00000000)

D0 Enable Local bus LSERR# (Unused)
D1 Enable Local bus LSERR# on a PCI parity error (Unused)
D2 Generate PCI Bus SERR#
D3 Mailbox Interrupt Enable (Unused)
D7:4 Reserved
D8 PCI Interrupt Enable
D9 PCI Doorbell Interrupt Enable (Unused)
D10 PCI Abort Interrupt Enable
D11 PCI Local Interrupt Enable
Local Interrupt must be enabled for USC/FIFO interrupts.
D12 Retry Abort Enable (Unused)
D13 PCI Doorbell Interrupt Status.
D14 PCI Abort Interrupt Status
D15 PCI Local Interrupt Status
D16 Local Interrupt Output Enable
D17 Local Doorbell Interrupt Enable (Unused)
D18 Local DMA Channel 0 Interrupt Enable
D19 Local DMA Channel 1 Interrupt Enable
D20 Local Doorbell Interrupt Status
D21 DMA Channel 0 Interrupt Status
D22 DMA Channel 1 Interrupt Status
D23 BIST Interrupt Status
D24 A '0' indicates a Direct Master was bus master during a Master or Target abort.
D25 A '0' indicates that DMA CH0 was bus master during a Master or Target abort.
D26 A '0' indicates that DMA CH1 was bus master during a Master or Target abort.
D27 A '0' indicates that a Target Abort was generated by the PCI9080 after 256 consecutive Master retries to a Target.
D31:28 PCI Mailbox 3:0 Write Status

2.4.51 SERIAL EEPROM CONTROL, PCI COMMAND CODES, USER I/O CONTROL, INIT CONTROL REGISTER
(PCI 0x6C, Reset 0x0x001767E)

D3:0 PCI Read Command Code for DMA
D7:4 PCI Write Command Code for DMA
D11:8 PCI Memory Read Command Code for Direct Master (Unused)
D15:12 PCI Memory Write Command Code for Direct Master (Unused)
D16 General Purpose Output (Unused)
D17 General Purpose Input (Unused)
D23:18 Reserved
D24 Serial EEPROM clock for Local or PCI bus reads or writes to Serial EEPROM.
D25 Serial EEPROM chip select
D26 Write bit to serial EEPROM
D27 Read serial EEPROM data bit
D28 Serial EEPROM present
D29 Reload Configuration Registers
D30 PCI Adapter Software Reset
D31 Local Init Status
A '1' indicates Local initialization done.

2.4.52 PCI PERMANENT CONFIGURATION ID REGISTER (PCI 0x70, Reset 0x10B59080)

D15:0 Permanent Vendor ID (0x10B5)
D31:16 Permanent Device ID (0x9080)

2.4.53 PCI PERMANENT REVISION ID REGISTER (PCI 0x74)

D7:0 Permanent Revision ID

2.4.54 4.4 LOCAL DMA REGISTERS

The Local DMA registers are used to setup the DMA transfers to and from the on-board FIFOs. Since the PCI/PMC-HPDI32 is half-duplex (data is only transferred in one direction at a time), only DMA Channel 0 is used.

Table 4.4: DMA Registers

PCI CFG Addr	Local Offset Addr	PCI/Local Writable	Register Name	Value after Reset
0x80	0x100	Y	DMA Channel 0 Mode Register	0x00000003
0x84	0x104	Y	DMA Channel 0 PCI Address Register	0x00000000
0x88	0x108	Y	DMA Channel 0 Local Address Register	0x00000000
0x8C	0x10C	Y	DMA Channel 0 Transfer Byte Count Register	0x00000000
0x90	0x110	Y	DMA Channel 0 Descriptor Pointer Register	0x00000000
0x94	0x114	Y	DMA Channel 1 Mode Register (Unused)	0x00000003
0x98	0x118	Y	DMA Channel 1 PCI Address Register (Unused)	0x00000000
0x9C	0x11C	Y	DMA Channel 1 Local Address Register (Unused)	0x00000000
0xA0	0x120	Y	DMA Channel 1 Transfer Byte Count Register (Unused)	0x00000000
0xA4	0x124	Y	DMA Channel 1 Descriptor Pointer Register (Unused)	0x00000000
0xA8	0x128	Y	DMA Channel 1Command/Status Register DMA Channel 0 Command/Status Register	0x00000010
0xAC	0x12C	Y	DMA Mode/ Arbitration Register	0x00000000
0xB0	0x130	Y	DMA Threshold Register	0x00000000

2.4.55 DMA CHANNEL 0 MODE REGISTER (PCI 0x80)

D1:0 Local Bus Width
00 = 8 bit DMA transfer width
01 = 16 bit DMA transfer width
10/11 = 32 bit DMA transfer width

D5:2 Internal Wait States (Unused)

D6 Ready Input Enable
Note: This bit should always be set to '1' (Ready Input Enabled)

D7 Bterm# Input Enable (Unused)
Note: This bit should always be set to '0' (BTERM# Disabled)

D8 Local Burst Enable
Note: If Burst enabled, the user must ensure FIFO will not become empty (read) or full (write) during the burst access. For Demand Mode DMA, this means the Almost Empty/Almost Full flags should be set to a value of at least 8.

D9 Chaining Enable
A '1' indicates chaining mode is enabled.

For chaining mode, the DMA source address, destination address and byte count are loaded from memory in PCI Space.

D10 Done Interrupt Enable
A '1' enables interrupt when DMA done.
Note: If DMA clear count mode is enabled, the interrupt won't occur until the byte count is cleared.

D11 Local Addressing Mode
A '1' indicates local addresses LA [31:2] to be held constant.
Note: This bit should always be set to '1' (no address increment)

D12 Demand Mode Enable
A '1' causes the DMA controller to operate in Demand Mode.
In Demand Mode, the DMA controller transfers data when its DREQ# input is asserted. The DMA controller transfers Lwords (32bits) of data. This may result in multiple transfers for an 8 or 16 bit bus.

D13 Write and Invalidate Mode for DMA Transfers
When set to 1, PCI 9080 performs Write and Invalidate cycles to the PCI bus. PCI 9080 supports Write and Invalidate sizes of 8 or 16 Lwords. The size is specified in the PCI Cache Line Size Register. If a size other than 8 or 16 is specified, PCI 9080 performs write transfers rather than Write and Invalidate transfers. Transfers must start and end at the Cache Line Boundaries.

D14 DMA EOT (End of Transfer) Enable (Unused)

D15 DMA Stop Data Transfer Mode
A'0' sends a BLAST to terminate DMA transfer
Note: This bit should always be set to '0'.

D16 DMA Clear Count Mode (Unused)

D17 DMA Channel 0 Interrupt Select
A '1' routes the DMA Channel 0 interrupt to the PCI interrupt.
Note: This bit should always be set to '1'.

D31:18 Reserved

2.4.56 DMA CHANNEL 0 PCI ADDRESS REGISTER (PCI 0x84)

D31:0 PCI Address Register

2.4.57 DMA CHANNEL 0 LOCAL ADDRESS REGISTER (PCI 0x88)

D31:0 Local Address Register
Note: Should be set to Local FIFO offset 0x18

2.4.58 DMA CHANNEL 0 TRANSFER SIZE (BYTES) REGISTER (PCI 0x8C)

D22:0 DMA Transfer Size
D31:23 Reserved

2.4.59 DMA CHANNEL 0 DESCRIPTOR POINTER REGISTER (PCI 0x90)

D0 Descriptor Location
A '1' indicates PCI address space.
Note: This bit should always be set to '1' if Chained DMA enabled.
D1 End of Chain
D2 Interrupt after Terminal Count
D3 Direction of transfer
A '1' indicates transfers from local bus to PCI bus (Read Receive FIFO)
A '0' indicates transfers from local bus to PCI bus (Write Transmit FIFO)
D31:4 Next Descriptor Address

2.4.60 DMA CHANNEL 0 COMMAND/STATUS REGISTER (PCI 0xA8)

D0 Channel 0 Enable
D1 Channel 0 Control
D2 Channel 0 Abort
D3 Clear Interrupt
D4 Channel 0 Done
D7:5 Reserved

2.4.61 DMA ARBITRATION REGISTER (PCI 0xAC)

Same as Mode /Arbitration Register (MARBR) (PCI 0x08 – See Section 2.2.2)

2.4.62 DMA THRESHOLD REGISTER (PCI 0xB0)

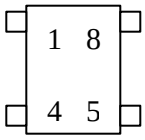
D3:0 DMA Channel 0 PCI to Local Almost Full (C0PLAF)
D7:4 DMA Channel 0 Local to PCI Almost Empty (C0LPAE)
D11:8 DMA Channel 0 Local to PCI Almost Full (C0LPAF)
D15:12 DMA Channel 0 PCI to Local Almost Empty (C0PLAE)
D19:16 DMA Channel 1 PCI to Local Almost Full (C1PLAF) (Unused)
D23:20 DMA Channel 1 Local to PCI Almost Empty (C1LPAE) (Unused)
D27:24 DMA Channel 1 PCI to Local Almost Full (C1LPAF) (Unused)
D31:28 DMA Channel 1 PCI to Local Almost Empty (C1PLAE) (Unused)

2.4.63 4.5 MESSAGING QUEUE REGISTERS

Messaging queue registers are not used on the PCI -DMI32.

2.4.64 THE ON-BOARD TRANSMIT CLOCK

The on-board oscillator, U11, is used as the transmit clock while in test mode. The oscillator is factory installed at 50MHz. This oscillator can be changed in the field by the end user. The maximum frequency supported by this clock is 50Mhz.



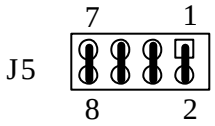
Pin	Name
1	NC
4	GND
5	OUT
8	VDD

8 pin oscillator pin-out

Figure 4.0-1: Oscillator specification

JUMPERS (J5)

J5 is a header consisting of four individual jumpers.



J5: 1 to J5: 2 EEPROM Configuration

This jumper connects the PNP EEPROM to the PCI chipset for power-up configuration. This jumper is intended for factory use only and should always be installed.

J5: 3 to J5: 4 FPGA Reload

This jumper connects the FPGA Reload to the local PCI. When this jumper is installed, the FPGA will reload when the PCI is reset. If the jumper is off, the FPGA will reload only at power-up. This jumper is intended for factory use only and should always be installed.

J5: 5 to J5: 6 JP0

This jumper is a general-purpose jumper, which may be read from the Board Status Register (D?). If two identical DMI cards are present in one system, this jumper may be removed on one card to provide a means to distinguish the cards via software.

J5: 7 to J5: 8 JP1(Test Mode Jumper)

When this jumper is removed, the card will reset to Test mode if D6 is set in the Board Control Register. The User I/O ports will also default to port A as input and port B as output. This bit may be read from D4 & 5 of the Board Status Register.

4.2 CABLE CONNECTOR

The 80-pin user connector (reference designator: P1) is manufactured by Robinson Nugent, the part number is P50E-080-P1-SR1-TG. The part number for the mate is P50E-080-S-TG, (50 mil. cabling is suggested for twisted pair), or P25E-080S-TG (25 mil. cabling may be used for multi-drop capability, but with loss of twisted pair).

Table 4.2-1: Cable Pin-Out:

Pin No.	Cable Signal Name	Pin No.	Cable Signal Name
1A	CLK IN +(CLK FROM SRI)	1B	CLK IN -(CLK FROM SRI)
2A	USER D0 +	2B	USER D0 -
3A	USER D1 +	3B	USER D1 -
4A	USER D2 +	4B	USER D2 -
5A	USER D3 +	5B	USER D3 -
6A	USER D4 +	6B	USER D4 -
7A	USER D5 +	7B	USER D5 -
8A	USER D6 +	8B	USER D6 -
9A	USER D7 +	9B	USER D7 -
10A	USER D8 +	10B	USER D8 -
11A	USER D9 +	11B	USER D9 -
12A	USER D10 +	12B	USER D10 -
13A	USER D11 +	13B	USER D11 -
14A	USER D12 +	14B	USER D12 -
15A	USER D13 +	15B	USER D13 -
16A	CLOCK OUT +(CLK TO SRI)	16B	CLOCK OUT -(CLK TO SRI)
17A	I/O D0 +	17B	I/O D0 -
18A	I/O D1 +	18B	I/O D1 -
19A	I/O D2 +	19B	I/O D2 -
20A	I/O D3 +	20B	I/O D3 -
21A	I/O D4 +	21B	I/O D4 -
22A	I/O D5 +	22B	I/O D5 -
23A	I/O D6 +	23B	I/O D6 -
24A	I/O D7 +	24B	I/O D7 -
25A	I/O D8 +	25B	I/O D8 -
26A	I/O D9 +	26B	I/O D9 -
27A	I/O D10 +	27B	I/O D10 -
28A	I/O D11 +	28B	I/O D11 -
29A	I/O D12 +	29B	I/O D12 -
30A	I/O D13 +	30B	I/O D13 -
31A	I/O D14 +	31B	I/O D14 -
32A	I/O D15 +	32B	I/O D15 -
33A	I/O D16 +	33B	I/O D16 -
34A	I/O D17 +	34B	I/O D17 -
35A	I/O D18 +	35B	I/O D18 -
36A	I/O D19 +	36B	I/O D19 -
37A	I/O D20 +	37B	I/O D20 -
38A	I/O D21 +	38B	I/O D21 -
39A	I/O D22 +	39B	I/O D22 -
40A	I/O D23 +	40B	I/O D23 -
41A	I/O D24 +	41B	I/O D24 -
42A	I/O D25 +	42B	I/O D25 -
43A	I/O D26 +	43B	I/O D26 -
44A	I/O D27 +	44B	I/O D27 -
45A	I/O D28 +	45B	I/O D28 -
46A	I/O D29 +	46B	I/O D29 -
47A	I/O D30 +	47B	I/O D30 -
48A	I/O D31 +	48B	I/O D31 -
49A	GND	49B	GND
50A	GND	50B	GND