

General Standards Corporation

High Performance Bus Interface Solutions

XMC-16AI32SSC1M

**32-Channel, Differential, 16-Bit Simultaneous Sampling
XMC Analog Input Board**

***With 1.0MSPS Sample Rate per Channel,
Time-tagging and Low-latency access***

Features

- 32 Differential analog inputs with dedicated 1.0MSPS 16-Bit ADC per channel
- Sampling rates to 1.0MSPS per channel
- Simultaneous sampling of all inputs; Minimum data skew
- Software-Selectable Input ranges: $\pm 10V$, $\pm 5V$, $\pm 2.5V$ or $\pm 1.25V$
- Sync and clock I/O support external control and multiboard configurations
- **Time Tagging** attaches time information to each input data value
- **Low Latency** provides 32 registers that duplicate the most recent samples from all channels
- Increased throughput capacity with local data packing
- Continuous, burst and single-sample clocking modes
- Hardware sync I/O for multiboard operation
- MByte FIFO data buffer; 512 K-Samples in packed-data mode
- 2-Channel DMA engine
- Conforms to PCI Express Specification revision 1.0a, x1 Link operating at 2.5Gbps
- Sample rate controlled by internal rate generators, by software triggering, or externally
- On-Demand internal Autocalibration of all channels
- **Same or Improved Performance Specifications as the PMC66-16AI32SSC**
- **Same System I/O pinout as the PMC66-16AI32SSC, as configured for Time Tagging**
- Single-width XMC form factor

Typical Applications

- | | | |
|------------------------------|-----------------------|--------------------------|
| ✓ High-Density Analog Inputs | ✓ Industrial Robotics | ✓ Acoustic Sensor Arrays |
| ✓ Analog Event Capture | ✓ Crash Analysis | ✓ Dynamic Test Systems |

--- PRELIMINARY ---

Rev: 112016

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8302A Whitesburg Drive · Huntsville, AL 35802
Phone: (256) 880-8787 or (800) 653-9970 FAX: (256) 880-8788 Email: Solutions@GeneralStandards.com

Functional Description

The 16-Bit XMC16AI32SSC1M analog input board provides 32 precision 16-Bit analog input channels on a standard single-width XMC module. All 32 inputs can be sampled simultaneously at rates from zero to 1MSPS, and the input range can be software-selected as $\pm 10V$, $\pm 5V$, $\pm 2.5V$ or $\pm 1.25V$. Each channel contains a dedicated 16-Bit sampling ADC, a differential input amplifier, and selftest input switches. Converted input data is available to the host bus through a 1-MByte FIFO buffer. The 32-Bit local data path supports full D32 local-bus data packing, or data can be accessed through low-latency data registers. Selectable Time Tagging attaches time information to each input data value. The board supports standard conduction-cooling.

Inputs can be sampled in groups of 2, 4, 8, 16 or 32 channels; or any contiguous channel group can be selected for sampling. The sample clock can be generated from an internal rate generator, or by software, or by external hardware.

On-demand autocalibration determines offset and gain correction values for each input channel, and applies the corrections subsequently during acquisition. A selftest switching network routes calibration reference signals to each channel through internal selftest switches, and permits board integrity to be verified by the host.

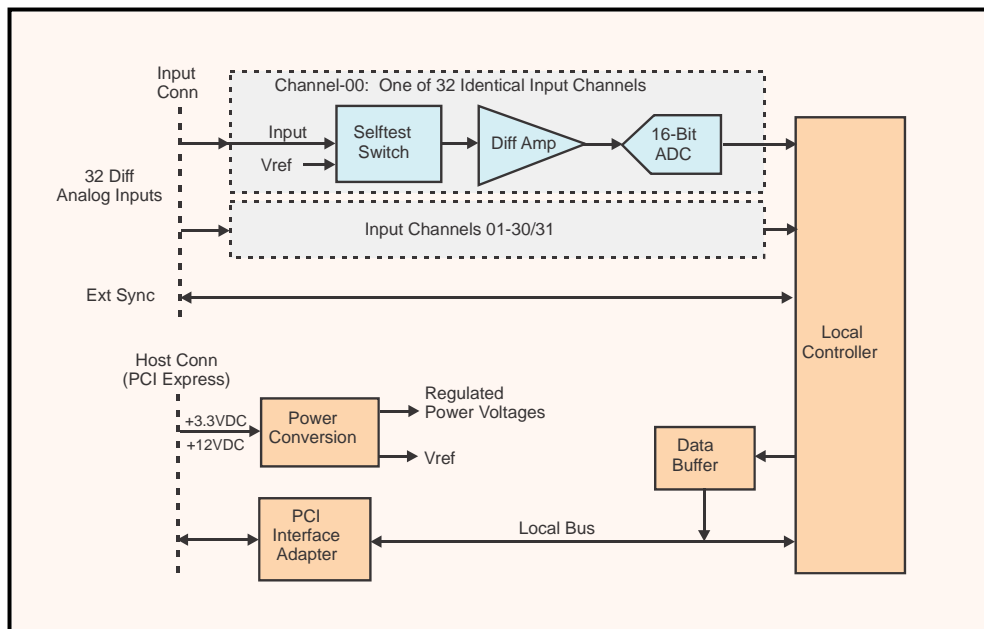


Figure 1. XMC-16AI32SSC1M; Functional Organization

This product complies with the IEEE PCI Express bus specification Revision 1.0a. System connections are made at the front panel through an 80-pin I/O connector. Power requirements consist of +12VDC and +3.3VDC in compliance with the PCI Express specification, and operation over the specified temperature range is achieved with conventional convection cooling.

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Performance Specifications

At +25 °C, with specified operating conditions, and with differential processing deselected

Input Characteristics:

Configuration:	32 differential analog input channels. 16-Channel version available.
Voltage Ranges:	Software configurable as $\pm 10V$, $\pm 5V$, $\pm 2.5V$ or $\pm 1.25V$ fullscale
Input Impedance:	2.0 Megohms typical, line-line. 1.0 Megohms line-ground..
Bias Current:	100nA maximum.
Common Mode Rejection:	80dB on $\pm 10V$ range; 85dB on $\pm 1.25V$ range; typical, DC-50kHz
Min/Max Input Levels for rated performance:	$\pm 11V$
Crosstalk Rejection:	85dB typical, DC-50kHz
Input Noise:	0.4mVRMS, $\pm 10V$ Range; 0.15mVRMS, $\pm 2.5V$ Range; typical, 0.01-250kHz
Overvoltage Protection:	Sustained ± 15 Volts with power removed; $\pm 30V$ with power applied

Transfer Characteristics:

Conversion Resolution:	16 Bits (0.0015 percent of FSR)		
Sample Rate:	Zero to 1,000 KSPS per channel		
Input Bandwidth (-3dB):	DC to 400 kHz typical		
Channels per Sample:	1-32		
DC Accuracy: (Maximum composite error after autocalibration)	<u>Range</u>	<u>Zero-Input</u>	<u>Fullscale</u>
	$\pm 10V$	$\pm 1.5mv$	$\pm 2.8mv$
	$\pm 5V$	$\pm 1.4mv$	$\pm 2.5mv$
	$\pm 2.5V$	$\pm 1.1mv$	$\pm 1.8mv$
	$\pm 1.25V$	$\pm 0.9mv$	$\pm 1.6mv$
Integral Nonlinearity:	± 0.008 percent of FSR, maximum		
Differential Nonlinearity:	± 0.004 percent of FSR, maximum		

Analog Input Operating Modes and Controls

Input Data Buffer:	FIFO; 1 Megabyte. 256 K-Samples in normal (16-Bit) mode; 512 K-samples in packed-data mode. A 'Low-Latency' array of 32 data registers is available in addition to the FIFO buffer.
Sample Clock Sources:	Internal rate generator; External Hardware Sync I/O, Software clock. Continuous, Burst and Single-Sample Clocking Modes.
Rate Generators:	Two rate generators provide sample rates from 0.016-1,000,000 sample clocks per second, by dividing the local master clock to the sample rate. (The standard master clock frequency is 64MHz. See ordering information for custom frequencies.)
External TTL Sync, Clock:	Bidirectional TTL lines; available through the I/O connector, or through a 6-pin connector located on the back of the board.
Input Data Format:	Nonpacked Mode: 16-Bit data word plus single-bit Channel-00 tag. Packed Mode: Lword sync code followed by packed channel data. Even-numbered channels occupy lower word (D00-15), odd channels occupy upper word (D16-31).
Data Format:	Selectable as offset binary or two's complement.
Low Latency:	In addition to the FIFO buffer, 32 data registers are directly accessible for minimum latency.
Time Tagging:	Provides 48-Bit 1-microsecond time stamping ('tagging') and windowed burst triggering.

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PCIe Compatibility:

Conforms to PCI Express Specification revision 1.0a; x1 Link operating at 2.5Gbps.
DMA transfers as bus master with two DMA channels.

Power Requirements:

+3.3VDC \pm 0.2 VDC, 0.9 Amps typical, 1.0 Amp maximum.
+12VDC \pm 0.4 VDC, 0.5 Amps typical, 0.6 Amps maximum
(or: +5VDC as VPWR, 1.2 Amps typical, 1.4 Amps maximum)
Total power consumption: 9.4 Watts typical, 11 Watts maximum.

Physical Parameters

Mechanical Characteristics

Height: 13.5 mm (0.53 in)
Depth: 149.0 mm (5.87 in)
Width: 74.0 mm (2.91 in)
Shield: Side-1 is protected by an EMI shield.

Environmental Specifications

Ambient Temperature Range: Operating: 0 to +65 Deg-C inlet air
(Optional extended-temp operation to +80 Deg-C).
Storage: -40 to +85 Degrees Celsius
Relative Humidity: Operating and Storage: 0 to 95%, non-condensing
Altitude: Operation to 10,000 ft.
Cooling: Conventional convection cooling; 150 LFPM

Ordering Information

Specify the basic product model number followed by an option suffix "-A-B-C", as indicated below. For extended-temperature operation to +80 Deg-C, add the suffix "I" to the base model number.

For example, model number XMC-16AI32SSC1M-32-64M-0 describes a board with 32 input channels, a standard 64.000MHz master clock frequency, and no custom features.

(All versions provide time tagging and low latency features).

Optional Parameter	Value	Specify Option As:
Number of Input Channels	32 Channels	A = 32
	16 Channels	A = 16
Master Clock Frequency:	64.000 MHz (Standard)	B = 64M
	Specify custom frequency; 64-66 MHz *	B = (Custom frequency)M
Custom Feature	No custom features	C = 0

* Frequencies other than the standard frequency will cause proportionate variations in the sample rate.

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System Interface Connector

Table 1. System Input/Output Connections

ROW-A		ROW-B	
PIN	SIGNAL	PIN	SIGNAL
1	INP00 LO	1	INP17 LO
2	INP00 HI	2	INP17 HI
3	INP01 LO	3	INP18 LO
4	INP01 HI	4	INP18 HI
5	INP02 LO	5	INP19 LO
6	INP02 HI	6	INP19 HI
7	INP03 LO	7	INP20 LO
8	INP03 HI	8	INP20 HI
9	INP04 LO	9	INP21 LO
10	INP04 HI	10	INP21 HI
11	INP05 LO	11	INPUT RTN
12	INP05 HI	12	INPUT RTN
13	INPUT RTN	13	INP22 LO
14	INPUT RTN	14	INP22 HI
15	INP06 LO	15	INP23 LO
16	INP06 HI	16	INP23 HI
17	INP07 LO	17	INP24 LO
18	INP07 HI	18	INP24 HI
19	INP08 LO	19	INP25 LO
20	INP08 HI	20	INP25 HI
21	INP09 LO	21	INP26 LO
22	INP09 HI	22	INP26 HI
23	INP10 LO	23	INPUT RTN
24	INP10 HI	24	INPUT RTN
25	INP11 LO	25	INP27 LO
26	INP11 HI	26	INP27 HI
27	INPUT RTN	27	INP28 LO
28	INPUT RTN	28	INP28 HI
29	INP12 LO	29	INP29 LO
30	INP12 HI	30	INP29 HI
31	INP13 LO	31	INP30 LO
32	INP13 HI	32	INP30 HI
33	INP14 LO	33	INP31 LO
34	INP14 HI	34	INP31 HI
35	INP15 LO	35	INPUT RTN
36	INP15 HI	36	REF CLK INP
37	INP16 LO	37	DIG RTN
38	INP16 HI	38	CLOCK I/O ¹ or SAMP CLK INP ²
39	INPUT RTN	39	DIG RTN
40	CLOCK RST INP	40	SYNC I/O ¹ or SAMP CLK OUT ²

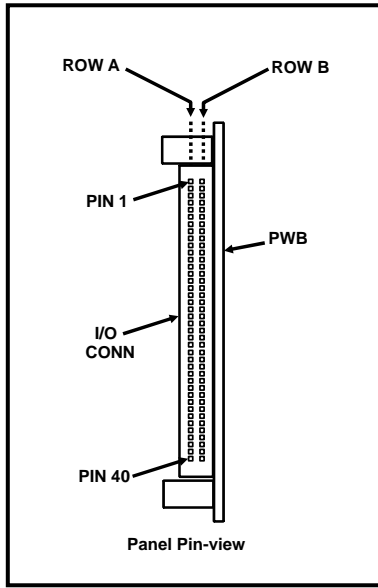
¹ Default configuration. Not software-configured for time tagging.

² If software-configured for time tagging.

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System Mating Connector:
Standard 80-pin 0.050" dual-ribbon socket connector:

Robinson Nugent **P50E-080S-TG**
or equivalent.

Figure 2. System I/O Connector

Table 2. Sync-I/O Connector

SYNC-I/O CONN PIN ¹	SIGNAL
1	DIG RTN
2	AUX CLOCK
3	DIG RTN
4	AUX SYNC
5	DIG RTN
6	Reserved. Connect to INPUT RTN or leave disconnected.

¹ Recommended Sync-I/O mating cable connector is: Molex# 51146-0600.

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