General Standards Corporation

High Performance Bus Interface Solutions

PMC66-16AISS8AO4

16-Bit, 12-Channel, 2-MSPS PMC Analog Input/Output Board

With Eight Simultaneously Sampled Analog Inputs, Four Analog Outputs, and Input Sampling Rates to 2.0 MSPS per channel

(Image in process)

Available also in PCI, cPCI and PC104-*Plus* form factors as:

PCI66-16AISS8AO4:	**PCI**, short length
cPCI66-16AISS8AO4:	**cPCI,** 3U
PC104P66-16AISS8AO4:	**PC104-*Plus***

See Ordering Information for details.

FEATURES:

- **Analog Inputs:**
  - 8 Differential Analog Inputs with Dedicated 16-Bit ADC per Channel
  - True Simultaneous Sampling of all Inputs to 2.0 MSPS per channel
  - SAR Architecture; No Minimum Sample Rate
- **Analog Outputs:**
  - 4 Single-Ended Analog Outputs with Dedicated 16-Bit DAC per Channel
  - Simultaneous Output Clocking Rates to 1.0 MSPS per Channel
  - Selectable Direct-Write or FIFO-Buffered Access
  - Buffer Configurable as Open for Data Streaming, or Circular for Periodic Functions
- **Common Analog I/O Features:**
  - Selectable Input/Output Ranges: ±10V, ±5V, ±2.5V
  - Independent 256-Ksample Input and Output FIFO Data Buffers
  - Hardware Clock and Sync I/O for Multiboard Operation
  - Internal Power Conversion; Single 5-Volt Power Requirement
  - DMA Engine Minimizes Bus Congestion
  - Timing Controlled by Internal Rate Generator, by Software Clocking, or Externally
  - Three Independent 24-Bit frequency dividers.
  - Internal Autocalibration
- 16-Bit Bidirectional TTL Digital I/O Port
- 66 MHz 32-Bit PCI Support, with Universal 5V/3.3V Signaling
- Single-Width PMC Form Fator with Integral EMI Shield.
- I/O Connector Pin-Compatible with PMC-12AISS8AO4, PMC-12AISS44AO4.

TYPICAL APPLICATIONS:

- ✓ High Performance Data Acquisition
- ✓ Arbitrary Waveform Generation
- ✓ Event Capture
- ✓ Ultrasound
- ✓ Robotics
- ✓ Positioning Systems

ADVANCE INFORMATION

REV: 110805

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FUNCTIONAL DESCRIPTION

The 16-Bit PMC-16AISS8AO4 analog I/O module samples and digitizes eight input channels simultaneously at rates up to 2.0 million samples per second for each channel. The resulting 16-bit sampled data is available to the PCI bus through a 256K-Sample FIFO buffer. Sampling can be controlled in groups of 1 through 8 channels, and the sample clock can be generated either from an internal rate generator, or through software, or by external hardware. Both burst and continuous sampling modes are supported. Input ranges are software-selectable as ±10V, ±5V, or ±2.5V. The inputs can be divided into two channel groups, with independent range assignments for both groups.

Four analog output channels provide software-selected output ranges of ±2.5V, ±5V or ±10V, and are accessed either directly through dedicated control registers, or output data can be routed through a 256K-Sample FIFO buffer for waveform generation. A 16-Bit bidirectional digital port can be configured as two independent byte-wide ports.

On-demand autocalibration determines and applies offset and gain correction values for all input and output channels. A selftest input switching network routes output channels or calibration reference signals to the analog inputs, and permits board integrity to be verified by the host..

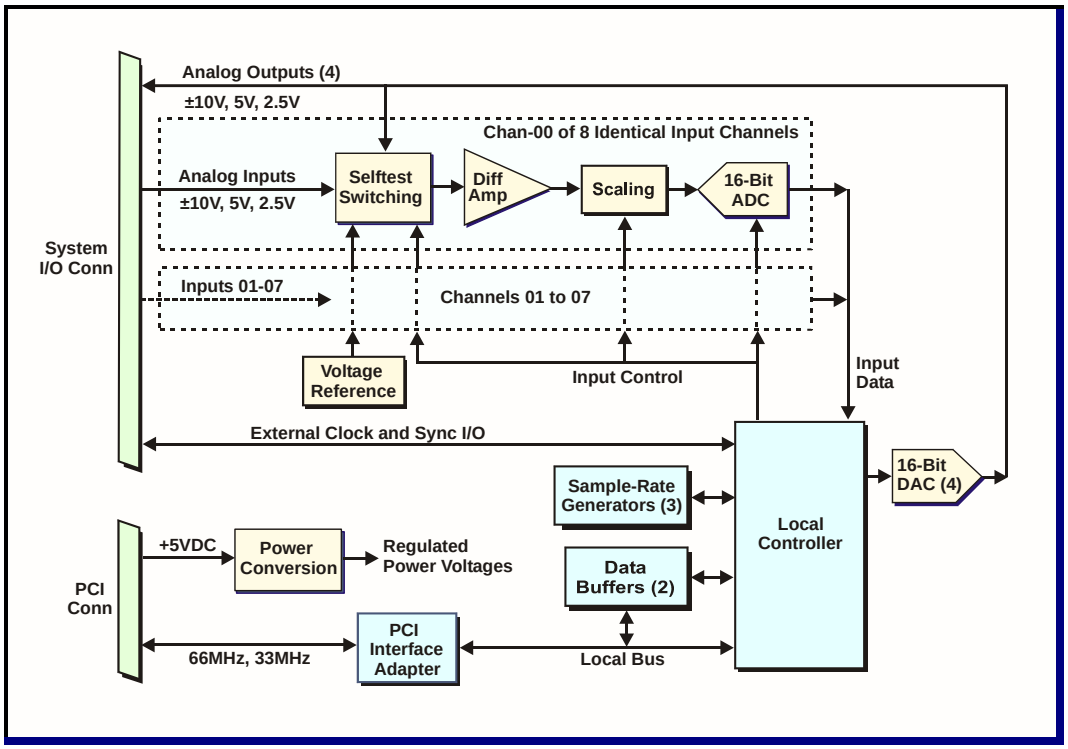

Figure 1. PMC-16AISS8AO4; Functional Organization

This product is functionally compatible with the IEEE PCI local bus specification Revision 2.3, and supports the "plug-n-play" initialization concept. System connections are made at the front panel through a high-density dual-ribbon 80-pin connector. Power requirements consist of +5 VDC in compliance with the PCI specification, and analog power voltages are generated internally. All operational parameters are software configurable. Operation over the specified temperature range is achieved with conventional air cooling.

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PERFORMANCE SPECIFICATIONS

At +25 ^{O}C, with specified operating voltages

Analog Input Characteristics:

Configuration:	Eight differential analog input channels; Dedicated 16-Bit ADC per channel. Optional 4-Channel version available.
Voltage Ranges:	Independently assignable between two groups of input channels as: ±10V, ±5V or ±2.5V full scale.
Input Impedance:	2 Megohms Line-Line in parallel with 40pF.
Bias Current:	100 nanoamps typical all ranges
Crosstalk Rejection:	84dB, DC-10kHz. 70dB at 100kHz.
Signal/Noise Ratio (SNR):	88dB typical; 10Hz to 500kHz
Common Mode Rejection:	65dB DC-10kHz; 53dB at 100kHz. Typical with CMV = ±10V, Vin = Zero.
Overvoltage Protection:	±25V with power applied, ±15 Volts with power removed.

Analog Input Transfer Characteristics:

Resolution:	16 Bits (0.0015 percent of FSR)		
Sample Rate:	Zero to 2.0 MSPS per channel		
Sampling Mode::	Simultaneous; all active input channels		
DC Accuracy:	Range	Midscale Accuracy	Fullscale Accuracy
(Maximum composite error after autocalibration)	±10V	± 2mV	± 5mV
	±5V	± 1mV	± 3mV
	±2.5V	± 0.8mV	± 2mV
Small Signal Bandwidth:	Zero to 5MHz, -3dB, all ranges		
Settling Time:	500ns to 0.1%; halfscale step; typical; all ranges.		
Power Bandwidth:	3MHz, 10Vp-p, -3dB		
Integral Nonlinearity:	±0.007 percent FSR (FSR = fullscale range; e.g.: 20Von ±10Vrange).		
Differential Nonlinearity:	±0.003 percent FSR.		

Analog Input Operating Modes and Controls

Input Data Buffer:	256K-sample FIFO
Sample Clock Sources:	Internal rate generator; External Hardware Clock I/O, Software clock.
Sampling Modes:	Continuous sampling, and triggered burst.
Internal Rate Generators:	Two independent rate generators, one for ADC clocking; one for burst triggering. Both programmable from 3-2,000,000 sample clocks per second, using 24-Bit dividers from the master clock frequency.
External Clock I/O:	TTL, bidirectional. Zero to 2,000,000 sample clocks per second.
Input Data Format:	16 Bits. Selectable as offset binary or two's complement. First-channel and end of-burst tagged.

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Analog Output Characteristics:

Configuration:	Four single-ended output channels. (Ordering option)
Voltage Ranges:	±10, ±5 or ±2.5 Volts; Independent of analog input ranges.
Output Resistance:	1.0 Ohm maximum at I/O connector pins.
Output protection:	Withstands sustained short-circuiting to ground
Load Current:	Zero to ±3ma per channel
Load Capacitance:	Stable with any load capacitance
Noise:	2.0mV-RMS, 10Hz-100KHz typical
Glitch Impulse:	7 nV-s, typical on ±5V range

Analog Output Transfer Characteristics:

Resolution:	16 Bits (0.0015 percent of FSR)		
Output Access:	Direct register access or 256K-Sample FIFO buffer.		
DC Accuracy:	Range	Midscale Accuracy	±Fullscale Accuracy
(Max error, no-load)	±10V	±4mV	±8mV
	±5V	±2mV	±6mV
	±2.5V	±1.5mV	±4mV
Settling Time:	2us to 0.1 percent, typical with halfscale step, no-load.		
Crosstalk Rejection:	70 dB minimum, DC-100 kHz		
Integral Nonlinearity:	±0.007 percent of FSR, maximum		
Differential Nonlinearity:	±0.002 percent of FSR, maximum		
Output Data Format:	16 Bits. Same format as selected for analog inputs.		

Analog Output Operating Modes and Controls

Output Data Buffer:	256K-sample FIFO
Sample Clock Sources:	Internal rate generator; External Clock I/O, Software clock.
Burst Triggering Sources:	TTL external Trigger I/O (shared with analog inputs), Software trigger.
Clocking Modes:	Continuous or periodic clocking, and triggered burst.
Internal Rate Generator:	Programmable from 3-1,000,000 output clocks per second. Divides Master Clock frequency to clocking rate using a 24-bit divider.
External Clock I/O:	TTL, bidirectional. Zero to 1,000,000 sample clocks per second.
Output Data Format:	16-Bits. Selectable as offset binary or two's complement.

Digital I/O Port:

Dual Independent 8-Bit bidirectional I/O ports. Standard TTL levels. Direct register Access.
±8 mA loading when configured as outputs. 0.15 mA source when configured as inputs.

PCI Compatibility:

Conforms to PCI Specification 2.3, D32 read/write, 33/66MHz, universal (5V/3.3V) signaling,
Provides one multifunction interrupt,
Supports block-mode DMA data transfers in two channels as bus master.

Power Requirements

+5VDC ±0.25 VDC at 1.5 Amp maximum, 1.1 Amp typical.

Maximum Power Dissipation: Side-1: 6.5 Watts. Side 2: 1.0 Watt.

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PHYSICAL PARAMETERS

Mechanical Characteristics *

Height: 13.5 mm (0.53 in)
Depth: 149.0 mm (5.87 in)
Width: 74.0 mm (2.91 in)
Shield: Side-1 is protected by an EMI shield.

* Mechanical dimensions are shown for the native single-width PMC form factor. See Ordering Information.

Environmental Specifications

Ambient Temperature Range:	Operating 0 to +65 Degrees Celsius inlet air: Storage: -40 to +85 Degrees Celsius
Relative Humidity:	Operating: 0 to 80%, non-condensing Storage: 0 to 95%, non-condensing
Altitude:	Operation to 10,000 ft.
Cooling:	Conventional air cooling; 150 LFPM

ORDERING INFORMATION

Specify the basic product model number followed by an option suffix "-A-B-C-D", as indicated below. For example, model number **PMC66-16AISS8AO4-8-4 -40.32M** describes a PMC module with eight input channels, four output channels, a 40.320MHz master clock frequency,and no custom features.

Basic Model Number	Form Factor
PMC66-16AISS8AO4	**PMC** (Native)
PCI66-16AISS8AO4 *	**PCI, short length**
cPCI66-16AISS8AO4 *	**cPCI, 3U**
PC104P66-16AISS8AO4 **	**PC104-*Plus***

* PMC module installed and tested on an adapter, with mechanical and functional equivalency.
** PMC module installed and tested on an adapter, with functional equivalency.
Contact factory for availability in native form factors.

Optional Parameter	Value	Specify Option As:
Number of Input Channels	**8 Input Channels**	**A = 8**
	4 Input Channels	**A = 4**
Number of Output Channels	**4 Output Channels**	**B = 4**
	No Analog Outputs	**B = 0**
Master Clock Frequency *	**40.320MHz**	**C = 40.32M**
Custom Feature	**---**	**D ****

* 40.320MHz if both 'C' and 'D' fields are blank. Custom frequencies available from 40-44MHz. Contact Sales for details.
** Numeric code, determined by specific feature. Blank or zero (0) if no custom feature applies.

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SYSTEM INTERFACE CONNECTOR

Table 1. System I/O Connector

ROW-A	
PIN	SIGNAL
1	OUTPUT RTN
2	ANA OUT 00
3	OUTPUT RTN
4	ANA OUT 01
5	OUTPUT RTN
6	ANA OUT 02
7	OUTPUT RTN
8	ANA OUT 03
9	INPUT RTN
10	INPUT RTN
11	INP00 LO *
12	INP00 HI *
13	INPUT RTN
14	INPUT RTN
15	INP01 LO *
16	INP01 HI *
17	INPUT RTN
18	INPUT RTN
19	INP02 LO **
20	INP02 HI **
21	INPUT RTN
22	INPUT RTN
23	INP03 LO **
24	INP03 HI **
25	INPUT RTN
26	INPUT RTN
27	INP04 LO *
28	INP04 HI *
29	INPUT RTN
30	INPUT RTN
31	INP05 LO *
32	INP05 HI *
33	INPUT RTN
34	INPUT RTN
35	INP06 LO **
36	INP06 HI **
37	INPUT RTN
38	INPUT RTN
39	INP07 LO **
40	INP07 HI **

ROW-B	
PIN	SIGNAL
1	DIGITAL RTN
2	DIO 00
3	DIGITAL RTN
4	DIO 01
5	DIGITAL RTN
6	DIO 02
7	DIGITAL RTN
8	DIO 03
9	DIGITAL RTN
10	DIO 04
11	DIGITAL RTN
12	DIO 05
13	DIGITAL RTN
14	DIO 06
15	DIGITAL RTN
16	DIO 07
17	DIGITAL RTN
18	DIO 08
19	DIGITAL RTN
20	DIO 09
21	DIGITAL RTN
22	DIO 10
23	DIGITAL RTN
24	DIO 11
25	DIGITAL RTN
26	DIO 12
27	DIGITAL RTN
28	DIO 13
29	DIGITAL RTN
30	DIO 14
31	DIGITAL RTN
32	DIO 15
33	VTEST RTN
34	VTEST
35	DIGITAL RTN
36	OUTPUT CLK I/O
37	DIGITAL RTN
38	TRIGGER I/O
39	DIGITAL RTN
40	INPUT CLK I/O

* Input Group-A. ** Input Group-B.
4 input-channel modules contain input Channels 00-03.

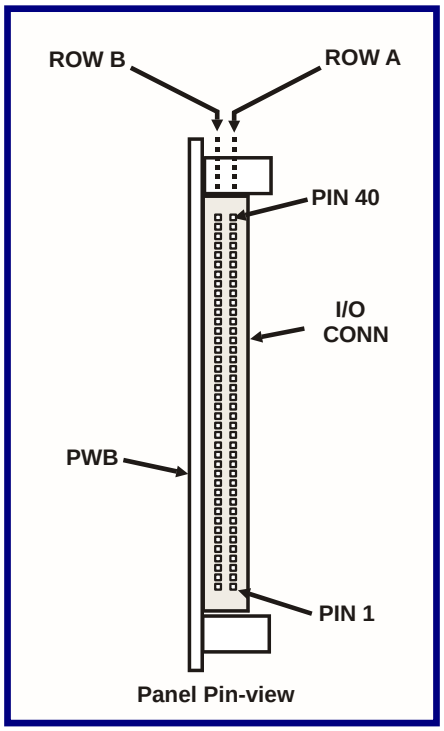

Figure 2. System I/O Connector

System Mating Connector:
Standard 80-pin 0.050" dual-ribbon socket:
Robinson Nugent **P50E-080S-TG,** or equivalent.

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