

General Standards Corporation

High Performance Bus Interface Solutions

PMC66-16A164SSA/C

64-Channel, 16-Bit Simultaneous Sampling PMC Analog Input Board

With 200 KSPS Sample Rate per Channel and 66 MHz PCI Support



Features

- 64 Analog Inputs with Dedicated 200KSPS 16-Bit ADC per Channel
- Simultaneous Sampling of all Inputs; Minimum Data Skew
- Sampling Rates to 200 KSPS per Channel (12.8 MSPS Aggregate Rate)
- D32; 66MHz, 33MHz PCI Compatibility, with Universal 5V/3.3V Signaling
- Increased Throughput Capacity with Local Data Packing
- Selectable Differential Processing Simulates Differential Operation of Channel Pairs
- Input Ranges: $\pm 10V$, $\pm 5V$, $\pm 2.5V$, $0/+5V$, $0/+10V$; Software-Selectable
- Hardware Sync I/O for Multiboard Operation
- 1 MByte FIFO Data Buffer
- 2-Channel DMA Engine
- Sampling Controlled by Internal Rate Generator, by Software Trigger, or Externally
- On-Demand Internal Autocalibration of all Channels
- Completely Software-Configurable; No Field Jumpers
- Auxiliary PXI Triggering Port Available through P1, P2.
- Single-width PMC Form Factor with Integral EMI Shield

Typical Applications

- | | | |
|------------------------------|-----------------------------|--------------------------|
| ✓ High-Density Analog Inputs | ✓ Industrial Robotics | ✓ Acoustic Sensor Arrays |
| ✓ Analog Event Capture | ✓ Biometric Signal Analysis | ✓ Dynamic Test Systems |

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Functional Description

The 16-Bit PMC66-16AI64SSA/C analog input board samples and digitizes 64 input channels simultaneously at rates up to 200,000 samples per second for each channel. Each input channel contains a dedicated 16-Bit sampling ADC, and the resulting 16-bit sampled data is available to the PCI bus through a 1 MByte FIFO buffer. The 32-Bit local data path supports full D32 local-bus data packing. Throughput capacity is further enhanced with 66MHz PCI support and increased local clocking frequency. All operational parameters are software configurable.

Inputs can be sampled in groups of 2, 4, 8, 16, 32 or 64 channels; or any single channel can be sampled continuously. The sample clock can be generated from an internal rate generator, or by software or external hardware. Input ranges are software-selectable as $\pm 10V$, $\pm 5V$ or $\pm 2.5V$.

An on-demand autocalibration feature determines offset and gain correction values for each input channel, and applies the corrections subsequently during acquisition. A selftest switching network routes calibration reference signals to each channel through internal selftest switches, and permits board integrity to be verified by the host..

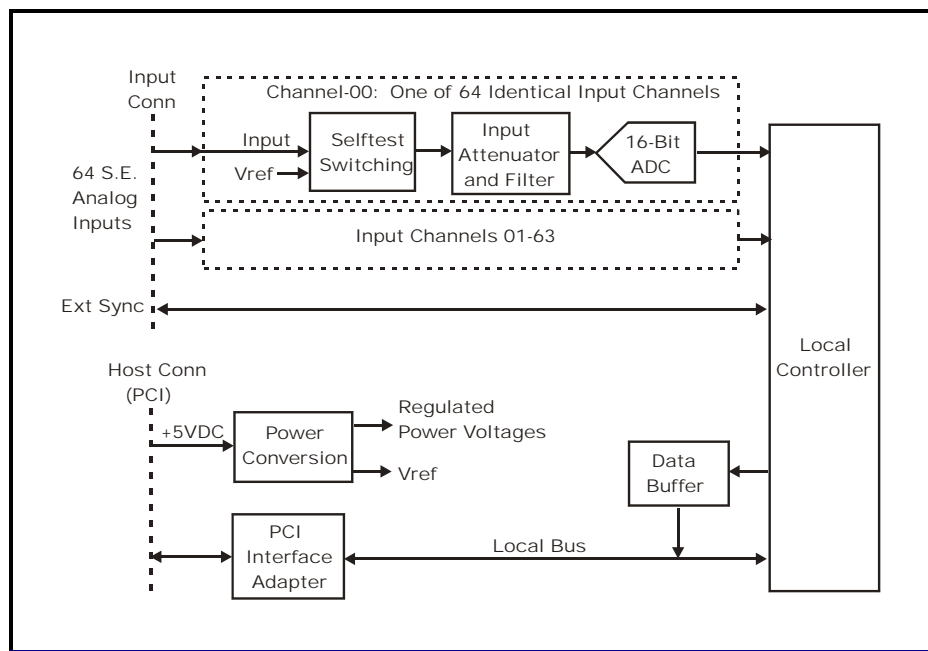


Figure 1. PM66-16AI64SSA; Functional Organization

This product is functionally compatible with the IEEE PCI local bus specification Revision 2.3, and supports the "plug-n-play" initialization concept. System connections are made at the front panel through a high-density 80-pin connector. Power requirements consist of +5 VDC, in compliance with the PCI specification, and operation over the specified temperature range is achieved with conventional convection cooling.

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Performance Specifications

At +25 °C, with specified operating conditions

Input Characteristics:

Configuration:	64 single-ended analog input channels; Dedicated 16-Bit ADC per channel. Optional 32-Channel version available.
Voltage Ranges:	Software configurable as $\pm 10V$, $\pm 5V$, $\pm 2.5V$, $0/+5V$ or $0/+10V$ full scale
Input Impedance:	750 KOhms, typical.
Bias Current:	1ua maximum, $\pm 2.5V$ range; 4ua maximum $\pm 10V$ range
Crosstalk Rejection:	85dB typical, DC-50kHz
Input Noise:	0.5 mVRMS; typical, all ranges; 0.01-50kHz
Overvoltage Protection:	± 40 Volts with power removed; $\pm 25V$ with power applied.

Transfer Characteristics:

Resolution:	16 Bits (0.0015 percent of FSR)																		
Maximum Sample Rate:	200 KSPS per channel																		
Input Bandwidth (-3dB):	DC to 120 kHz typical																		
Channels per Sample:	2, 4, 8, 16, 32 or 64 channels; or any single channel.																		
DC Accuracy: (Maximum composite error after autocalibration)	<table><thead><tr><th>Range</th><th>Zero-Input *</th><th>Fullscale *</th></tr></thead><tbody><tr><td>$\pm 10V$</td><td>$\pm 1.5mv$</td><td>$\pm 2.8mv$</td></tr><tr><td>$\pm 5V$</td><td>$\pm 1.4mv$</td><td>$\pm 2.5mv$</td></tr><tr><td>$\pm 2.5V$</td><td>$\pm 0.9mv$</td><td>$\pm 1.5mv$</td></tr><tr><td>$0/+10V$</td><td>$\pm 1.8mv$</td><td>$\pm 3.0mv$</td></tr><tr><td>$0/+5V$</td><td>$\pm 1.2mv$</td><td>$\pm 2.7mv$</td></tr></tbody></table>	Range	Zero-Input *	Fullscale *	$\pm 10V$	$\pm 1.5mv$	$\pm 2.8mv$	$\pm 5V$	$\pm 1.4mv$	$\pm 2.5mv$	$\pm 2.5V$	$\pm 0.9mv$	$\pm 1.5mv$	$0/+10V$	$\pm 1.8mv$	$\pm 3.0mv$	$0/+5V$	$\pm 1.2mv$	$\pm 2.7mv$
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Integral Nonlinearity:	± 0.008 percent of FSR, maximum																		
Differential Nonlinearity:	± 0.004 percent of FSR, maximum																		

* Averaged values, referred to inputs. Typical values are approximately one-half the maximum values shown here.

Analog Input Operating Modes and Controls

Input Data Buffer:	1 MByte; 512 K-Samples in packed-data mode.
Sample Clock Sources:	Internal rate generator; External Hardware Sync I/O, Software clock.
Rate Generator:	Programmable from 0.01-200,000 sample clocks per second. Divides a 50 MHz local clock to sample rate. (Alternate clock frequencies available).
External TTL Sync:	Bidirectional TTL line; Zero to 200,000 sample clocks per second.
Auxiliary Sync I/O:	Four independent bidirectional "PXI" lines in both PMC-P1/P2 and edge-board header; Zero to 200,000 sample clocks per second.
Input Data Format:	Nonpacked Mode: 16-Bit data word plus single-bit Channel-00 tag. Packed Mode: Lword sync code followed by packed channel data. Even-numbered channels occupy lower word (D00-15), odd channels occupy upper word (D16-31).
Data Format:	Selectable as offset binary or two's complement.
Differential Processing:	Selectable processing options process input data as 63 pseudo-differential channels or as 32 full-differential channels.

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PCI Compatibility:

Conforms to PCI Specification 2.3, with 66MHz/33MHz, D32 and universal signaling (5/3.3 Volt).
Single multifunction interrupt.
DMA transfers as bus master with two DMA channels.

Power Requirements

+5VDC \pm 0.2 VDC at 1.2 Amp maximum, 0.8 Amp typical.

Maximum Power Dissipation: Side-1: 5.0 Watts. Side 2: 1.0 Watt.

Physical Parameters

Mechanical Characteristics

Height: 13.5 mm (0.53 in)
Depth: 149.0 mm (5.87 in)
Width: 74.0 mm (2.91 in)
Shield: Side-1 is protected by an EMI shield.

Environmental Specifications

Ambient Temperature Range: Operating: 0 to +65 Degrees Celsius inlet air
Storage: -40 to +85 Degrees Celsius
Relative Humidity: Operating: 0 to 80%, non-condensing
Storage: 0 to 95%, non-condensing
Altitude: Operation to 10,000 ft.
Cooling: Conventional convection cooling; 150 LFPM

Ordering Information

Specify the basic product model number followed by an option suffix "-A-B-C", as indicated below. For example, model number PMC66-16AI64SSA/C-64-49.152M-50K describes a board with 64 input channels, a 49.152MHz master clock frequency, and a 50kHz input filter.

Optional Parameter	Value	Specify Option As:
Number of Input Channels	64 Channels	A = 64
	32 Channels	A = 32
Master Clock Frequency	45.000 MHz	B = 45.000M
	49.152 MHz	B = 49.152M
	50.000 MHz	B = Blank, or: 50.000M
Custom Feature	No custom features	C = Blank
	Input Filter = 50kHz	C = 50K

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System Interface Connector

Table 1. System I/O Connector

ROW-A		ROW-B	
PIN	SIGNAL	PIN	SIGNAL
1	INP00	1	INP32
2	INP01	2	INP33
3	INP02	3	INP34
4	INP03	4	INP35
5	INPUT RTN	5	INPUT RTN
6	INP04	6	INP36
7	INP05	7	INP37
8	INP06	8	INP38
9	INP07	9	INP39
10	INPUT RTN	10	INPUT RTN
11	INP08	11	INP40
12	INP09	12	INP41
13	INP10	13	INP42
14	INP11	14	INP43
15	INPUT RTN	15	INPUT RTN
16	INP12	16	INP44
17	INP13	17	INP45
18	INP14	18	INP46
19	INP15	19	INP47
20	INPUT RTN	20	INP48
21	INP16	21	INPUT RTN
22	INP17	22	INP49
23	INP18	23	INP50
24	INP19	24	INP51
25	INPUT RTN	25	INP52
26	INP20	26	INP53
27	INP21	27	INPUT RTN
28	INP22	28	INP54
29	INP23	29	INP55
30	INPUT RTN	30	INP56
31	INP24	31	INP57
32	INP25	32	INP58
33	INP26	33	INPUT RTN
34	INP27	34	INP59
35	INPUT RTN	35	INP60
36	INP28	36	INP61
37	INP29	37	INP62
38	INP30	38	INP63
39	INP31	39	SYNC I/O RTN
40	INPUT RTN	40	SYNC I/O

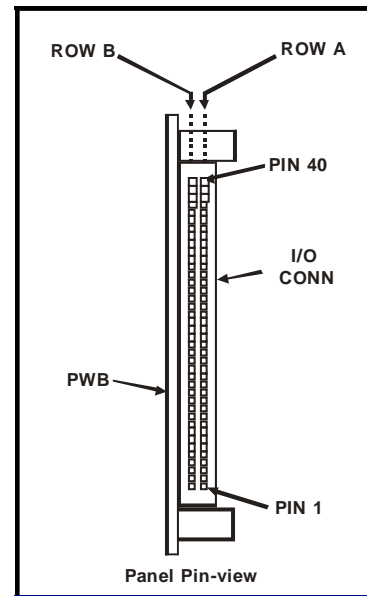


Figure 2. System Input Connector

System Mating Connector:

Standard 80-pin 0.050" dual-ribbon socket connector:

Robinson Nugent P50E-080S-TG, or equivalent.

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