

General Standards Corporation

High Performance Bus Interface Solutions

PMC64-HPDI32ALT

High-speed 64 Bit Parallel Digital I/O PCI Board

up to 200Mbytes/s Cable I/O



Features Include:

- Up to 200 Mbytes per second LVDS transfer rate @ 50MHz (20MHz default)
- Up to 100 Mbytes per second TTL transfer rate @ 25MHz (20MHz default)
- 264 Mbytes per second PCI transfer rate in burst mode.
- A single board can interface to a wide variety of external high-speed devices.
- Up to 128k x 32 (512 Kbytes) FIFO buffers allow data bursts to be transferred over the PCI bus independent of transfers over the cable.
- 64-Bit data transfers on the PCI bus.
- On-board controller, FIFOs, and DMA engine provide for continuous data transfer capability.
- Data input/output clock rate - up to 50 MHz LVDS / 25MHz TTL
- Data input/output width of 32 bits
- 64-Bit, 66MHz PCI v2.2 compliant
- Interrupts available upon DMA-comple, FIFO status, cable status, frame-valid and line-valid.
- External interrupt input line
- A variety of device drivers are available, including VxWorks, Windows, and Linux.

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Overview:

The PMC64-HPDI32ALT board is a very high speed parallel digital input/output board. The card provides for data I/O via the cable at up to 200 Mbytes per second for LVDS transceivers (100MBps for TTL) and can transfer data indefinitely without host intervention. The board employs General Standards' high performance PCI-DMA (PLX) engine. The PCI-DMA is easily set up and operated by writing only a few programming instruction statements to the board. Once the link between the PMC64-HPDI32ALT board and the external customer device is established, the desired data transfers between the two devices are performed and are transparent to the user. The board employs TTL or LVDS transceivers and the data path is 32 bits wide. The board will interface to a wide variety of digital I/O devices.

Functional Description:

The PMC64-HPDI32ALT board includes the PCI-DMA engine, FIFO memory, a 32-Bit cable input/output controller, and cable receivers (LVDS or TTL). The DMA engine is capable of transferring data to host memory using D64 block transfers; while the FIFO memory provides continuous transmission of data without interrupting the DMA transfers or requiring intervention from the Host CPU.

After the DMA is initialized and started, the Host CPU will be free to proceed with other duties and will need to only respond to interrupts.

The board also includes interrupt generation for interface flexibility and end-of-transfer indication. Interrupts are also available to indicate FIFO status (Transmit and Receive FIFO almost-empty and almost-full), cable status, and frame and line valid for easy manipulation of the cable interface.

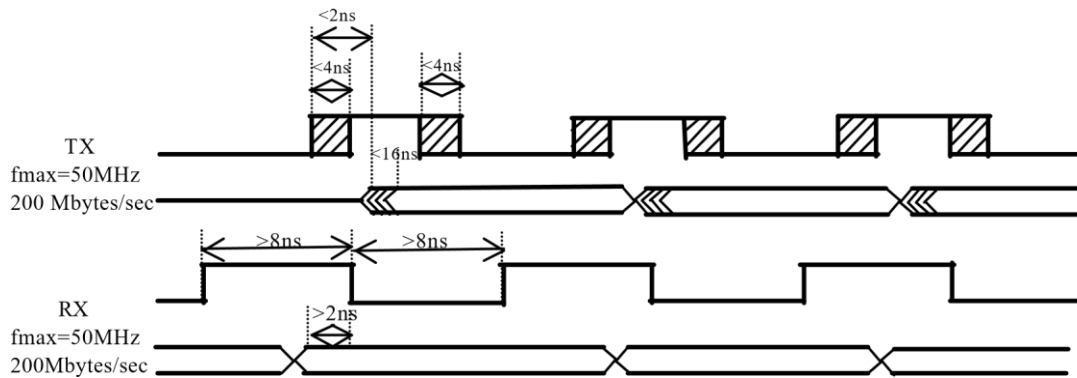
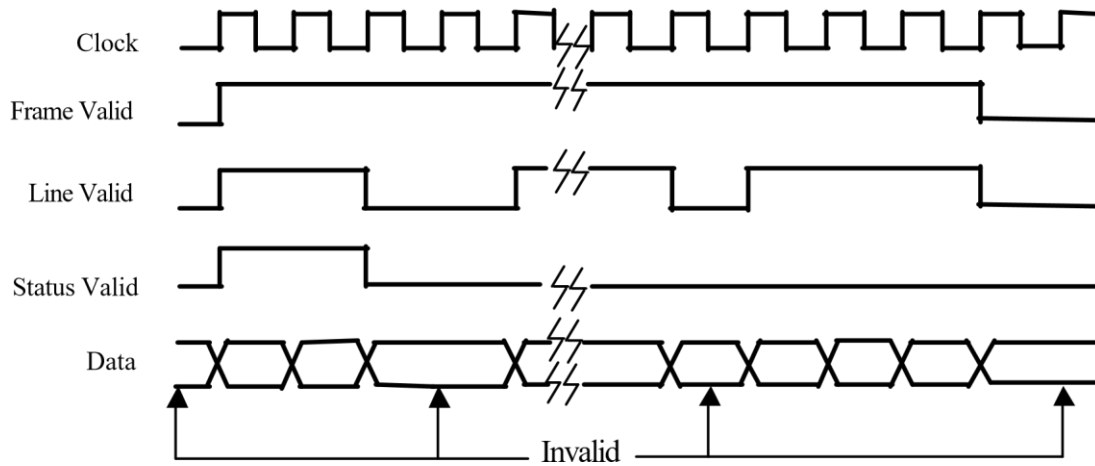
The PMC64-HPDI32ALT also offers 7 Bi-directional signals that can be customized to accommodate almost any handshaking protocol. General Standards routinely modifies the cable protocol to meet the customer's exact interface protocol.

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Cable Interface:

The cable interface provides for very high-speed reception of data (up to 200 Mbytes/sec). The cable interface provides for a data interface width of 32 bits. The data receivers are TTL or LVDS. The PMC64-HPDI32ALT board offers different cable transfer protocols that can be software defined to accommodate almost any handshake protocol desired. An example handshake protocol is shown in the following timing diagram.



Note: Data is transmitted on the rising edge of the Transmit clock and received on the negative edge of the receive clock.

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SPECIFICATIONS

DMA Transfer Rates

- Transfer Rate over cable (TTL Transceivers):
100 Mbytes/sec (Max) at 25 MHz clock rate and 32-bit cable interface.
- Transfer Rate over cable (LVDS Transceivers):
200 Mbytes/sec (max) at 50Mhz and 32 bit cable interface.
- PCI transfer rate from on-board FIFO to PCI:
264 Mbytes/sec max
- Data transfers over the cable do not interrupt data transfers over PCI since data is decoupled using FIFO buffering.

DMA Start Latency (when started by cable input or by CPU)

Initialization and DMA start: less than 1 microsecond typ.

FIFO Memory

The FIFOs on the PMC64-HPDI32ALT are used for buffering the transmit or receive data. There is a total of eight FIFOs on the board; 1 set of 4 for transmit, and 1 set of 4 for receive. Each set consists of 32 bits of data and 4 status flags. The receive FIFOs are loaded by the cable receive control logic and read by either the CPU or the DMA.

The transmit FIFOs are loaded by either the CPU or the DMA and read by the cable transmit control logic. The 4 status flags that accompany the FIFOs are all active low ('0' being TRUE) and are as follows: Empty, Almost Empty, Almost Full, Full. The Almost Empty and the Almost Full status flags can be programmed by the software to become true at most desired levels.

Cable Interface Transceivers

TTL levels

Output Voltage:	High > 2.5V Low >0.6V
Input Voltages are:	High > 2.0V Low >0.8V
Output sink capability:	64 mA
Output Source capability:	32 mA

LVDS levels

Low Voltage Differential :	$\pm 140-360\text{mV}$ Output Differential Voltage with +1-1.65 Offset Voltage.
Receiver Input Threshold:	$\pm 100\text{ mV}$.

The transceivers are configured in Bi-Directional Half-Duplex Receiver with termination resistors. The Termination resistors can be removed for Multi-drop Configurations.

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PCI INTERFACE

- Compatibility:** Conforms to 64-Bit 66MHz PCI Specification v2.2
 D64 read/write transactions.
 Supports "plug-n-play" initialization.
 Single multifunction interrupt.
 Supports DMA transfers as bus master.

MECHANICAL AND ENVIRONMENTAL SPECIFICATIONS

- Power Requirements**
 +5.0 VDC ±0.20 VDC at 4.5 Amps, maximum
- Physical Dimensions**
 Length: 149 mm
 Width: 74 mm
- Environmental Specifications**

Ambient Temperature Range:	Operating: 0 to +55 degrees Celsius	Storage: -40 to +85 degrees Celsius
Relative Humidity:	Operating: 0 to 80%, non-condensing	Storage: 0 to 95%, non-condensing
Altitude:	Operation to 10,000 ft.	
- Cooling Requirements**
 200 LFPM minimum air flow across component side of board;

ORDERING INFORMATION

PMC64-HPDI32ALT - <FIFO Size> - <Xcvr> - <Clock>

Option	Value	Description
FIFO Size	64K	8K x 32 FIFOs
	256K	32K x 32 FIFOs
	1M	128K x 32 FIFOs
Xcvr	(blank)	TTL transceiver
	LVDS	LVDS transceiver
Clock	(blank)	20MHz (80 Mbyte/sec)
	25MHz	25MHz (100 Mbyte/sec)
	50MHz	50MHz (200 Mbyte/sec)

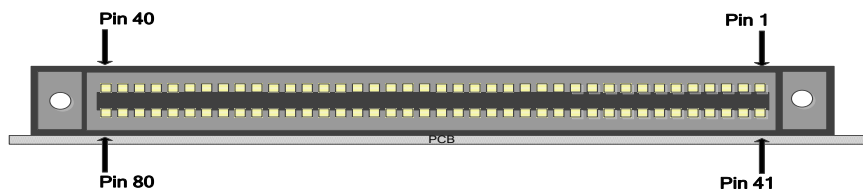
Consult factory for other Clock options

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SYSTEM I/O CONNECTIONS

User I/O Connector: 80 pin IO connector (female)
 Part Number: 3M P50E-080P1-SR1-EA
 Mating Connector: 3M P50E-080S-EA (50 mil twisted pair)
 3M P25E-080S-EA (25 mil non-twisted pair)



Pin No.	LVDS Signal	TTL Signal	Pin No.	LVDS Signal	TTL Signal
1	CABLE CLK +	CABLE CLK	41	CABLE D12 +	CABLE D12
2	CABLE CLK -	GND	42	CABLE D12 -	GND
3	CABLE CM D0 +	CABLE CM D0	43	CABLE D13 +	CABLE D13
4	CABLE CMD0 -	GND	44	CABLE D13 -	GND
5	CABLE CMD1 +	CABLE CM D1	45	CABLE D14 +	CABLE D14
6	CABLE CMD1 -	GND	46	CABLE D14 -	GND
7	CABLE CMD2 +	CABLE CM D2	47	CABLE D15 +	CABLE D15
8	CABLE CMD2 -	GND	48	CABLE D15 -	GND
9	CABLE CMD3 +	CABLE CM D3	49	CABLE D16 +	CABLE D16
10	CABLE CMD3 -	GND	50	CABLE D16 -	GND
11	CABLE CMD4 +	CABLE CM D4	51	CABLE D17 +	CABLE D17
12	CABLE CMD4 -	GND	52	CABLE D17 -	GND
13	CABLE CMD5 +	CABLE CM D5	53	CABLE D18 +	CABLE D18
14	CABLE CMD5 -	GND	54	CABLE D18 -	GND
15	CABLE CMD6 +	CABLE CM D6	55	CABLE D19 +	CABLE D19
16	CABLE CMD6 -	GND	56	CABLE D19 -	GND
17	CABLE D0 +	CABLE D0	57	CABLE D20 +	CABLE D20
18	CABLE D0 -	GND	58	CABLE D20 -	GND
19	CABLE D1 +	CABLE D1	59	CABLE D21 +	CABLE D21
20	CABLE D1 -	GND	60	CABLE D21 -	GND
21	CABLE D2 +	CABLE D2	61	CABLE D22 +	CABLE D22
22	CABLE D2 -	GND	62	CABLE D22 +	GND
23	CABLE D3 +	CABLE D3	63	CABLE D23 +	CABLE D23
24	CABLE D3 -	GND	64	CABLE D23 -	GND
25	CABLE D4 +	CABLE D4	65	CABLE D24 +	CABLE D24
26	CABLE D4 -	GND	66	CABLE D24 -	GND
27	CABLE D5 +	CABLE D5	67	CABLE D25 +	CABLE D25
28	CABLE D5 -	GND	68	CABLE D25 -	GND
29	CABLE D6 +	CABLE D6	69	CABLE D26 +	CABLE D26
30	CABLE D6 -	GND	70	CABLE D26 -	GND
31	CABLE D7 +	CABLE D7	71	CABLE D27 +	CABLE D27
32	CABLE D7 -	GND	72	CABLE D27 -	GND
33	CABLE D8 +	CABLE D8	73	CABLE D28 +	CABLE D28
34	CABLE D8 -	GND	74	CABLE D28 -	GND
35	CABLE D9 +	CABLE D9	75	CABLE D29 +	CABLE D29
36	CABLE D9 -	GND	76	CABLE D29 -	GND
37	CABLE D10 +	CABLE D10	77	CABLE D30 +	CABLE D30
38	CABLE D10 -	GND	78	CABLE D30 -	GND
39	CABLE D11 +	CABLE D11	79	CABLE D31 +	CABLE D31
40	CABLE D11 -	GND	80	CABLE D31 -	GND

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