

PCI66-18AISS8A08

8-Input, 8-Output 18-Bit Precision Wideband 500KSPS PCI Analog Input/Output Board With Selectable Current-Loop Input Terminators

FEATURES:

8 Differential 18-Bit Analog Input Channels

Simultaneous Sampling; Individual Low-Latency SAR 18-Bit ADC per input channel
DC to 500KSPS sample rate per channel; 0-4 MSPS aggregate rate
500-Ohm current-loop input termination; 0-20mA; Individually selectable per channel.
Dual lowpass 4th-Order filters per channel; Software-selectable.

8 Single-ended or 3-Wire Differential 18-Bit Analog Output Channels

Simultaneous Clocking; Individual R-2R 18-Bit DAC per output channel
DC to 500KSPS Sample Rate per Channel; 0-4 MSPS aggregate rate
High Current $\pm 15\text{mA}$ Outputs Available with 4-Channel Configuration

Common Input/Output Characteristics:

Input/Output ranges: $\pm 10\text{V}$, $\pm 5\text{V}$, $\pm 2.5\text{V}$, $0/+10\text{V}$, $0/+5\text{V}$. Independent input and output ranges.
Synchronous or independent input/output clocking
Independent 512K-sample input and output FIFO Buffers; 1024K-samples total; Optional 512K-samples total.

Supporting Features:

8 Bidirectional Digital I/O lines; TTL compatible

Internal Sample Rate Generators with 24-Bit rate dividers
Hardware Sync and Clock I/O for Multiboard Synchronization
Conforms to PCI Bus Specification, Revision 2.3, 66/33 MHz with Universal Signaling
Standard Full-Length PCI Form Factor
DMA Engine Supports both Block-Mode and Demand-Mode Transfers in Two Channels
On-demand Autocalibration
Integrated DC/DC Conversion and Dual Regulation for Internal Supply Voltages

TYPICAL APPLICATIONS:

- | | | |
|------------------------|-------------------|-----------------------|
| ✓ Voltage Input/Output | ✓ Servo Systems | ✓ Waveform Generation |
| ✓ Current-Loop Inputs | ✓ Process Control | ✓ Positioning Systems |

REV: 072814

FUNCTIONAL DESCRIPTION

The PCI66-18AISS8AO8 is a precision 18-Bit analog I/O product that provides eight simultaneously sampled input channels and eight simultaneously clocked output channels. Inputs and outputs can be clocked synchronously or independently at rates up to 500 KSPS per channel, and are supported by independent 512K-Sample FIFO data buffers. Both continuous and burst clocking modes are supported, and voltage ranges are independently software-selectable as $\pm 10V$, $\pm 5V$, $\pm 2.5V$, 0 to $+10V$ or 0 to $+5V$ for inputs and outputs. Clocking and triggering rates can be derived from internal rate generators, or from external clock and trigger sources to support the synchronous operation of multiple boards.

Input sampling employs successive-approximation (SAR) conversion, which avoids the high latency or minimum-rate limitations of delta-sigma and pipelined conversion schemes. Each analog input channel can be individually programmed to provide termination for current-loop instrumentation. The analog outputs use a weighted-DAC R-2R configuration which, like the analog inputs, minimizes latency and has no minimum clocking rate. The outputs can be software-configured for either single-ended or 3-wire differential operation.

On-demand autocalibration determines and applies error correction for all input and output channels, and a selftest input switching network permits board integrity to be verified by the host. Eight bidirectional digital I/O lines are programmable as inputs or outputs.

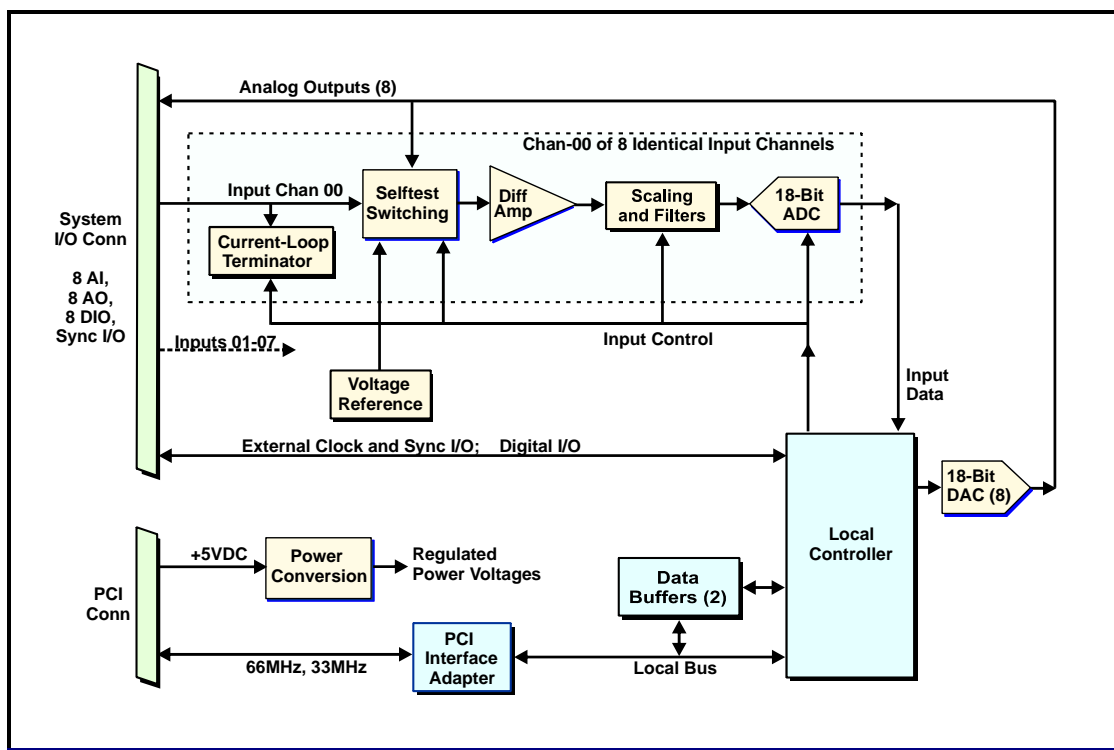


Figure 1. PCI66-18AISS8AO8; Functional Organization

This product complies with the IEEE PCI local bus specification Revision 2.3. System connections are made at the front panel through a high-density dual-ribbon 100-pin connector. Power requirements consist of $+5$ VDC in compliance with the PCI specification, and analog power voltages are generated internally. Operation over the specified temperature range is achieved with conventional air cooling.

PERFORMANCE SPECIFICATIONS

At +25 °C, with specified operating voltages

Analog Input Characteristics:

| | |
|---------------------------|--|
| Configuration: | Eight simultaneously sampled input channels with dedicated 18-Bit SAR ADC per channel. Optional 4-Channel version available. |
| Voltage Ranges: | $\pm 10V$, $\pm 5V$, $\pm 2.5V$, $0/+10V$ or $0/+5V$ full scale for all input channels, software-selectable independently of the selected output range. |
| Input Impedance: | Loop termination disabled: 2 Megohms $\pm 10\%$; Line-Line in parallel with 80pF. Loop termination enabled: 510 Ohms ± 8 Ohms in parallel with 150pF. |
| Bias Current: | 50 nanoamps typical, all ranges. Loop terminators disabled. |
| Crosstalk Rejection: | 90dB typical DC-10kHz. 80dB at 250kHz. |
| Common Mode Rejection: | 65dB DC-80kHz; 50dB at 500kHz. Typical with CMV = $\pm 12V$, $V_{in} = \text{Zero}$. |
| Input Voltage Limits | $\pm 12V$ line-ground on any input for normal operation. |
| Overvoltage Protection: | $\pm 15V$ with power applied, ± 4 Volts with power removed. $\pm 30mA$ max overdrive. If current-loop option is omitted: power applied: $\pm 30V$, power removed: $\pm 15V$. |
| Current Loop Terminators: | Software-selected individually by channel. 500 Ohms $\pm 0.05\%$ sensing; with 510 ± 8 Ohms across the input lines. 0.4 Watts maximum per channel. |

Input Transfer Characteristics:

| | | | |
|---|---|--------------------------|---|
| Resolution: | 18 Bits (0.0004 percent of FSR) | | |
| Sample Rate: | Zero to 500KSPS per channel. | | |
| Sampling Mode:: | Simultaneous; Successive-approximation conversion, all active inputs. | | |
| DC Accuracy: | <u>Range</u> | <u>Midscale Accuracy</u> | <u>\pmFullscale Accuracy</u> |
| (Maximum composite error after autocalibration) | $\pm 10V$ | $\pm 0.5mV$ | $\pm 1.5mV$ |
| | $\pm 5V$ | $\pm 0.3V$ | $\pm 1.0mV$ |
| | $\pm 2.5V$ | $\pm 0.2mV$ | $\pm 0.6mV$ |
| | <u>Range</u> | <u>Zero Accuracy</u> | <u>+Fullscale Accuracy</u> |
| | $0/+10V$ | $\pm 0.5mV$ | $\pm 1.0mV$ |
| | $0/+5V$ | $\pm 0.3V$ | $\pm 0.8mV$ |
| Small Signal Bandwidth: | Zero to 1.0MHz with no filter selected, or Zero to selected filter frequency. | | |
| Input Filters: | Selectable for all channels as 80kHz, 200kHz or no filter. 4th-order continuous-time Butterworth. | | |
| Settling Time: | 5us to 0.1% for halfscale step; typical with no filter selected. | | |
| Power Bandwidth: | 2.2 Vpp-MHz; -3dB; typical with no filter selected. | | |
| Signal/Noise Ratio (SNR): | 89dB typical; 10Hz - 250kHz; referred to fullscale rms input. | | |
| Integral Nonlinearity: | ± 0.002 percent FSR (FSR = fullscale range; e.g.: 20V on $\pm 10V$ range). | | |
| Differential Nonlinearity: | ± 0.001 percent FSR. | | |

Input Operating Modes and Controls

| | |
|---------------------------|--|
| Input Data Buffer: | 512K-sample FIFO |
| Sample Clock Sources: | Internal rate generator; External Hardware Clock I/O, Software clock. |
| Sampling Modes: | Continuous sampling or triggered burst. |
| Internal Rate Generators: | Two independent rate generators, one for ADC clocking; one for burst triggering. Both programmable from 3-500,000 sample clocks per second, using 24-Bit dividers from the master clock frequency. |
| External Sync I/O: | TTL, clock and burst trigger. Zero to 500,000 sample clocks per second. |
| Input Data Format: | 18 Bits, selectable as offset binary or two's complement coding, with attached channel number and end-of-burst tag. Coding shared with analog outputs. |

Analog Output Characteristics:

| | |
|---------------------------|---|
| Configuration: | Eight simultaneously clocked output channels with dedicated 18-Bit R-2R DAC per channel. Selectable as either single-ended or 3-wire balanced differential. 4-Channel version available. |
| Voltage Ranges: | $\pm 10V$, $\pm 5V$, $\pm 2.5V$, $0/+10V$ or $0/+5V$ full scale for all output channels, software-selectable independently of the selected input range. |
| Output Resistance: | 1.0 Ohm maximum at I/O connector pins. |
| Output protection: | Withstands sustained short-circuiting to ground |
| Maximum Loading: | Stable with any load capacitance: 8-Channel configuration: Zero to $\pm 5ma$, any single channel. <i>Maximum total of 24mA on all outputs</i> 4-Channel configuration: Same as 8-Channel config, or optionally Zero to $\pm 15ma$, any or all channels. |
| Line Imbalance: | (Differential output mode) $\pm 15mV$ max. |
| Signal/Noise Ratio (SNR): | 90dB typical on $\pm 10V$ range; 10Hz - 250kHz |
| Glitch Impulse: | 15 nV-s, typical on $\pm 5V$ range |

Analog Output Transfer Characteristics:

| | | | |
|----------------------------|---|---------------------------|--|
| Resolution: | 18 Bits (0.0004 percent of FSR) | | |
| Output Access: | 512K-Sample FIFO buffer. | | |
| DC Accuracy: | <u>S.E. Range</u> | <u>S.E. Zero Accuracy</u> | <u>S.E. \pmFullscale Accuracy</u> |
| (Max error, no-load) | $\pm 10V$ | $\pm 0.6mV$ | $\pm 1.7mV$ |
| | $\pm 5V$ | $\pm 0.4V$ | $\pm 1.2mV$ |
| | $\pm 2.5V$ | $\pm 0.3mV$ | $\pm 0.7mV$ |
| | $0/+10V$ | $\pm 0.6mV$ | $\pm 1.2mV$ |
| | $0/+5V$ | $\pm 0.4V$ | $\pm 0.9mV$ |
| | <u>Diff Range</u> | <u>Diff Zero Accuracy</u> | <u>Diff \pmFullscale Accuracy</u> |
| | $\pm 10V$ | $\pm 1.5mV$ | $\pm 9mV$ |
| | $\pm 5V$ | $\pm 1.2V$ | $\pm 5mV$ |
| | $\pm 2.5V$ | $\pm 1.2mV$ | $\pm 3mV$ |
| | $0/+10V$ | $\pm 1.3mV$ | $\pm 5mV$ |
| | $0/+5V$ | $\pm 1.1V$ | $\pm 3mV$ |
| Settling Time: | 8 μ s to 0.1 percent, typical with halfscale step, no-load. | | |
| Crosstalk Rejection: | 90 dB minimum, DC-100 kHz | | |
| Integral Nonlinearity: | ± 0.002 percent of FSR, maximum | | |
| Differential Nonlinearity: | ± 0.001 percent of FSR, maximum | | |

Analog Output Operating Modes and Controls

| | |
|--------------------------|---|
| Output Data Buffer: | 512K-sample FIFO |
| Sample Clock Sources: | Internal rate generator; External Clock I/O, Software clock. 500kHz max. |
| Triggering Sources: | Internal rate generator, TTL external trigger I/O, Software trigger. |
| Clocking Modes: | Continuous or periodic. Supports triggered functions. |
| Internal Rate Generator: | Programmable from 3 to 500,000 output clocks per second. Divides Master Clock frequency to clocking rate using a 24-bit divider. |
| External Sync I/O: | TTL, clock and trigger. Zero to 500,000 output clocks per second. |
| Output Data Format: | 18 Bits, selectable as offset binary or two's complement coding, with attached end-of-function flag and channel number. Coding shared with analog inputs. |

Digital Input/Outputs:

Eight TTL I/O lines in two groups of four bits, group-configurable as inputs or outputs. 0.2ma maximum input loading as current source, 8ma output loading as either source or sink. Direct register control.

PCI Compatibility:

Conforms to PCI Specification 2.3, D32 read/write, 33/66MHz, universal (5V/3.3V) signaling, Supports block-mode and demand-mode DMA data transfers as bus master in two channels.

Power Requirements

+5VDC ±0.25 VDC at 4.0 Amps typical, 4.8 Amps maximum. Supplied by PCI bus.

PHYSICAL PARAMETERS

Physical Dimensions (Excluding panel bracket)

Height: 106.7 mm (4.20 in)
Depth: 312.0 mm (12.28 in)
Width: 21.6 mm (0.85 in).

Environmental Specifications

Ambient Temperature Range: Operating 0 to +65 Degrees Celsius inlet air;
Storage: -40 to +85 Degrees Celsius

Relative Humidity: Operating: 0 to 80%, non-condensing
Storage: 0 to 95%, non-condensing

Altitude: Operation to 10,000 ft.

Cooling: Conventional air cooling; 150 LFPM

ORDERING INFORMATION

Specify the basic product model number followed by an option suffix "-A-B-C-D-E", as indicated below. For example, model number **PCI66-18AISS8AO8-88-4M-F1-40.32M-0** describes a PCI module with eight input channels, eight output channels, Type-F1 input filters, a 40.320MHz master clock frequency, and standard outputs loading.

| Optional Parameter | Value | Specify Option As: |
|--------------------------|---|--------------------|
| Number of Channels: | 4 input channels and 4 output channels | A = 44 |
| | 8 input channels and 8 output channels | A = 88 |
| Buffer Capacity | 512K-samples; 2MByte effective capacity | B= 2M |
| | 1024K-samples; 4MByte effective capacity | B= 4M |
| Input Filter Frequencies | Standard 80kHz and 200kHz | C= F1 |
| | * | * |
| Master Clock Frequency | Standard 40.32MHz. | D= 40.32M |
| | * | * |
| Custom Features | No custom features | E=0 |
| | 15mA analog output loading (4-channel versions only) | E=15MA |

* Contact factory for custom frequencies.

SYSTEM INTERFACE CONNECTOR

Table 1. System I/O Connector

| ROW-A | | ROW-B | |
|-------|---------------|-------|-----------------|
| PIN | SIGNAL | PIN | SIGNAL |
| 1 | INPUT 00 LO | 1 | OUTPUT 04 LO |
| 2 | INPUT 00 HI | 2 | OUTPUT 04 HI |
| 3 | INPUT RTN | 3 | OUTPUT RTN 04 |
| 4 | INPUT RTN | 4 | OUTPUT RTN 04 |
| 5 | INPUT 01 LO | 5 | OUTPUT 05 LO |
| 6 | INPUT 01 HI | 6 | OUTPUT 05 HI |
| 7 | INPUT RTN | 7 | OUTPUT RTN 05 |
| 8 | INPUT RTN | 8 | OUTPUT RTN 05 |
| 9 | INPUT 02 LO | 9 | OUTPUT 06 LO |
| 10 | INPUT 02 HI | 10 | OUTPUT 06 HI |
| 11 | INPUT RTN | 11 | OUTPUT RTN 06 |
| 12 | INPUT RTN | 12 | OUTPUT RTN 06 |
| 13 | INPUT 03 LO | 13 | OUTPUT 07 LO |
| 14 | INPUT 03 HI | 14 | OUTPUT 07 HI |
| 15 | INPUT RTN | 15 | OUTPUT RTN 07 |
| 16 | INPUT RTN | 16 | OUTPUT RTN 07 |
| 17 | INPUT 04 LO | 17 | VTEST RTN |
| 18 | INPUT 04 HI | 18 | VTEST |
| 19 | INPUT RTN | 19 | DIGITAL RTN |
| 20 | INPUT RTN | 20 | DIGIO 00 |
| 21 | INPUT 05 LO | 21 | DIGITAL RTN |
| 22 | INPUT 05 HI | 22 | DIGIO 01 |
| 23 | INPUT RTN | 23 | DIGITAL RTN |
| 24 | INPUT RTN | 24 | DIGIO 02 |
| 25 | INPUT 06 LO | 25 | DIGITAL RTN |
| 26 | INPUT 06 HI | 26 | DIGIO 03 |
| 27 | INPUT RTN | 27 | DIGITAL RTN |
| 28 | INPUT RTN | 28 | DIGIO 04 |
| 29 | INPUT 07 LO | 29 | DIGITAL RTN |
| 30 | INPUT 07 HI | 30 | DIGIO 05 |
| 31 | INPUT RTN | 31 | DIGITAL RTN |
| 32 | INPUT RTN | 32 | DIGIO 06 |
| 33 | OUTPUT RTN 00 | 33 | DIGITAL RTN |
| 34 | OUTPUT RTN 00 | 34 | DIGIO 07 |
| 35 | OUTPUT 00 LO | 35 | DIGITAL RTN |
| 36 | OUTPUT 00 HI | 36 | OUTPUT CLK INP |
| 37 | OUTPUT RTN 00 | 37 | DIGITAL RTN |
| 38 | OUTPUT RTN 00 | 38 | OUTPUT CLK OUT |
| 39 | OUTPUT 01 LO | 39 | DIGITAL RTN |
| 40 | OUTPUT 01 HI | 40 | OUTPUT TRIG INP |
| 41 | OUTPUT RTN 01 | 41 | DIGITAL RTN |
| 42 | OUTPUT RTN 01 | 42 | OUTPUT TRIG OUT |
| 43 | OUTPUT 02 LO | 43 | DIGITAL RTN |
| 44 | OUTPUT 02 HI | 44 | INPUT CLK INP |
| 45 | OUTPUT RTN 02 | 45 | DIGITAL RTN |
| 46 | OUTPUT RTN 02 | 46 | INPUT CLK OUT |
| 47 | OUTPUT 03 LO | 47 | DIGITAL RTN |
| 48 | OUTPUT 03 HI | 48 | INPUT TRIG INP |
| 49 | OUTPUT RTN 03 | 49 | DIGITAL RTN |
| 50 | OUTPUT RTN 03 | 50 | INPUT TRIG OUT |

The 4-channel configuration contains input/output Channels 00-03.

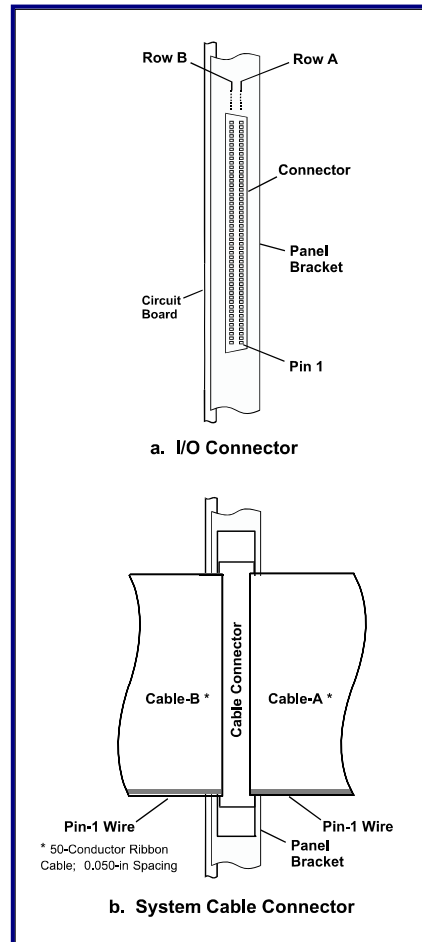


Figure 2. System I/O Connections

System Cable Mating Connector:
 100-Pin 2-row 0.050" dual
 ribbon-cable connector:
 AMP # 749621-9.

**I/O Connector Installed on
 Board (Ref):**
 AMP # 787170-9

General Standards Corporation assumes no responsibility for the use of any circuits in this product. No circuit patent licenses are implied. Information included herein supersedes previously published specifications on this product and is subject to change without notice.