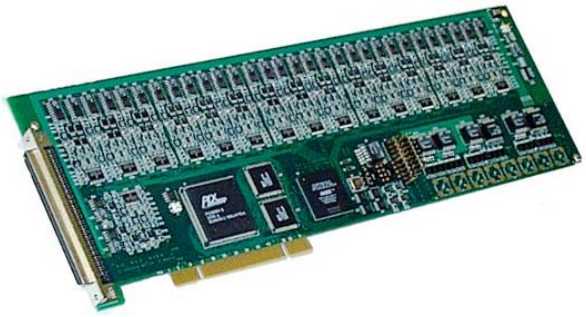
General Standards Corporation

High Performance Bus Interface Solutions

PCI-24DSI32

32-Channel 24-Bit Delta-Sigma PCI Analog Input Board

With 200 KSPS Sample Rate per Channel



FEATURES:

- **32 Differential 24-Bit Analog Input Channels**
- **Delta-Sigma Converter per Channel, with Linear Phase Digital Antialias Filtering**
- **Sample rates from 2 KSPS to 200 KSPS per Channel**
- **Software-Selectable Input Ranges: ±2.5V, ±5V, ±10V**
- 256 K-sample FIFO Buffer
- Synchronous Operation; All Channels Clocked Simultaneously
- Internal Sample Rate Generator
- Hardware Sync and Clock I/O for Multiboard Synchronization
- Low Phase Skew; Typically Less than 0.1-Degree with Fsig < 0.35*Fsamp
- DMA Engine Supports both Block-Mode and Demand-Mode Transfers
- Low Power Consumption. 12 Watts Typical. Only +5VDC Required from PCI bus.
- 100dB Dynamic Range; 93 dB SINAD
- On-demand Autocalibration Ensures DC Offset Precision as well as AC performance
- Integrated DC/DC Conversion and Regulation of Precision Internal Supply Voltages
- Conforms to PCl Bus Specification, Revision 2.3, with Universal Signaling

TYPICAL APPLICATIONS:

✓ Sonar Arrays	✓ Voltage Acquisition	✓ Phase Comparison
✓ Analog Inputs	✓ Acoustic Analysis	✓ Audio Waveform Analysis

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Overview:

The 32-channel PCI-24DSI32 analog input board provides high-density 24-bit analog input resources on a standard PCI expansion board. Optimized for flexibility and performance, the board is ideal for a wide variety of applications, ranging from simple precision voltage measurements, to the analysis of complex audio signals and waveforms. 32 delta-sigma analog input channels are organized into four simultaneously-clocked groups, three of which can be independently enabled or disabled. Multiple boards can be synchronized and phase-locked. Input bandwidth is from DC to 80kHz. Sample rates are adjustable from 2KSPS to 200KSPS, and the input range is software selectable as ±2.5V, ±5V or ±10V. Internal autocalibration networks permit on-demand calibration to be performed without removing the board from the system.

An optional configuration provides four independent internal rate generators, each of which can be assigned to any or all of the four channel groups.

Functional Description:

A PCI interface adapter provides the interface between the controlling PCI bus and the internal local controller through a 32-bit local bus (Figure 1). Each of 32 analog input channels contains a lowpass image filter, and a delta-sigma A/D converter that provides digital antialias filtering. An internal voltage reference can be applied to all channels to support selftest operations and autocalibration. Gain and offset trimming is performed by applying correction values that are determined during on-demand autocalibration.

Each ADC contains a linear-phase digital antialiasing filter that rejects out-of-band signals. Lowpass analog input filters reject those interference signals that fall within the harmonic images of the digital filter.

The internal sample-rate generator is adjustable over a 2:1 frequency range, and is divided down within the local controller to provide individual channel sample rates from 2KSPS to 200KSPS. Conversion data from all active channels is transferred to the PCI bus through a 256K-sample data buffer that is supported by two DMA channels.

Multiple channels can be synchronized to perform sampling in "lockstep", either by a software command, or by external hardware sync and clock input signals. Hardware sync and clock input/output signals permit multiple boards to be connected together in daisy-chain or star configurations for phase-locked operation from a common clock.

This product is functionally compatible with the IEEE PCI local bus specification Revision 2.3, and supports the "plug-n-play" initialization concept. System input/output connections are made at the panel bracket through a high-density 100-Pin I/O connector. Power requirements consist of +5 VDC, in compliance with the PCI specification, and operation over the specified temperature range is achieved with minimal 200 LFPM air cooling.

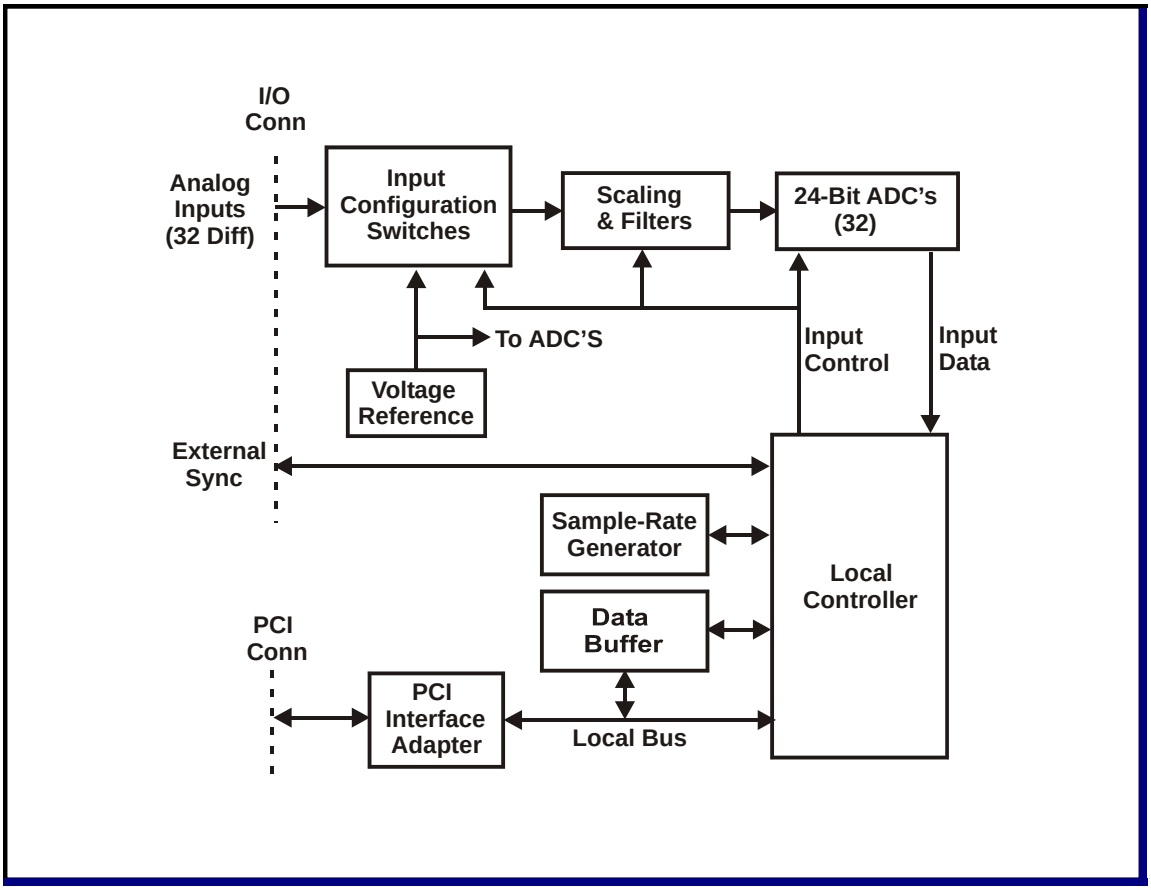

Figure 1. PCI-24DSI32; Functional Organization

SPECIFICATIONS

At +25 ^{O}C, with specified operating voltages.

Input Characteristics:

Configuration:	32 differential input channels. 8 and 16-channel configurations available.
Voltage Range:	Software Configurable as ±2.5 Volts, ±5 Volts or ±10 Volts
Input Impedance:	1.0 Megohm typical, in parallel with 20 pF. 2.0 Megohms line-line.
Common Mode Rejection:	80dB to 1kHz; 60dB to 50kHz.; typical
Common Mode Range:	±11 Volts with zero normal-mode input
Overvoltage Protection:	±25-Volt transients with power applied; ±45 Volts with power removed

Transfer Characteristics:

Quantizing Resolution:	24 Bits
Sample Rate:	2,000 to 200,000 samples per second per channel
Oversampling Factor:	2-50ksps: x128; 50-100ksps: x64; 100-200ksps: x32

DC Accuracy:
(Maximum composite error after autocalibration)

Input Range	Midrange (Zero) Accuracy	Gain Accuracy at Fsamp 2-10ksps	Gain Accuracy at Fsamp 10-200ksps
±10V	±0.5mV	±0.3%	±0.1%
±5V	±0.3mV	±0.3%	±0.1%
±2.5V	±0.1mV	±0.3%	±0.1%

Bandwidth (-3dB): DC to typically 49 percent of selected sample rate for sample rates to 100KSPS, or to 40 percent of sample rate from 100kSPS to 200KSPS. Typically DC to 80 kHz overall.
0.1dB to 0.45Fsamp; 2-100KSPS; 0.24Fsamp 100-200KSPS.

Passband Ripple: ±0.06dB maximum

Phase Skew: Typically less than 55ns (0.1-Degree for Fsig = 5kHz), with Fsig/Fsamp <0.35; channel-channel (board-board for multiboard configurations), excluding noise, with high-frequency image filter.

Stopband Characteristics

Sample Rate:	Threshold*	Rejection*
2-50KSPS:	0.58 Fsamp	93dB
50-100KSPS:	0.68 Fsamp	90dB
100-200KSPS:	0.78 Fsamp	95dB

* Typical values. (Fsamp = sample rate)

Antialias Filtering: Each ADC provides linear-phase digital antialias filtering as indicated for "Stopband Characteristics." Sample-rate images from the digital filter are suppressed with a 2-Pole Butterworth filter with a software-selectable cutoff frequency of either 40kHz or 270kHz. Alternative filter frequencies are available.

Dynamic Range: 100dB; typical 2 KSPS to 200 KSPS

SINAD: (Signal to Noise-and-Distortion ratio):
93dB typical to 10 kHz input bandwidth; 86 dB typical to 40 kHz
(93dB typical to 40kHz with optional extended low-distortion range)

Interchannel Crosstalk: -96dB typical to 50kHz

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Operating Modes and Controls

Organization:	Four analog input channel groups. All channels in all groups operate at the same sample rate which is further controlled by division of the selected rate generator frequency. Each channel group contains one-fourth of the channels on the board.
Internal Rate Generator:	An internal rate generator provides sample rates from 2.0 KSPS to 200 KSPS. Setting-resolution is 0.2 percent or less, and setting accuracy is ±25PPM.
External Clock I/O:	An LVDS hardware clock output can be derived either from a 0.512-51.200 MHz LVDS external hardware input clock or from an internal rate generator. Multiple boards can be locked to a common clock by daisy-chaining the output clock from each board to the input clock of the next board in the chain. Any number of boards can be daisy-chained together, with a typical propagation delay of 10ns introduced per board. Star-configuration also is supported.
Synchronization:	Sampling of multiple channel groups can be synchronized through software, or each group can be synchronized to an external LVDS hardware sync input. By using the daisy-chain configuration described for External Clock I/O, hardware sync inputs and outputs can be used to synchronize sampling among multiple boards.
Data Format:	Software-selectable as either offset binary or two's complement. Width of the data-field is selectable as 16, 18, 20 or 24 bits.
Channel Tags:	Each input data value is appended with a 5-bit channel tag.
Buffer Threshold Flag:	Asserted when the number of samples in the selected buffer exceeds the selected threshold. The buffer threshold can be any integer from 0 0000 to 3 FFFEh.
Buffer Access:	The input buffer FIFO is accessed through either of two DMA channels, with both block-mode and demand-mode transfers supported.

PCI COMPATIBILITY

Conforms to PCI Specification 2.3: D32, 33MHz, 3.3V/5V signaling.
Supports "plug-n-play" initialization.
Single multifunction interrupt on INTA#.
Two-Channel DMA in block and demand modes.

Power Requirements

+5.0 VDC ±0.25 VDC at 2.4 Amps typical, 3.5 Amps, maximum
(4.0 Amps typical, 6.0 Amps maximum with extended low-distortion range option)

Physical Dimensions (Excluding panel bracket)

Height: 106.7 mm (4.20 in)
Depth: 312.0 mm (12.28 in)
Width: 21.6 mm (0.85 in)

Environmental Specifications

Ambient Temperature Range:`	Operating: 0 to +65 degrees Celsius inlet air (Contact factory for extended operating range) Storage: -40 to +85 degrees Celsius
Relative Humidity:	Operating: 0 to 80%, non-condensing Storage: 0 to 95%, non-condensing
Altitude:	Operation to 10,000 ft.

Cooling Requirements: 200 LFPM minimum air flow across component side of board; .

ORDERING INFORMATION

Specify the basic product model number (PCI-24DSI32), followed by an option suffix "-A-B-C-D", as indicated below. For example, model number PCI-24DSI32-32-SD-0-PL25 describes a board with 32 input channels, standard low-distortion range, standard image filter frequencies, and a PLL rate generator..

Optional Parameter	Value	Specify Option As:
Number of Input Channels:	8 Channels	A = 8
	16 Channels	A = 16
	32 Channels	A = 32
Low-Distortion Range	Standard low- distortion range	B = SD
	Extended low-distortion range (Increased power consumption)	B = ELD
Image Filter Frequencies	Standard 40kHz and 270kHz	C= 0
	33kHz and 130kHz	C= 1 or AA1*
	10kHz and 80kHz	C= 2
Rate Generator	Standard Resolution: 0.2-percent resolution, ±0.08% Accuracy **	D= Blank or SR **
	Phase-Locked Loop (PLL), ±25PPM Accuracy	D= PL25

Notes:

* C = AA1 indicates a custom configuration. Use C= 1 for this option if not previously ordered as C = AA1.
** This option will be supported indefinitely for legacy systems, but is not recommended for new applications.

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SYSTEM I/O CONNECTIONS

I/O CONNECTOR PIN ASSIGNMENTS

ROW-A	
PIN	FUNCTION
1	CLOCK INPUT LO
2	CLOCK INPUT HI
3	SYNC INPUT LO
4	SYNC INPUT HI
5	DIGITAL RETURN
6	DIGITAL RETURN
7	CLOCK OUTPUT LO
8	CLOCK OUTPUT HI
9	SYNC OUTPUT LO
10	SYNC OUTPUT HI
11	INPUT RETURN
12	INPUT RETURN
13	VTEST RETURN
14	VTEST OUTPUT
15	INPUT RETURN
16	INPUT RETURN
17	INPUT CH 00 LO
18	INPUT CH 00 HI
19	INPUT CH 01 LO
20	INPUT CH 01 HI
21	INPUT CH 02 LO
22	INPUT CH 02 HI
23	INPUT CH 03 LO
24	INPUT CH 03 HI
25	INPUT CH 04 LO
26	INPUT CH 04 HI
27	INPUT CH 05 LO
28	INPUT CH 05 HI
29	INPUT CH 06 LO
30	INPUT CH 06 HI
31	INPUT CH 07 LO
32	INPUT CH 07 HI
33	INPUT CH 08 LO
34	INPUT CH 08 HI
35	INPUT CH 09 LO
36	INPUT CH 09 HI
37	INPUT CH 10 LO
38	INPUT CH 10 HI
39	INPUT CH 11 LO
40	INPUT CH 11 HI
41	INPUT CH 12 LO
42	INPUT CH 12 HI
43	INPUT CH 13 LO
44	INPUT CH 13 HI
45	INPUT CH 14 LO
46	INPUT CH 14 HI
47	INPUT CH 15 LO
48	INPUT CH 15 HI
49	INPUT RETURN
50	INPUT RETURN

ROW-B	
PIN	FUNCTION
1	(Reserved, N/C)
2	(Reserved, N/C)
3	DIGITAL RETURN
4	DIGITAL RETURN
5	(Reserved, N/C)
6	(Reserved, N/C)
7	INPUT RETURN
8	INPUT RETURN
9	INPUT CH 16 LO
10	INPUT CH 16 HI
11	INPUT CH 17 LO
12	INPUT CH 17 HI
13	INPUT CH 18 LO
14	INPUT CH 18 HI
15	INPUT RETURN
16	INPUT RETURN
17	INPUT CH 19 LO
18	INPUT CH 19 HI
19	INPUT CH 20 LO
20	INPUT CH 20 HI
21	INPUT CH 21 LO
22	INPUT CH 21 HI
23	INPUT RETURN
24	INPUT RETURN
25	INPUT CH 22 LO
26	INPUT CH 22 HI
27	INPUT CH 23 LO
28	INPUT CH 23 HI
29	INPUT CH 24 LO
30	INPUT CH 24 HI
31	INPUT RETURN
32	INPUT RETURN
33	INPUT CH 25 LO
34	INPUT CH 25 HI
35	INPUT CH 26 LO
36	INPUT CH 26 HI
37	INPUT CH 27 LO
38	INPUT CH 27 HI
39	INPUT RETURN
40	INPUT RETURN
41	INPUT CH 28 LO
42	INPUT CH 28 HI
43	INPUT CH 29 LO
44	INPUT CH 29 HI
45	INPUT CH 30 LO
46	INPUT CH 30 HI
47	INPUT CH 31 LO
48	INPUT CH 31 HI
49	INPUT RETURN
50	INPUT RETURN

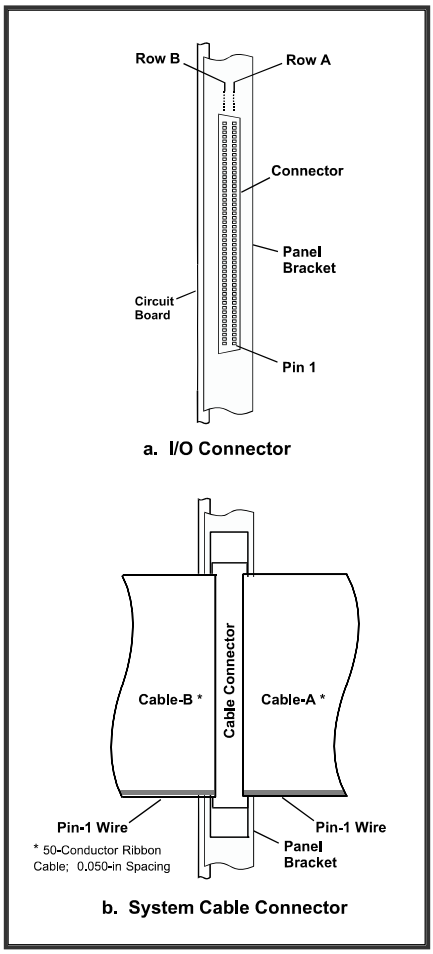

Figure 2. System I/O Connections

System Cable Mating Connector:
100-Pin 2-row 0.050" dual ribbon-cable connector: AMP # 749621-9.

I/O Connector Installed on Board (Ref)**:**
AMP # 787170-9

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