General Standards Corporation

High Performance Bus Interface Solutions

PC104P-24DSI6LN

Six-Channel Low-Noise 24-Bit Delta-Sigma PC104-*Plus* Analog Input Module

With 200 KSPS Sample Rate per Channel

Available also in PCI, cPCI and PMC form factors as:

PCI-24DSI6LN:	**PCI**, short length
cPCI-24DSI6LN:	**cPCI,** 3U
PMC-24DSI6LN:	**PMC**

See Ordering Information for details.

FEATURES:

- **6 Differential 24-Bit Analog Input Channels**
- **Delta-Sigma Converter per Channel, with Linear Phase Digital Antialias Filtering**
- **Sample rates from 2 KSPS to 200 KSPS per Channel**
- **±10V Input Range; or Optional ±2.5V or ±5V Input Range**
- **Software-Compatible, and I/O Connector-Compatible with PC104P-24DSI12**
- 256 K-sample FIFO Buffer
- Synchronous or Independent ADC Clocking
- Internal Sample Rate Generators
- Hardware Sync and Clock I/O for Multiboard Synchronization
- Supports GPS Synchronization to a 1PPS Input
- Low Phase Skew; Typically Less than 55ns with Fsig < 0.35*Fsamp
- DMA Engine Supports both Block-Mode and Demand-Mode Transfers
- 112dB Dynamic Range to 100KSPS in AC-coupled mode; 100dB DC-coupled
- Integrated DC/DC Conversion and Regulation of Precision Internal Supply Voltages
- Conforms to PCl Bus Specification, Revision 2.3, with Universal Signaling
- Available in Alternate Form Factors: PCI, cPCI, PMC

TYPICAL APPLICATIONS:

✓ Sonar Arrays	✓ Voltage Acquisition	✓ Phase Comparison
✓ Analog Inputs	✓ Acoustic Research	✓ Audio Waveform Analysis

PRELIMINARY

REV 111612

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Overview:

The 6-channel PC104P-24DSI6LN analog input board provides high-density 24-bit analog input resources on a standard PC104-*Plus* module. This module is ideal for a wide variety of dynamic applications, including the analysis of complex audio signals and waveforms.

Functional Description:

Each of six analog input channels contains a lowpass image filter and a delta-sigma A/D converter that provides digital antialias filtering. A linear-phase digital antialiasing filter rejects out-of-band signals, and a lowpass analog filter reject those interference signals that fall within the harmonic images of the digital filter. Input response can be selected as DC coupled for response down to DC, or as AC-coupled for maximum dynamic range.

An internal sample-rate generator is adjustable over a 2:1 frequency range, and is divided down within the local controller to provide individual channel sample rates from 2KSPS to 200KSPS. Conversion data from all active channels is transferred to the PCI bus through a 256K-sample data buffer that is supported by two DMA channels. Multiple channels can be synchronized to perform sampling in "lockstep", either by a software command, or by external hardware sync and clock input signals.

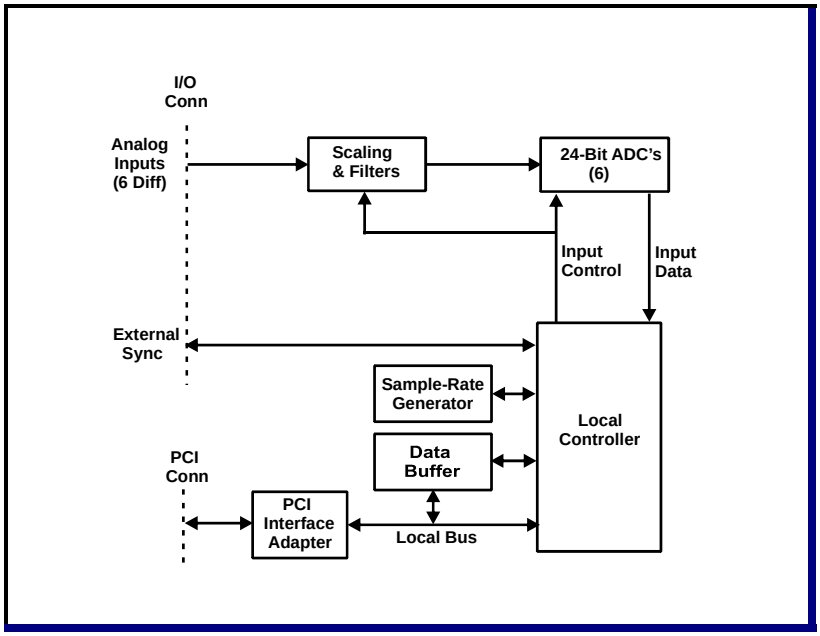

Figure 1. PC104P-24DSI6LN; Functional Organization

This product is functionally compatible with the IEEE PCI local bus specification Revision 2.3. System input/output connections are made at the front panel through a high-density 68-Pin I/O connector. Power requirements consist of +5 VDC, in compliance with the PCI specification, and operation over the specified temperature range is achieved with conventional 150 LFPM air cooling.

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ELECTRICAL SPECIFICATIONS

At +25 ^{O}C, with specified operating conditions.

Input Characteristics:

Configuration:	6 differential input channels. 4-channel configuration available.
Voltage Range:	Factory configured as ±10 Volts (standard), ±5 Volts or ±2.5 Volts
Input Impedance:	1.0 Megohm typical, in parallel with 20 pF; 2.0 Megohms line-line.
Input Coupling:	Selectable as either AC-coupled or DC-coupled. AC coupling provides lower noise.
Common Mode Rejection:	60dB to 50kHz.; typical
Common Mode Range:	±11 Volts with zero normal-mode input
Overvoltage Protection:	±25-Volt transients with power applied; ±15 Volts with power removed

Transfer Characteristics:

Quantizing Resolution:	24 Bits
Sample Rate:	2,000 to 200,000 samples per second per channel
Oversampling Factor:	2-50ksps: x128; 50-100ksps: x64; 100-200ksps: x32
DC Offset:	±50mV max; Inputs connected to input return.
Passband (0.1dB):	Sample Rate: Typical, DC Coupling* 2-50ksps: DC to 0.47 Fsamp 50-100ksps: DC to 0.46 Fsamp 100-200ksps: DC to 0.24 Fsamp *-0.13dB low end of passband is Fsamp/2400 in AC-coupled mode. E.g.: 20Hz if Fsamp=48KSPS.
Passband Ripple:	±0.06dB maximum
Stopband:	Sample Rate: Threshold Rejection 2-50ksps: 0.58 Fsamp 100dB 50-100ksps: 0.68 Fsamp 95dB 100-200ksps: 0.78 Fsamp 100dB
Phase Skew:	Typically less than 55ns (0.1-Degree for Fsig = 5kHz), with Fsig/Fsamp <0.35; channel-channel (board-board for multiboard configurations), excluding noise, with high-frequency image filter.
Antialias Filtering:	Each ADC provides linear-phase digital antialias filtering as indicated for Passband and Stopband. A 270kHz lowpass analog image filter in each channel suppresses images from the digital filter. Optional alternative image filter frequencies are available, and should be selected to be well above the expected passband.
Dynamic Range:	112dB to 100KSPS, typical with AC coupling; 100dB with DC coupling. 78dB above 100KSPS; AC or DC coupled.
SINAD:	98dB typical to Fsig=20kHz and sample rates to 100KSPS.
Interchannel Crosstalk:	-100dB typical to 50kHz

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Operating Modes and Controls:

Organization:	Two analog input channel groups. All channels in each group operate at the same sample rate, which is further controlled by division of the selected rate generator frequency. Each channel group contains one-half of the channels on the board, and can operate either synchronously from a single rate generator, or independently from either of two generators.
Sample Rate Generators:	Two independent internal PLL rate generators provide sample rates from 2.0 KSPS to 200 KSPS. The frequency of each generator is controlled by the ratio of two 10-Bit integers, and setting accuracy is 25 PPM.
External Clock I/O:	An LVDS or TTL hardware input clock can be derived either from a 25.6-51.2 MHz external hardware input or from an internal rate generator. Multiple boards can be locked to a common clock by daisy-chaining the output clock from each board to the input clock of the next board in the chain. Any number of boards can be daisy-chained together, with a typical propagation delay of 10ns introduced per board. The 'star-configuration' also is supported.
Synchronization:	Sampling of multiple channel groups can be phase-synchronized through software, or each group can be synchronized to an external hardware clock input. Daisy-chained hardware sync inputs and outputs can be used to synchronize sampling among multiple boards. Synchronization to a 1PPS GPS input also is supported.
Data Format:	Software-selectable as either offset binary or two's complement. Width of the data-field is selectable as 16, 18, 20 or 24 bits.
Channel Tags:	A channel tag is appended to each input data value.
Buffer Threshold Flag:	Asserted when the number of samples in the selected buffer exceeds the selected threshold. The threshold can be any integer from zero to 3 FFFEh.
Buffer Access:	The input buffer FIFO is accessed through either of two DMA channels, with both block-mode and demand-mode transfers supported.

PCI Compatibility:

Conforms to PCI Specification 2.3: D32, 33MHz, universal (3.3V/5V) signaling.

Supports "plug-n-play" initialization.

Single multifunction interrupt on INTA#.

Two-Channel DMA as bus master in block and demand modes.

Power Requirements:

+5.0 VDC ±0.25 VDC at 1.2 Amps typical, 1.5 Amps, maximum

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Mechanical Characteristics:

Height: 23.3 mm (0.92 in); Width: 94.0 mm (3.78 in); Depth: 95.9 mm (3.70 in)

(Mechanical dimensions are shown for the native PC104-*Plus* form factor. See Ordering Information.)

Environmental Specifications:

Ambient Temperature Range:`	Operating: Standard: 0 to +65 degrees Celsius inlet air Extended: -40 to +80 degrees Celsius inlet air Storage: -40 to +85 degrees Celsius.
Relative Humidity:	Operating: 0 to 80%, non-condensing Storage: 0 to 95%, non-condensing
Altitude:	Operation to 10,000 ft.
Cooling:	Conventional convection cooling; 150 LFPM

Ordering Information:

Specify the basic product model number followed by an option suffix "-A-B-C-D", as indicated below. For example, model number PC104P-24DSI6LN-4 describes a PC104-*Plus* module with four ±10V input channels, standard lowpass analog filter frequencies and standard operating temperature range.

Basic Model Number	Form Factor
PC104P-24DSI6LN	**PC104-*Plus (Native)****
PMC-24DSI6LN	PMC
PCI-24DSI6LN	PCI, short length
cPCI-24DSI6LN	cPCI, 3U

* Contact factory for availability of other form factors.

Optional Parameter	Value	Specify Option As:
Number of Input Channels	4 Channels	A = 4
	6 Channels	A = 6
Input Ranges	±10V (Standard input range)	B = 10 (or blank)
	±5V	B = 5
	±2.5V	B = 2.5
Image Filter Frequency	Standard 270kHz	C = SF (or Blank)
	Custom Frequencies *:	C = CFx
Operating Temperature	Standard Range: 0 to +65 Deg-C	D = S (or Blank)
	Extended Range: -40 to +80 Deg-C	D = ET

* +/-12%, 1kHz-300kHz; 22%, 100Hz-1kHz. Contact factory for availability of specific frequencies.

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SYSTEM I/O CONNECTIONS

I/O CONNECTOR PIN ASSIGNMENTS

ROW-A		ROW-B	
PIN	**FUNCTION**	**PIN**	**FUNCTION**
1	INPUT RETURN	1	INPUT RETURN
2	INPUT RETURN	2	INPUT RETURN
3	**INP CHAN 00 LO**	3	INPUT RETURN
4	**INP CHAN 00 HI**	4	INPUT RETURN
5	INPUT RETURN	5	INPUT RETURN
6	INPUT RETURN	6	INPUT RETURN
7	**INP CHAN 01 LO**	7	INPUT RETURN
8	**INP CHAN 01 HI**	8	INPUT RETURN
9	INPUT RETURN	9	INPUT RETURN
10	INPUT RETURN	10	INPUT RETURN
11	**INP CHAN 02 LO**	11	INPUT RETURN
12	**INP CHAN 02 HI**	12	INPUT RETURN
13	INPUT RETURN	13	INPUT RETURN
14	INPUT RETURN	14	INPUT RETURN
15	**INP CHAN 03 LO**	15	INPUT RETURN
16	**INP CHAN 03 HI**	16	INPUT RETURN
17	INPUT RETURN	17	INPUT RETURN
18	INPUT RETURN	18	INPUT RETURN
19	**INP CHAN 04 LO**	19	INPUT RETURN
20	**INP CHAN 04 HI**	20	INPUT RETURN
21	INPUT RETURN	21	INPUT RETURN
22	INPUT RETURN	22	INPUT RETURN
23	**INP CHAN 05 LO**	23	INPUT RETURN
24	**INP CHAN 05 HI**	24	INPUT RETURN
25	INPUT RETURN	25	INPUT RETURN
26	INPUT RETURN	26	INPUT RETURN
27	DIGITAL RETURN	27	DIGITAL RETURN
28	DIGITAL RETURN	28	DIGITAL RETURN
29	**EXT CLK INP LO ****	29	**EXT CLK OUT LO**
30	**EXT CLK INP HI ***	30	**EXT CLK OUT HI ***
31	DIGITAL RETURN	31	DIGITAL RETURN
32	DIGITAL RETURN	32	DIGITAL RETURN
33	**EXT SYNC INP LO ****	33	**EXT SYNC OUT LO**
34	**EXT SYNC INP HI ***	34	**EXT SYNC OUT HI ***

* TTL signal levels when TTL sync I/O is selected.
** 'LO' digital inputs must be open (unconnected) in TTL mode.

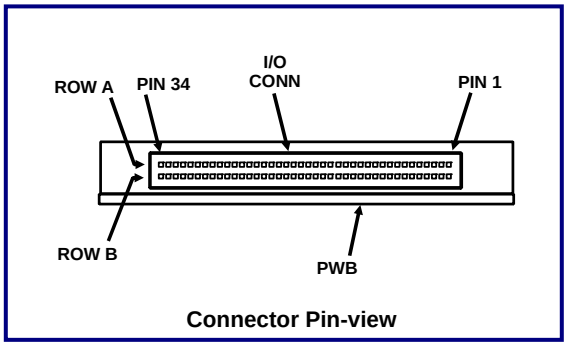

Figure 2. System I/O Connector

System Cable Mating Connector:
68-pin 0.050" Subminiature connector: with metal shield: AMP #749621-7 or equivalent.

I/O Connector Installed on Board (Ref)**:**
Amp # 787170-7

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