

General Standards Corporation

High Performance Bus Interface Solutions

PC104P-16AO20

20-Channel 16-Bit High-Speed Analog Output PC104-Plus Board
With 440,000 Samples per Second per Channel, and Simultaneous Clocking

Features Include:

- 20 Precision High-Speed Analog Output Channels;
- 16-Bit Resolution; D/A Converter per Channel
- Data Rates to 440K Samples per Second per Channel; 8.8 MSPS Aggregate Rate
- Output Ranges of $\pm 10V$, $\pm 5V$ or $\pm 2.5V$
- Output Clocking Mode Selectable as Simultaneous or Sequential
- 256K-Sample Output Data Buffer
- Analog Output FIFO Buffer Software-Configurable as Open or Circular
- Continuous and Burst (One-Shot) Output Modes Support Seamless Waveform Sequencing
- Data Rate Controlled by Adjustable Internal Clock, or by Externally Supplied Clock
- Supports Real-Time Rate Adjustments
- Hardware I/O Supports Multiboard Synchronization
- Software-Selectable Differential Clock I/O for Synchronizing Sigma-Delta A/D Boards
- On-Demand Autocalibration of all Channels
- Remote Ground Sensing
- High Accuracy; 0.017% FSR max error on $\pm 10V$ Range, INL = 0.007%
- Fast Settling; 5 μs to 0.1%; 8 μs to 0.01%; with No-filter Option
- VxWorks™ and NT Drivers™ Available

Applications Include:

- | | | |
|----------------------------|----------------------|----------------------|
| ✓ Precision Voltage Source | ✓ Acoustic Research | ✓ Waveform Synthesis |
| ✓ Industrial Robotics | ✓ Process Monitoring | ✓ Audio Synthesis |

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Overview:

The PC104P-16AO20 board contains twenty 16-bit D/A converters (DAC's), and all supporting functions necessary for adding precision high-speed analog output capability to a PC104-*Plus* application. The board is functionally compatible with the IEEE PCI local bus specification Revision 2.3, and supports the "plug-n-play" initialization concept. Unique FIFO buffer controls support the seamless sequencing of successive waveforms. In less demanding applications, the outputs can be updated individually. An optional clock output for synchronizing Sigma-Delta ADC boards is available.

A PCI interface adapter provides the interface between the controlling PCI bus and the internal local controller (Figure 1). Twenty output channels are controlled through an analog output FIFO buffer, and can be updated either simultaneously or sequentially. The output sample rate can be controlled by an internal rate generator or by an external clock. The local controller manages all input/output configuration and data manipulation functions, including autocalibration. Analog output levels are initialized to zero (midrange). Multiboard synchronization is supported.

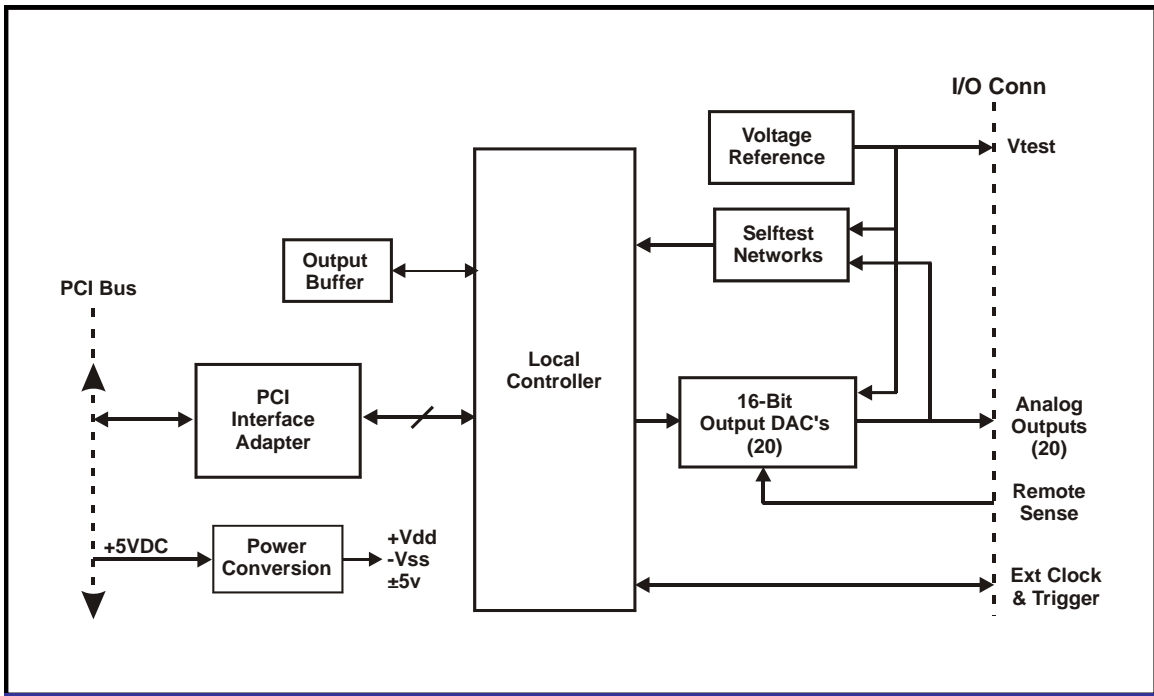


Figure 1. PC104P-16AO20 Board; Functional Organization

This product is designed for minimum off-line maintenance. On-demand autocalibration eliminates the need for disconnecting or removing the module from the system for calibration. All analog input and output system connections are made through a single 50-pin I/O connector. Power requirements consist of +5 VDC, in compliance with the PCI specification, and operation over the specified temperature range is achieved with conventional convection cooling.

Electrical Specifications

(At +25 °C, with specified operating conditions)

Analog Output Channels

Output Characteristics:

| | |
|--|--|
| Configuration: | Twenty single-ended analog output channels, with dedicated 16-Bit DAC per channel; Optional 12-channel and 6-Channel configurations available. |
| Voltage Ranges: | Factory configured as ± 10 Volts, ± 5 Volts or ± 2.5 Volts |
| Output Resistance: | 1.0 Ohm maximum |
| Output protection: | Withstands sustained short-circuiting to ground without damage |
| Load Current: | ± 3 ma maximum; ± 2 ma recommended for minimum crosstalk and line loss |
| Load Capacitance: | Stable with zero to 2000 pF shunt capacitance |
| Settling Time: (Typical, Fullscale) | No Filter : 5 us to 0.1%, 8 us to 0.01% 100 kHz Filter: 14 us to 0.1%, 18 us to 0.01% 10 kHz Filter: 100 us to 0.1%, 140 us to 0.01% |
| Noise: | No Filter: 1.3 mVRMS, 10Hz-10MHz 10 kHz Filter: 0.4 mVRMS, 10Hz-10MHz |
| Glitch Impulse: | ± 2.5 V Range: 3 nV-Sec max. ± 5 V Range: 5 nV-Sec ± 10 V Range: 8 nV-Sec |
| Remote Sensing: | Single input pin compensates for ground potential at load. Maximum range ± 1.0 Volt. Correction ± 1 percent. Enabled or disabled through application software. |

Transfer Characteristics:

| Resolution: | 16 Bits (0.0015 percent of FSR) | | | | | | | | | | | | |
|--------------------------------------|---|--------------------------|-------------------|--------------------------|------------|--------------|--------------|-----------|--------------|--------------|-------------|--------------|--------------|
| Sample Clocking Rate: | Internal Rate Clock: 460 to 440,000 samples per second per channel External Rate Clock: 0 to 440,000 samples per second per channel | | | | | | | | | | | | |
| DC Accuracy: (Max error, no-load) | <table><thead><tr><th>Range</th><th>Midscale Accuracy</th><th>\pmFullscale Accuracy</th></tr></thead><tbody><tr><td>± 10V</td><td>± 2.4mv</td><td>± 3.3mv</td></tr><tr><td>± 5V</td><td>± 1.7mv</td><td>± 2.2mv</td></tr><tr><td>± 2.5V</td><td>± 1.4mv</td><td>± 1.6mv</td></tr></tbody></table> | Range | Midscale Accuracy | \pm Fullscale Accuracy | ± 10 V | ± 2.4 mv | ± 3.3 mv | ± 5 V | ± 1.7 mv | ± 2.2 mv | ± 2.5 V | ± 1.4 mv | ± 1.6 mv |
| Range | Midscale Accuracy | \pm Fullscale Accuracy | | | | | | | | | | | |
| ± 10 V | ± 2.4 mv | ± 3.3 mv | | | | | | | | | | | |
| ± 5 V | ± 1.7 mv | ± 2.2 mv | | | | | | | | | | | |
| ± 2.5 V | ± 1.4 mv | ± 1.6 mv | | | | | | | | | | | |
| Bandwidth: (Single-pole lowpass) | 10 kHz, 100 kHz and No-Filter (300 kHz) options, Typical at -3dB. | | | | | | | | | | | | |
| Crosstalk Rejection: | 80 dB minimum, DC-10 kHz | | | | | | | | | | | | |
| Integral Nonlinearity: | ± 0.007 percent of FSR, maximum | | | | | | | | | | | | |
| Differential Nonlinearity: | ± 0.003 percent of FSR, maximum | | | | | | | | | | | | |

Operating Modes and Control

| | |
|-------------------------------------|--|
| DAC Clocking Source: | Internal rate generator, external hardware input, or software clock. |
| Multiboard Clocking Configurations: | To support the simultaneous clocking of DAC outputs on multiple boards, the 16AO20 can be software-designated as either a clock initiator or a clock target. Initiators provide an output clock for target boards, each of which retransmits the clock signal to subsequent boards connected in a daisy-chain configuration. |
| Burst Trigger: | Software control bit, or external TTL/LVDS trigger input (Same as clock I/O option). Burst triggering also can be obtained from an external source. |
| Update Mode: | Simultaneous or channel-sequential output updating |
| Active Buffer Size: | From 8 output values to 256K-values, in 2:1 steps, software-selectable. |
| Buffer Mode: | Selected as Circular for periodic waveforms, or as Open for one-shot functions |
| Data Format: | Software selected as Offset Binary or Two's complement |

PCI Compatibility

Conforms to PCI Specification 2.3, with 33 MHz, D32 read/write transactions.
Multifunction interrupt.
Supports DMA transfers as bus master.

Power, Mechanical and Environmental Specifications

Power Requirements:

+5VDC \pm 0.25 VDC at 1.5Amps maximum, 1.1 Amp typical. Outputs fully loaded.
Power Dissipation: 7.5 Watts max; 5.5 Watts typical

Mechanical Characteristics:

Height: 23.3 mm (0.92 in)
Width: 94.0 mm (3.78 in)
Depth: 95.9 mm (3.70 in)

Power, Mechanical and Environmental Specifications (Continued)

Environmental Requirements:

| | |
|-----------------------------|--|
| Ambient Temperature Range : | Operating: 0 to +65 degrees Celsius inlet air Storage: -40 to +85 degrees Celsius |
| Relative Humidity: | Operating: 0 to 80%, non-condensing Storage: 0 to 95%, non-condensing |
| Altitude: | Operation to 10,000 ft. |
| Cooling: | Conventional convection cooling. |

Ordering Information

Specify the basic product model number (PC104P-16AO20), followed by an option suffix "-ABC", as indicated below. For example, model number PC104P-16AO20-102 describes a board with a ± 5 Volt output range, no output filter, and 20 output channels.

| Optional Parameter | Value | Specify Option As: |
|--|-----------------------|--------------------|
| Output Range: | ± 2.5 Volts | A = 0 |
| | ± 5 Volts | A = 1 |
| | ± 10 Volts | A = 2 |
| Output Lowpass Filter: (Single-pole) | No output Filter | B = 0 |
| | 10 kHz Output Filter | B = 1 |
| | 100 kHz Output Filter | B = 2 |
| Number of Output Channels: | 6 Channels | C = 0 |
| | 12 Channels | C = 1 |
| | 20 Channels | C = 2 |

System I/O Connections

Table 1. System Connector Pin Functions

| PIN | SIGNAL | PIN | SIGNAL |
|-----|-------------------|-----|---------------------|
| 1 | OUTPUT RETURN | 26 | REMOTE GROUND SENSE |
| 2 | OUTPUT CHANNEL 00 | 27 | OUTPUT CHANNEL 12 |
| 3 | OUTPUT RETURN | 28 | OUTPUT RETURN |
| 4 | OUTPUT CHANNEL 01 | 29 | OUTPUT CHANNEL 13 |
| 5 | OUTPUT RETURN | 30 | OUTPUT RETURN |
| 6 | OUTPUT CHANNEL 02 | 31 | OUTPUT CHANNEL 14 |
| 7 | OUTPUT RETURN | 32 | OUTPUT RETURN |
| 8 | OUTPUT CHANNEL 03 | 33 | OUTPUT CHANNEL 15 |
| 9 | OUTPUT RETURN | 34 | OUTPUT RETURN |
| 10 | OUTPUT CHANNEL 04 | 35 | OUTPUT CHANNEL 16 |
| 11 | OUTPUT RETURN | 36 | OUTPUT CHANNEL 17 |
| 12 | OUTPUT CHANNEL 05 | 37 | OUTPUT RETURN |
| 13 | OUTPUT RETURN | 38 | OUTPUT CHANNEL 18 |
| 14 | OUTPUT CHANNEL 06 | 39 | OUTPUT CHANNEL 19 |
| 15 | OUTPUT RETURN | 40 | VTEST RETURN |
| 16 | OUTPUT CHANNEL 07 | 41 | VTEST OUT |
| 17 | OUTPUT RETURN | 42 | DIGITAL RETURN |
| 18 | OUTPUT CHANNEL 08 | 43 | TRIGGER IN HI * |
| 19 | OUTPUT RETURN | 44 | TRIGGER IN LO * |
| 20 | OUTPUT CHANNEL 09 | 45 | TRIGGER OUT HI * |
| 21 | OUTPUT RETURN | 46 | TRIGGER OUT LO * |
| 22 | OUTPUT CHANNEL 10 | 47 | DAC CLOCK OUT HI * |
| 23 | OUTPUT RETURN | 48 | DAC CLOCK OUT LO * |
| 24 | OUTPUT CHANNEL 11 | 49 | CLOCK I/O HI ** |
| 25 | OUTPUT RETURN | 50 | CLOCK I/O LO ** |

* Software-selectable as LVDS differential pairs. In TTL mode, 'LO' inputs should be connected to digital return.

** Bidirectional synchronization signal.

Channels available in 6-Channel and 12-Channel configurations:

6-Channel Board: Channels 00-05,

12-Channel board: Channels 00-11.

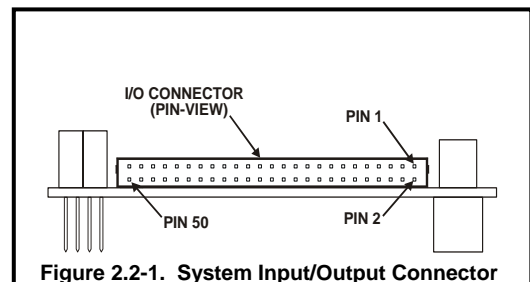


Figure 2.2-1. System Input/Output Connector

**System Mating Connector:
Polarized 50-Pin socket connector:
AMP #1-746288-0,
with strain-relief #499252-4.**

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