General Standards Corporation

High Performance Bus Interface Solutions

CCVPX-16AO16C

16-Channel 16-Bit High-Speed Conduction-Cooled 3U VPX Analog Output Board

With 450,000 Samples per Second per Channel

Features

- **16 precision 16-Bit high-speed analog output channels; D/A converter per channel**
- **Balanced 3-Wire differential outputs, or optional 2-wire single-ended outputs with remote ground sensing**
- **Front-panel system access**
- **Standard conduction-cooled 3U VPX form Factor**
- Data rates to 450K samples per second per channel
- Software-selectable output ranges of ±10V, ±5V, ±2.5V or ±1.25V; optional ±20V,±10V, ±5V differential output ranges
- 256K-Sample output data FIFO buffer; configurable as open or circular
- Conforms to PCI Express Specification revision 1.0a; x1 link operating at 2.5Gbps
- Two DMA channels available for buffer access in either block-mode or demand-Mode
- Simultaneous or channel-sequential output clocking
- Multiboard synchronization supported
- Continuous and burst (one-shot) output modes support seamless waveform sequencing
- Data rate controlled internally or externally
- Software-selectable differential clock I/O for synchronizing GSC sigma-delta A/D products
- Accuracy supported by on-demand autocalibration

Typical Applications

✓ Precision Voltage Source	✓ Acoustic Research	✓ Waveform Synthesis
✓ Audio Synthesis	✓ Process Control	✓ Industrial Robotics

--- PRELIMINARY ---

REV: 032417

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Functional Description

The CCVPX-16AO16C contains sixteen 16-bit D/A converters (DAC's), and all supporting functions necessary for adding precision high-speed differential or single-ended analog output capability to a 3U VPX application. Output ranges are software-selectable as ±10 Volts, ±5 Volts or ±2.5 Volts. . Buffer operation can be selected as either Open for data streaming, or as Closed (circular) for periodic waveform generation. Unique FIFO buffer controls support the seamless sequencing of successive waveforms through a single buffer port. In less demanding applications, the outputs can be updated individually. Hardware clock I/O permits synchronization with a variety of GSC products, including Sigma-Delta ADC boards.

A PCI Express adapter provides the interface between the control bus and the internal local controller (Figure 1). Sixteen output channels are controlled through an analog output FIFO buffer, and can be updated either simultaneously or sequentially. The output sample rate can be controlled by an internal rate generator or by an external clock. The local controller manages all input/output configuration and data manipulation functions, including autocalibration. Analog output levels are initialized to zero (midrange). Multiboard synchronization is supported.

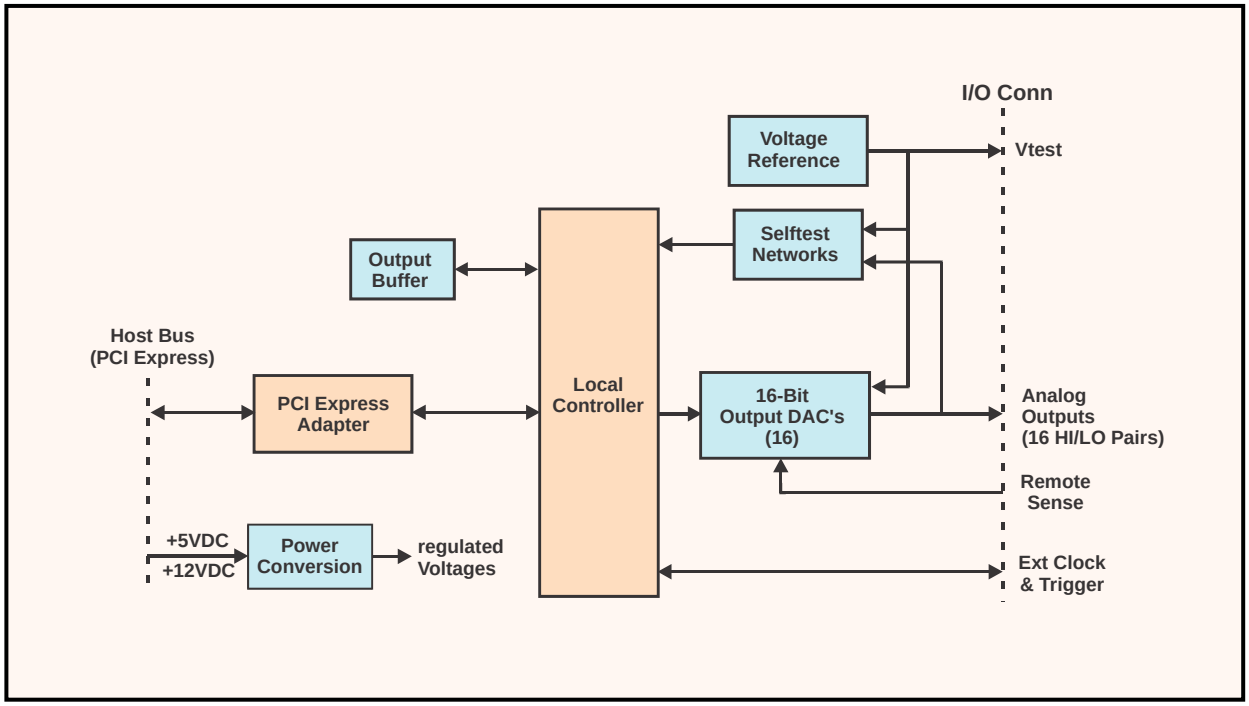

Figure 1. CCVPX-16AO16C Board; Functional Organization

This product conforms to the VPX baseline standard ANSI/VITA 46.0-2007 (R2013). System connections are made at the front panel through a high-density front-panel I/O connector. Power requirements consist of +12VDC and +5VDC in compliance with the VPX specification, and operation over the specified temperature range is achieved with standard conduction cooling.

Performance Specifications

At +25 ^{O}C, with specified operating conditions.

Output Characteristics:

Configuration:	Sixteen 3-wire balanced differential analog output channels, with a dedicated 16-Bit DAC per channel. Each 3-Wire output consists of complementary 'HI' and 'LO' signal lines, with 'output return' as the center (balance) reference. All output returns are electrically common internally. Optional 12-channel and 8-Channel configurations are available, as well as 2-wire single-ended analog outputs with remote ground sensing.
Voltage Ranges:	Software-selected as ±10V, ±5V, ±2.5Vor ±1.25V, Line-to-Line for differential configuration. Line-to-Ground with Single-Ended option (Output-HI relative to output return). Optional High-Level (HL) ±20V, ±10V, ±5V differential outputs . See Ordering information.
Output Resistance:	1.0 Ohm maximum
Protection:	Withstands sustained short-circuiting to ground without damage
Load Current:	±3 ma maximum on all channels simultaneously; ±2 ma recommended for minimal crosstalk and line loss. (10mA maximum on individual channels, if total load on all outputs does not exceed 50mA).
Load Capacitance:	Stable with zero to 10,000 pF shunt capacitance; all ranges, all loads.
Settling Time (Typical):	No Filter : 5 us to 0.1%, 8 us to 0.01% 100 kHz Filter: 14 us to 0.1%, 18 us to 0.01% 10 kHz Filter: 100 us to 0.1%, 140 us to 0.01%
Noise:	No Filter: 1.3 mVRMS, 10Hz-10MHz 10 kHz Filter: 0.4 mVRMS, 10Hz-10MHz
Glitch Impulse:	±2.5V Range: 3 nV-Sec max.. ±10V Range: 8 nV-Sec
Remote Sensing: (Single-ended outputs)	Single input pin compensates for ground potential at load. Max range ±1.0V. Enabled or disabled through application software. Correction ±1 percent. Input resistance: 15K typical.

Transfer Characteristics:

Resolution:	16 Bits (0.0015 percent of FSR)
Sample Clocking Rate:	Internal Rate Clock: 172 to 450,000 samples per second per channel External Rate Clock: 0 to 450,000 samples per second per channel

DC Accuracy, Line-Line: (Max error, no-load)

Range	Midscale Accuracy	±Fullscale Accuracy
±20V	±6.2mv	±15mv
±10V	±2.4mv	±3.3mv
±5V	±1.7mv	±2.2mv
±2.5V	±1.4mv	±1.6mv
±1.25V	±1.2mv	±1.4mv

Output Balance:	10mV maximum HI/LO unbalance.
Bandwidth	10 kHz, 100 kHz and No-Filter (>300 kHz) options, Typical at -3dB. (Single-pole lowpass)
Crosstalk Rejection:	80 dB minimum, DC-50 kHz
Integral Nonlinearity:	±0.007 percent of FSR, maximum
Differential Nonlinearity:	±0.003 percent of FSR, maximum

Operating Modes and Controls:

DAC Clocking Source:	Internal rate generator, external hardware input, or software clock. The internal rate generator is selectable as either (a) a division of the 64MHz master clock oscillator, or (b) a software-controlled VCO with 0.2% setting resolution, and ±0.02% accuracy.
Multiboard Clocking Configurations:	To support the simultaneous clocking of DAC outputs on multiple boards, the 16AO16 can be software-designated as either a clock initiator or a clock target. Initiators provide an output clock for target boards, each of which can retransmit the clock signal to subsequent boards connected in a daisy-chain configuration.
Burst Trigger:	Software control bit, or external TTL/LVDS trigger input (Same as clock I/O option). Burst triggering also can be obtained from an external source.
Update Mode:	Simultaneous or channel-sequential output updating
Active Buffer Size:	From 8 output values to 256K-values, in 2:1 steps, software-selectable.
Buffer Mode:	Selected as Circular for periodic waveforms, or as Open for one-shot functions
Data Format:	Software selected as Offset Binary or Two's complement

Bus Compatibility

Conforms to VPX VITA 46.0.
Also conforms to PCI Express Specification revision 1.0a; x1 Link operating at 2.5Gbps.
DMA transfers as bus master with two DMA channels.

Power Requirements

+5VDC ±0.2 VDC, 1.0 Amps typical, 1.2 Amp maximum.
+12VDC ±0.4 VDC, 0.5 Amps typical, 0.6 Amps maximum
Total power consumption: 11 Watts typical, 13 Watts maximum.

Mechanical Characteristics

Height: 18.8mm (0.74 in)
Depth: 170.6 mm (6.717 in)
Width: 100.0 mm (3.937 in)
Shield: Side-1 is protected by an EMI shield.
Thermal transfer rails are provided for conduction cooling.

Environmental Specifications

Ambient Temperature Range:	Operating: 0 to +80 Degrees Celsius inlet air Storage: -40 to +85 Degrees Celsius
Relative Humidity:	Operating and Storage: 0 to 95%, non-condensing
Altitude:	Operation to 10,000 ft.
Cooling:	Standard conduction cooling thermal interfaces.

Ordering Information

Specify the basic model number, followed by an option suffix "-A-B-C-D", as indicated below. For example, model number CCVPX-16AO16C-12-F10-DF-0 describes a 3U VPX module with 12 differential output channels, 10 kHz output filters and no custom features (standard output levels).

Optional Parameter	Value	Specify Option As:
Number of Output Channels:	**8 Channels**	**A = 8**
	12 Channels	**A= 12**
	16 Channels	**A = 16**
Output Lowpass Filter: (Single-pole)	**No output Filters (>300kHz)**	**B = F0**
	10 kHz Output Filters	**B = F10**
	100 kHz Output Filters	**B = F100**
Output Configuration: *	**Differential**	**C = DF**
	Single-Ended	**C = SE**
Custom Feature:	**High-Level Differential Outputs (±20V,±10V, ±5V differential output ranges). Requires Option-C = DF**	**D = HL**
	No custom features	**0**

* Differential outputs are essentially immune to ground potential differences, and do not implement compensation for ground potential at the load. Single-ended outputs are affected by remote ground potentials however, and are supported with a Remote Ground Sense input to compensate for potential differences between the CCVPX-16AO16C outputs and the load.

System Interface Connector

Table 1. System I/O Connector Pin Functions

Pin	Signal	Pin	Signal
43	OUTPUT RETURN	---	
42	OUTPUT 00 LO	85	OUTPUT 00 HI
41	OUTPUT RETURN	84	OUTPUT RETURN
40	OUTPUT 01 LO	83	OUTPUT 01 HI
39	OUTPUT RETURN	82	OUTPUT RETURN
38	OUTPUT 02 LO	81	OUTPUT 02 HI
37	OUTPUT RETURN	80	OUTPUT RETURN
36	OUTPUT 03 LO	79	OUTPUT 03 HI
35	OUTPUT RETURN	78	OUTPUT RETURN
34	OUTPUT 04 LO	77	OUTPUT 04 HI
33	OUTPUT RETURN	76	OUTPUT RETURN
32	OUTPUT 05 LO	75	OUTPUT 05 HI
31	OUTPUT RETURN	74	OUTPUT RETURN
30	OUTPUT 06 LO	73	OUTPUT 06 HI
29	OUTPUT RETURN	72	OUTPUT RETURN
28	OUTPUT 07 LO	71	OUTPUT 07 HI
27	OUTPUT RETURN	70	OUTPUT RETURN
26	OUTPUT 08 LO	69	OUTPUT 08 HI
25	OUTPUT RETURN	68	OUTPUT RETURN
24	OUTPUT 09 LO	67	OUTPUT 09 HI
23	OUTPUT RETURN	66	OUTPUT RETURN
22	OUTPUT 10 LO	65	OUTPUT 10 HI
21	OUTPUT RETURN	64	OUTPUT RETURN
20	OUTPUT 11 LO	63	OUTPUT 11 HI
19	OUTPUT RETURN	62	OUTPUT RETURN
18	OUTPUT 12 LO	61	OUTPUT 12 HI
17	OUTPUT RETURN	60	OUTPUT RETURN
16	OUTPUT 13 LO	59	OUTPUT 13 HI
15	OUTPUT RETURN	58	OUTPUT RETURN
14	OUTPUT 14 LO	57	OUTPUT 14 HI
13	OUTPUT RETURN	56	OUTPUT RETURN
12	OUTPUT 15 LO	55	OUTPUT 15 HI
11	OUTPUT RETURN	54	REM GND SENSE
10	VTEST RETURN	53	VTEST OUT
9	DIGITAL RETURN	52	DIGITAL RETURN
8	TRIG IN LO*	51	TRIG IN HI *
7	DIGITAL RETURN	50	DIGITAL RETURN
6	TRIG OUT LO*	49	TRIG OUT HI *
5	DIGITAL RETURN	48	DIGITAL RETURN
4	DAC CLK OUT LO *	47	DAC CLK OUT HI *
3	DIGITAL RETURN	46	DIGITAL RETURN
2	CLOCK OUT LO **	45	CLOCK OUT HI *
1	DIGITAL RETURN	44	DIGITAL RETURN

The differential analog output configuration is shown. For optional single-ended outputs, OUTPUT XX HI is an output, and OUTPUT XX LO should be left disconnected.

* Software-selectable as LVDS differential pairs. In TTL mode, 'HI' pins are signal pins, and 'LO' inputs should be connected to digital return.

** Bidirectional synchronization signal.

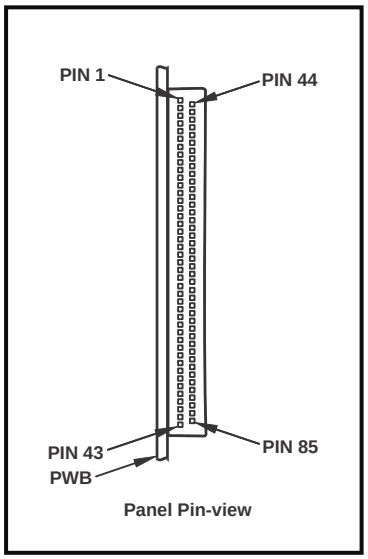

Figure 2. System I/O Connector

System I/O Mating Connector:
Omnetics # MNPO-85-DD-N-EJS-C, dual-row, straight tail.
(Assembled cables available)