

General Standards Corporation

High Performance Bus Interface Solutions

CCPMC-24DSI8R

8-Channel 24-Bit Delta-Sigma Conduction Cooled PMC

Analog Input Board

With 200 KSPS Sample Rate per Channel

FEATURES:

- ◆ 8 Differential 24-Bit Analog Input Channels
- ◆ Delta-Sigma Converter per Channel, with Linear Phase Digital Antialias Filtering
- ◆ Sample rates from 2 KSPS to 200 KSPS per Channel
- ◆ Software-Selectable Input Ranges: $\pm 2.5V$, $\pm 5V$, $\pm 10V$
- ◆ 256 K-sample FIFO Buffer
- ◆ Synchronous or Independent ADC Clocking
- ◆ Internal Sample Rate Generators
- ◆ Hardware Sync and Clock I/O for Multiboard Synchronization
- ◆ Supports GPS Synchronization to a 1PPS Input
- ◆ Low Phase Skew; Typically Less than 55ns with $F_{sig} < 0.35 * F_{samp}$
- ◆ DMA Engine Supports both Block-Mode and Demand-Mode Transfers
- ◆ Low Power Consumption. 6 Watts Typical. Only +5VDC Required from PCI bus.
- ◆ 100dB Dynamic Range to 100KSPS; 93 dB SINAD
- ◆ On-demand Autocalibration Ensures DC Precision as well as AC performance
- ◆ Integrated DC/DC Conversion and Regulation of Precision Internal Supply Voltages
- ◆ Conforms to PCI Bus Specification, Revision 2.3, with Universal Signaling
- ◆ Triggered Acquisition feature supports external acquisition triggering

TYPICAL APPLICATIONS:

- | | | |
|-----------------|-----------------------|---------------------------|
| ✓ Sonar Arrays | ✓ Voltage Acquisition | ✓ Phase Comparison |
| ✓ Analog Inputs | ✓ Acoustic Research | ✓ Audio Waveform Analysis |

REV: 110912

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Overview:

The 8-channel PMC-24DSI8R analog input board provides high-density 24-bit analog input resources on a standard single-width Conduction Cooled PMC board. Optimized for flexibility and performance, the board is ideal for a wide variety of applications, ranging from simple precision voltage measurements, to the analysis of complex audio signals and waveforms.

Functional Description:

Each of 8 analog input channels contains a lowpass image filter, and a delta-sigma A/D converter that provides digital antialias filtering. An internal voltage reference can be applied to all channels to support self-test operations and autocalibration. Gain and offset trimming is performed by applying correction values that are determined during on-demand autocalibration. A linear-phase digital antialiasing filter rejects out-of-band signals, and a lowpass analog filter reject those interference signals that fall within the harmonic images of the digital filter.

An internal sample-rate generator is adjustable over a 2:1 frequency range, and is divided down within the local controller to provide individual channel sample rates from 2KSPS to 200KSPS. Conversion data from all active channels is transferred to the PCI bus through a 256K-sample data buffer that is supported by two DMA channels. Multiple channels can be synchronized to perform sampling in "lockstep", either by a software command, or by external hardware sync and clock input signals.

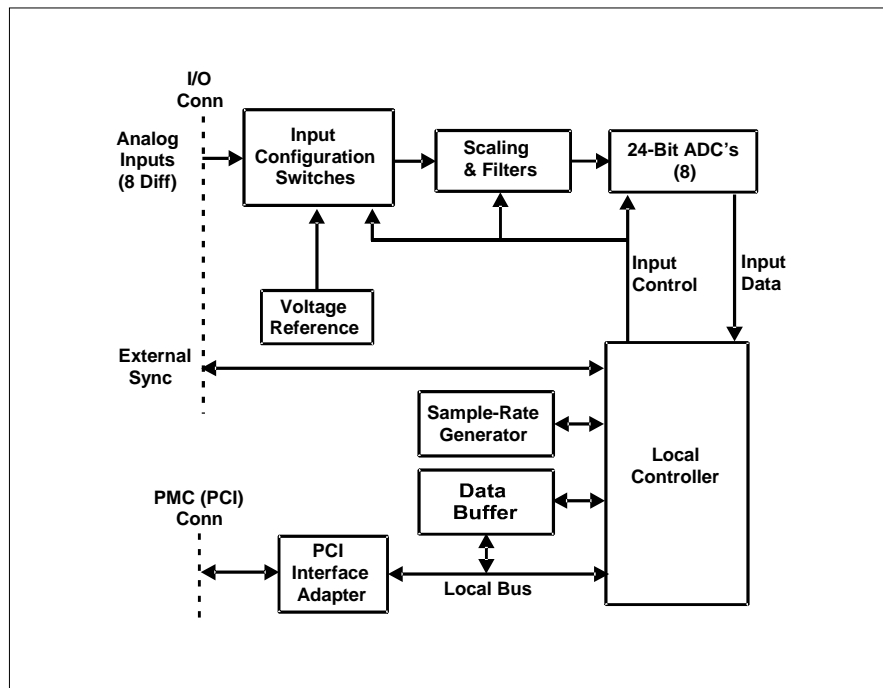


Figure 1. PMC-24DSI12; Functional Organization

This product is functionally compatible with the IEEE PCI local bus specification Revision 2.3. System input/output connections are made through the rear PMC 64-pin I/O connector. Power requirements consist of +5 VDC, in compliance with the PCI specification, and operation over the specified temperature range is achieved by conduction cooling by means of a CCPMC host board.

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ELECTRICAL SPECIFICATIONS

At +25 °C, with specified operating conditions.

Input Characteristics:

Configuration:	8 differential input channels. 4-channel configurations available.
Voltage Range:	Software Configurable as ± 2.5 Volts, ± 5 Volts or ± 10 Volts
Input Impedance:	1.0 Megohm typical, in parallel with 20 pF. 2.0 Megohms line-line.
Common Mode Rejection:	80dB to 1kHz; 60dB to 50kHz.; typical
Common Mode Range:	± 11 Volts with zero normal-mode input
Overvoltage Protection:	± 25 -Volt transients with power applied; ± 45 Volts with power removed

Transfer Characteristics:

Quantizing Resolution:	24 Bits																									
Sample Rate:	2,000 to 200,000 samples per second per channel																									
Oversampling Factor:	2-50ksps: x128; 50-100ksps: x64; 100-200ksps: x32																									
DC Accuracy: (Mean composite error after autocalibration)	<table><thead><tr><th>Input Range</th><th>Midrange (Zero) Accuracy</th><th colspan="3">Gain Accuracy at Fsamp</th></tr><tr><th></th><th></th><th>2-4ksps</th><th>4-15ksps</th><th>15-200ksps</th></tr></thead><tbody><tr><td>$\pm 10V$</td><td>$\pm 0.5mv$</td><td>$\pm 0.9\%$</td><td>$\pm 0.3\%$</td><td>$\pm 0.1\%$</td></tr><tr><td>$\pm 5V$</td><td>$\pm 0.3mv$</td><td>$\pm 0.9\%$</td><td>$\pm 0.3\%$</td><td>$\pm 0.1\%$</td></tr><tr><td>$\pm 2.5V$</td><td>$\pm 0.1mv$</td><td>$\pm 0.9\%$</td><td>$\pm 0.3\%$</td><td>$\pm 0.1\%$</td></tr></tbody></table>	Input Range	Midrange (Zero) Accuracy	Gain Accuracy at Fsamp					2-4ksps	4-15ksps	15-200ksps	$\pm 10V$	$\pm 0.5mv$	$\pm 0.9\%$	$\pm 0.3\%$	$\pm 0.1\%$	$\pm 5V$	$\pm 0.3mv$	$\pm 0.9\%$	$\pm 0.3\%$	$\pm 0.1\%$	$\pm 2.5V$	$\pm 0.1mv$	$\pm 0.9\%$	$\pm 0.3\%$	$\pm 0.1\%$
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Bandwidth (-3dB)	DC to typically 49 percent of selected sample rate for sample rates to 100KSPS, or to 35 percent of sample rate from 100kSPS to 200KSPS. Typically DC to 70 kHz overall. 0.1dB to 0.45Fsamp; 2-100KSPS; 0.24Fsamp 100-200KSPS.																									
Passband Ripple:	± 0.06 dB maximum																									
Phase Skew:	Typically less than 55ns (0.1-Degree for Fsig = 5kHz), with Fsig/Fsamp < 0.35; channel-channel (board-board for multiboard configurations), excluding noise, with high-frequency image filter.																									
ADC Stopband:	<table><thead><tr><th>Sample Rate:</th><th>Threshold*</th><th>Rejection*</th></tr></thead><tbody><tr><td>2-50KSPS:</td><td>0.58 Fsamp</td><td>93dB</td></tr><tr><td>50-100KSPS:</td><td>0.68 Fsamp</td><td>90dB</td></tr><tr><td>100-200KSPS:</td><td>0.78 Fsamp</td><td>95dB</td></tr></tbody></table> <p>* Typical values. (Fsamp = sample rate)</p>	Sample Rate:	Threshold*	Rejection*	2-50KSPS:	0.58 Fsamp	93dB	50-100KSPS:	0.68 Fsamp	90dB	100-200KSPS:	0.78 Fsamp	95dB													
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Antialias Filtering:	Each ADC provides linear-phase digital antialias filtering as indicated for "ADC Stopband." A 2-pole Butterworth lowpass analog image filter in each channel provides a software-selected cutoff frequency of either 40kHz or 270kHz, and suppresses images from the digital filter. Optional alternative image filter frequencies are available, and should be selected to be well above the expected passband.																									
Dynamic Range:	100dB; typical 2 KSPS to 100 KSPS; 80dB from 100ksps to 200ksps.																									
SINAD:	(Signal to Noise-and-Distortion ratio): 93dB typical to 10 kHz input bandwidth; 85 dB typical to 50 kHz.																									
Interchannel Crosstalk:	-96dB typical to 50kHz																									

Operating Modes and Controls:

Organization:	Two analog input channel groups. All channels in each group operate at the same sample rate, which is further controlled by division of the selected rate generator frequency. Each channel group contains one-half of the channels on the board, and can operate either synchronously from a single rate generator, or independently from either of two generators.
Sample Rate Generators:	Two independent internal PLL rate generators provide sample rates from 2.0 KSPS to 200 KSPS. The frequency of each generator is controlled by the ratio of two 10-Bit integers, and setting accuracy is 25 PPM.
External Clock I/O:	An LVDS or TTL hardware input clock can be derived either from a 25.6-51.2 MHz external hardware input or from an internal rate generator. Multiple boards can be locked to a common clock by daisy-chaining the output clock from each board to the input clock of the next board in the chain. Any number of boards can be daisy-chained together, with a typical propagation delay of 10ns introduced per board. The 'star-configuration' also is supported.
Synchronization:	Sampling of multiple channel groups can be phase-synchronized through software, or each group can be synchronized to an external hardware clock input. Daisy-chained hardware sync inputs and outputs can be used to synchronize sampling among multiple boards. Synchronization to a 1PPS GPS input also is supported.
Data Format:	Software-selectable as either offset binary or two's complement. Width of the data-field is selectable as 16, 18, 20 or 24 bits.
Channel Tags:	A 4-bit channel tag is appended to each input data value.
Buffer Threshold Flag:	Asserted when the number of samples in the selected buffer exceeds the selected threshold. The threshold can be any integer from zero to 3 FFEh.
Buffer Access:	The input buffer FIFO is accessed through either of two DMA channels, with both block-mode and demand-mode transfers supported.
Triggered Acquisition	Allows an external event to initiate data acquisition.

PCI Compatibility:

Conforms to PCI Specification 2.3: D32, 33MHz, universal (3.3V/5V) signaling.
Supports "plug-n-play" initialization.
Single multifunction interrupt on INTA#.
Two-Channel DMA as bus master in block and demand modes.

Power Requirements:

+5.0 VDC \pm 0.25 VDC at 1.2 Amps typical, 1.5 Amps, maximum
Maximum Power Dissipation: Side-1: 6.5 Watts. Side 2: 1.0 Watt.

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Mechanical Characteristics:

(HxWxD): 13.5 mm (0.53 in) x 74.0 mm (2.91 in) x 143.75 mm (5.66 in)

(Mechanical dimensions are shown for the native CCPMC form factor)

Environmental Specifications:

Ambient Temperature Range:

Extended Temperature:

Operating: -40 to +80 Degrees Celsius *

Storage: -40 to +85 Degrees Celsius

* Air temperature at board surface.

Relative Humidity:

0 to 95%, non-condensing

Altitude:

Operation to 10,000 ft.

Cooling:

Conduction Cooled

Ordering Information:

Specify the basic product model number followed by an option suffix "-A-B", as indicated below. For example, model number CCPMC-24DSI8R-8-SF describes a CCPMC module with 8 input channels and standard low-pass analog filter frequencies.

Basic Model Number	Form Factor
CCPMC-24DSI8R	CCPMC (Native)

Optional Parameter	Value	Specify Option As:
Number of Input Channels	4 Channels	A = 4
	8 Channels	A = 8
Image Filter Frequencies	Standard 40kHz and 270kHz	B = SF
	Custom Frequencies: (TBD)	B = CF*

* +/-12%, 1kHz-300kHz; 22%, 100Hz-1kHz.. Contact factory for availability of specific frequencies.

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SYSTEM I/O CONNECTIONS

REAR I/O PMC CONNECTOR PIN ASSIGNMENTS

ROW-A		ROW-B	
PIN	FUNCTION	PIN	FUNCTION
1	DIGITAL RETURN	2	DIGITAL RETURN
3	EXT SYNC OUT HI *	4	EXT SYNC OUT LO
5	DIGITAL RETURN	6	DIGITAL RETURN
7	EXT CLK OUT HI *	8	EXT CLK OUT LO
9	DIGITAL RETURN	10	DIGITAL RETURN
11	EXT SYNC INP HI *	12	EXT SYNC INP LO
13	DIGITAL RETURN	14	DIGITAL RETURN
15	EXT CLK INP HI *	16	EXT CLK INP LO
17	DIGITAL RETURN	18	DIGITAL RETURN
19		20	
21		22	
23		24	
25		26	
27	INPUT RETURN	28	INPUT RETURN
29	INP CHAN 07 HI	30	INP CHAN 07 LO
31	INPUT RETURN	32	INPUT RETURN
33	INP CHAN 06 HI	34	INP CHAN 06 LO
35	INPUT RETURN	36	INPUT RETURN
37	INP CHAN 05 HI	38	INP CHAN 05 LO
39	INPUT RETURN	40	INPUT RETURN
41	INP CHAN 04 HI	42	INP CHAN 04 LO
43	INPUT RETURN	44	INPUT RETURN
45	INP CHAN 03 HI	46	INP CHAN 03 LO
47	INPUT RETURN	48	INPUT RETURN
49	INP CHAN 02 HI	50	INP CHAN 02 LO
51	INPUT RETURN	52	INPUT RETURN
53	INP CHAN 01 HI	54	INP CHAN 01 LO
55	INPUT RETURN	56	INPUT RETURN
57	INP CHAN 00 HI	58	INP CHAN 00 LO
59	INPUT RETURN	60	INPUT RETURN
61		62	
63	VTEST RETURN	64	VTEST

* TTL signal levels when TTL sync I/O is selected.

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