General Standards Corporation

High Performance Bus Interface Solutions

66-18AISS6C

18-Bit, 6-Channel, 550KSPS Analog Input Module

With Six Simultaneously Sampled Analog Inputs and 8-Bit Digital I/O Port

Available in PMC, PCI, cPCI and PC104-*Plus* and PCI Express form factors as:

PMC66-18AISS6C:	**PMC**, Single-width
PCI66-18AISS6C:	**PCI**, short length
cPCI66-18AISS6C:	**cPCI,** 3U
PC104P66-18AISS6C:	**PC104-*Plus***
PCIe-18AISS6C:	**PCI Express**

See Ordering Information for details.
Call for the availability of other form factors, such as XMC, 104-Express, CCPMC, etc.

FEATURES:

- Six differential analog inputs with dedicated 18-Bit ADC per channel
- True simultaneous sampling of all inputs to 550 KSPS per channel
- SAR architecture; No minimum sample rate
- Software-selectable input ranges [1]: ±20V (40Vpp), ±10V, or optional ±10V, ±5V ranges
- Independent 256-Ksample Input FIFO data buffer
- Low noise; >98 dB dynamic range with antialias filter disabled
- Integral antialias filter minimizes out of band components, 200kHz 5th order Chebyshev
- Hardware ADC-Clock and Burst-Trigger I/O for multiboard Operation
- Timing controlled by internal rate generators, by software clocking, or externally
- Internal on-demand autocalibration
- A *Low-Latency* option provides 32 registers that duplicate the last samples from all A/D converters
- 8-Bit Bidirectional TTL Digital I/O Port
- Two independent 24-Bit frequency dividers
- Completely software-configurable; No field jumpers
- 66 MHz 32-Bit PCI support, with universal 5V/3.3V signaling
- DMA engine minimizes bus congestion
- Single-width PMC form factor with Integral EMI shield
- Internal power conversion; Dual regulation for maximum supply integrity
- Available on adapters for alternate form factors, including PCI, cPCI and PC104-*Plus*, as well as PCI-Express, PCIX and cPCIX

[1] Input range is defined here as the entire active range of voltage differences between the two conductors in a differential HI/LO input pair. 'Equal to ±Vpk, or ±1/2*Vpp.

TYPICAL APPLICATIONS:

- ✓ High-resolution data acquisition
- ✓ Precision voltage measurement
- ✓ Transient analysis
- ✓ Event capture
- ✓ Position monitoring
- ✓ Research instrumentation

REV: 070813

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Phone: (256) 880-8787 or (800) 653-9970 FAX: (256) 880-8788 Email: Solutions@GeneralStandards.com

FUNCTIONAL DESCRIPTION

The 18AISS6C is a precision 18-Bit analog input product that provides six simultaneously sampled low-noise input channels. The inputs can be sampled at rates from zero to 550 KSPS per channel, and are supported by a 256K-Sample FIFO data buffer. Both continuous and burst clocking modes are supported, and voltage ranges are software-selectable as ±20V and ±10V differential (line-to-line), or optionally as ±10V and ±5V. Sampling and triggering rates can be derived from internal rate generators, or from external clock and trigger sources to support the synchronous operation of multiple boards. A low-latency option provides a directly accessible data register for each input channel, and eliminates the delay introduced by reading data serially from a FIFO buffer.

Input sampling employs successive-approximation (SAR) conversion, which eliminates the high latency or minimum-rate limitations of delta-sigma and pipelined conversion schemes. Single-ended inputs can be accommodated by grounding the low side of each differential input pair. A fifth-order analog lowpass filter can be inserted into the signal path under software control, and can be employed to minimize the presence of aliased out-of-band signal components.

On-demand autocalibration determines and applies error correction for all input channels, and a selftest input switching network permits board integrity to be verified by the host. Eight bidirectional digital I/O lines are programmable as inputs or outputs.

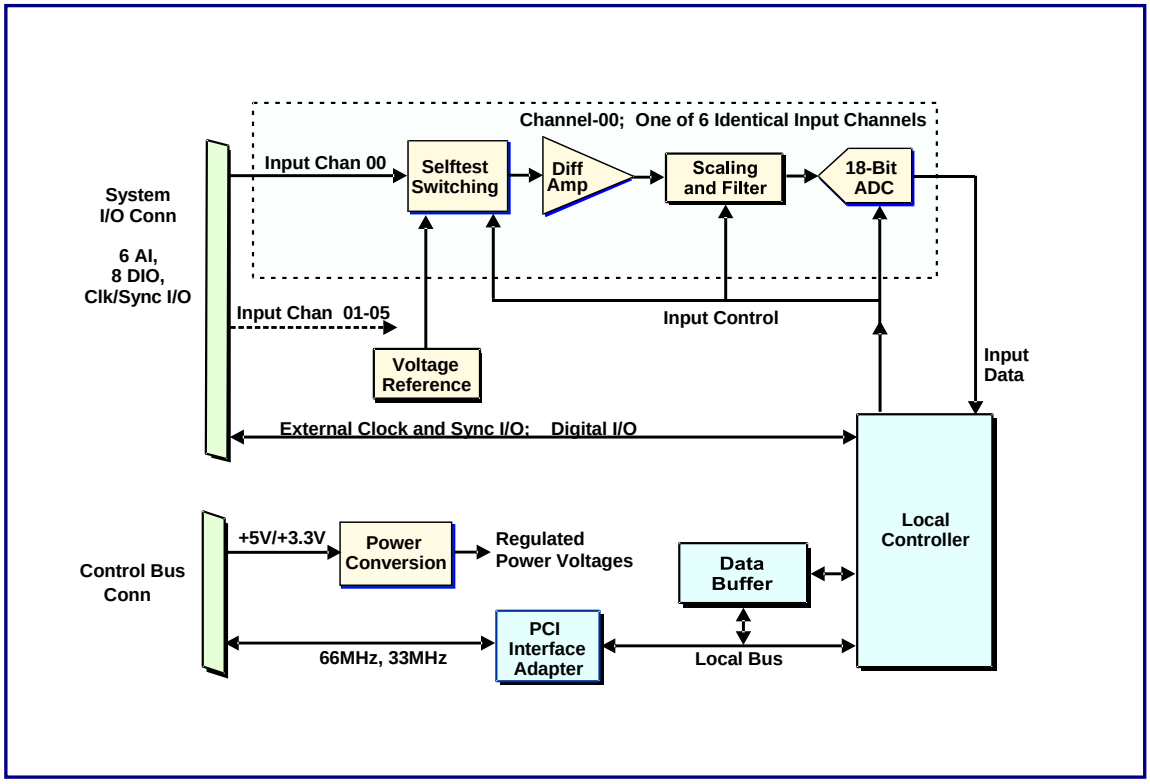

Figure 1. 18AISS6C; Functional Organization

This product complies with the IEEE PCI local bus specification Revision 2.3. System connections are made at the front panel through a high-density dual-ribbon 68-pin connector. Power requirements consist of +5VDC in compliance with the PCI specification, and analog power voltages are generated internally. Operation over the specified temperature range is achieved with conventional air cooling.

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PERFORMANCE SPECIFICATIONS

At +25 ^{O}C, with specified operating voltages

Analog Input Characteristics:

Configuration:	Six simultaneously sampled input channels with dedicated 18-Bit SAR ADC per channel. Optional 4-Channel and 2-Channel configurations available.
Voltage Ranges:	±20V or ±10V full scale for all input channels, software-selectable. Optionally selectable as ±10V or ±5V; See ordering information.
Input Impedance:	2 Megohms ±20%; typical; line-line in parallel with 80pF.
Bias Current:	2-Chan Config: 50 nanoamps typical, all ranges. 4,6-Chan Config: 100 nanoamps typical, all ranges.
Crosstalk Rejection:	90dB typical DC-50kHz. 80dB at 250kHz.
Common Mode Rejection:	65dB DC-80kHz; 50dB at 500kHz. Typical with CMV = ±11V, Vin = Zero.
Input Voltage Limits	±11V line-ground on any input for normal operation.
Overvoltage Protection:	±35V line-ground or line-to-line with power applied or removed.

Input Transfer Characteristics:

Resolution:	18 Bits (0.0004 percent of FSR)
Sample Rate:	Zero to 550KSPS per channel.
Sampling Mode::	Simultaneous; Successive-approximation conversion, all inputs active.
DC Accuracy: (Maximum composite error after autocalibration)	Range * / Midscale Accuracy / ±Fullscale Accuracy ±20V / ±0.8mV / ±3.0mV ±10V / ±0.5mV / ±1.9mV ±5V / ±0.3mV / ±1.2mV * Input range is defined here as the entire active range of voltage differences between the two conductors in a differential HI/LO input pair. 'Equal to ±Vpk, or ±1/2*Vpp.
Small Signal Bandwidth:	Zero to 800kHz, -3dB with the filter disabled, or Zero to filter frequency if enabled.
Input Filter:	Selectable either as 'no filter', or as a 5th order Chebyshev, 200kHz, 0.5dB, continuous-time lowpass analog filter.
Settling Time:	2us to 0.1% for halfscale step; typical with input filter disabled.
Data Latency::	2.2us typically from each sample clock to the appearance in the buffer (or low-latency registers) of data from all active channels.
Input Power Bandwidth:	2-Chan Config: 4.8 Vpp-MHz; -3dB; typical. 4,6-Chan Config: 11 Vpp-MHz; -3dB; typical.
Dynamic Range, Typical, ±20V Range, 500KSPS	Freq Range / Filter Disabled * / Filter Enabled * 10Hz - 10kHz / 113dB / 111dB / 113dB / 110dB 10Hz - 200kHz / 101dB / 98dB / 95dB / 93dB * The first figure refers to a 2-Channel board; the second figure applies to 4 and 6-Channel boards. Subtract 2dB for ±10V range.
Integral Nonlinearity:	±0.002 percent FSR. (FSR = fullscale range; e.g.: 40V on ±20V range).
Differential Nonlinearity:	±0.001 percent FSR
Low Latency:	(Optional) In addition to the FIFO buffer, 32 data registers are directly accessible by single-reads for minimum latency, and are updated at the full sample rate.

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Input Operating Modes and Controls

Input Data Buffer:	256K-sample FIFO
Input Data Format:	18 Bits, selectable as offset binary or two's complement coding, with attached channel number and end-of-burst tag.
Sample Clock Sources:	Internal rate generator; External Hardware Clock I/O, Software clock.
Sampling Modes:	Continuous sampling or triggered burst.
Internal Rate Generators:	Two independent rate generators, one for ADC clocking; one for burst triggering. Both programmable from 3-550,000 sample clocks per second, using 24-Bit dividers from the master clock frequency.
External Sync I/O:	TTL, clock and burst trigger. Zero to 550,000 sample clocks per second.
Auxiliary External Clk/Sync:	Internal connector supports external clock and sync (trigger) control within the enclosure.

Digital Input/Outputs:

Eight TTL I/O lines in two groups of four bits, group-configurable as inputs or outputs. 0.2ma maximum input loading as current source, 8ma output loading as either source or sink. Direct register control.

PCI Compatibility:

Conforms to PCI Specification 2.3, D32 read/write, 33/66MHz, universal (5V/3.3V) signaling,
Supports block-mode and demand-mode DMA data transfers as bus master in either of two channels.

PHYSICAL PARAMETERS

Power Requirements:

+5VDC ±0.2 VDC at 1.3 Amps typical for 2-Channel and 4-Channel configurations; 1.6 Amps typical for 6-Channel configuration.

Maximum Power Dissipation: Side-1: 6.8 Watts. Side-2: 2.5 Watts.

Mechanical Characteristics *(PMC form factor)*

Height: 13.5 mm (0.53 in)
Depth: 143.75 mm (5.66 in)
Width: 74.0 mm (2.91 in)

Environmental Specifications

Ambient Temperature Range:

Standard Temperature:	Operating: 0 to +70 Degrees Celsius * Storage: -40 to +85 Degrees Celsius
Extended Temperature:	Operating: -40 to +80 Degrees Celsius * Storage: -40 to +85 Degrees Celsius
	* Air temperature at board surface.
Relative Humidity:	0 to 95%, non-condensing
Altitude:	Operation to 10,000 ft.
Cooling:	Conventional air cooling; 150 LFPM

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ORDERING INFORMATION

Specify the basic product model number followed by an option suffix "**-A-B-C-D-E**", as indicated below. For example, model number **PMC66-18AISS6C-2-20V-F1-45M** describes a PMC module with two input channels, high-level input ranges (±20V,±10V), standard F1 filter type, standard 45MHz master clock frequency, and standard latency.

Basic Model Number	Form Factor
PMC66-18AISS6C	**PMC** (Native)
PCI66-18AISS6C [1, 2]	**PCI, short length**
cPCI66-18AISS6C [1, 2]	**cPCI, 3U**
PC104P66-18AISS6C [1, 3]	**PC104-*Plus***
PCIe-18AISS6C [1, 3]	**PCI Express**

[1] Contact factory for availability in native form factors.
[2] PMC module installed and tested on an adapter, with mechanical and functional equivalency.
[3] PMC module installed and tested on an adapter, with functional equivalency.

Optional Parameter	Value	Specify Option As:
Number of Input Channels	2 Channels	A = 2
	4 Channels	A = 4
	6 Channels	A = 6
Input Range Set	High-Level Range Set: Software-selectable ±20V or±10V	B = 20V
	Low-Level Range Set: Software-selectable ±10V or ±5V	B = 10V
Lowpass Input Filter Type	Chebyshev, 200kHz, 5th order, 0.5dB	C = F1
	Chebyshev, 100kHz, 5th order, 0.5dB	C = F2
	Custom Filter [2]	C = F3, F4, etc.
Master Clock Frequency:	Standard frequency = 45.000 MHz	D = 45M
	Specify nonstandard frequency [1]	D = (frequency, MHz)M
Data Latency	Standard latency	E = Blank or Zero
	Low-Latency [1]	E = LL

[1] 45-48MHz. Contact factory for availability of nonstandard frequencies.
[2] Contact factory for availability of custom features.

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Table 1. System I/O Connector

ROW-A	
PIN	SIGNAL
1	INPUT RTN
2	INPUT RTN
3	INPUT 00 LO
4	INPUT 00 HI
5	INPUT RTN
6	INPUT RTN
7	INPUT 01 LO
8	INPUT 01 HI
9	INPUT RTN
10	INPUT RTN
11	INPUT 02 LO
12	INPUT 02 HI
13	INPUT RTN
14	INPUT RTN
15	INPUT 03 LO
16	INPUT 03 HI
17	INPUT RTN
18	INPUT RTN
19	INPUT 04 LO
20	INPUT 04 HI
21	INPUT RTN
22	INPUT RTN
23	INPUT 05 LO
24	INPUT 05 HI
25	INPUT RTN
26	INPUT RTN
27	VTEST LO
28	VTEST HI
29	INPUT RTN
30	INPUT RTN
31	INPUT RTN
32	INPUT RTN
33	INPUT RTN
34	INPUT RTN

ROW-B	
PIN	SIGNAL
1	DIGITAL RTN
2	DIGITAL RTN
3	DIGITAL RTN
4	DIGITAL RTN
5	DIGITAL RTN
6	DIGITAL RTN
7	DIGITAL RTN
8	DIGITAL RTN
9	DIGITAL RTN
10	DIGIO 00
11	DIGITAL RTN
12	DIGIO 01
13	DIGITAL RTN
14	DIGIO 02
15	DIGITAL RTN
16	DIGIO 03
17	DIGITAL RTN
18	DIGIO 04
19	DIGITAL RTN
20	DIGIO 05
21	DIGITAL RTN
22	DIGIO 06
23	DIGITAL RTN
24	DIGIO 07
25	DIGITAL RTN
26	INP TRIG OUT *
27	DIGITAL RTN
28	INP TRIG INP *
29	DIGITAL RTN
30	INP CLK OUT *
31	DIGITAL RTN
32	INP CLK INP *
33	DIGITAL RTN
34	DIGITAL RTN

.* TTL, asserted LOW.

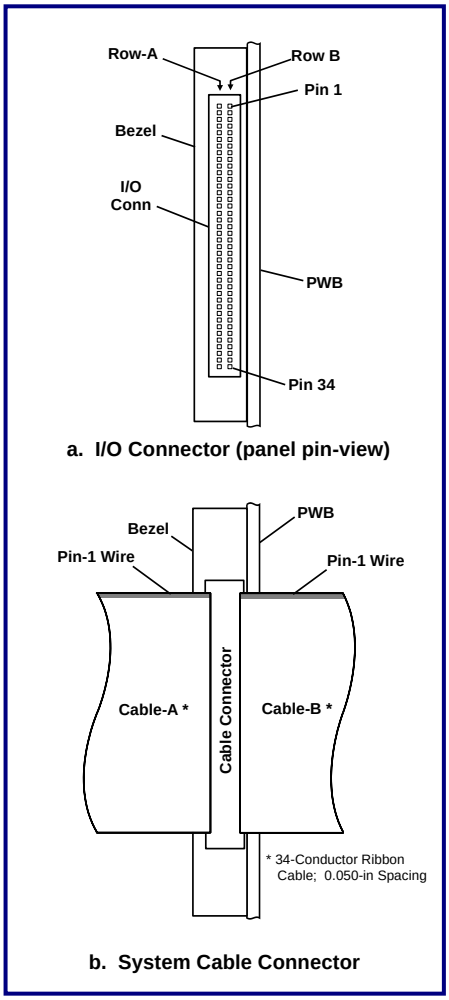

Figure 2. System I/O Connector

Table 2. Sync-I/O Connector (Side-2)

PIN	SIGNAL
1	DIGITAL RTN
2	AUX CLOCK I/O
3	DIGITAL RTN
4	AUX SYNC I/O
5	DIGITAL RTN
6	(No internal connection)

Recommended Sync-I/O mating cable connector is:
Molex# 51146-0600.

System Cable Mating Connector:
68-pin 0.050" Subminiature connector with metal shield:
AMP #749621-7 or equivalent.

I/O Connector Installed on Board (Ref)**:**
Amp # 787170-7.

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