General Standards Corporation

High Performance Bus Interface Solutions

66-16AISS2AO2A2M

16-Bit, 4-Channel, 2-MSPS PMC Analog Input/Output Board

With Two Simultaneously Sampled Analog Inputs, Two Analog Outputs, and Eight Buffered Digital Outputs

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Input and Output Sampling Rates to 2.0 MSPS per channel

FEATURES:

Analog Inputs:

- Two Differential Analog Inputs with dedicated 16-Bit ADC per channel
- True Simultaneous Sampling of all inputs to 2.0 MSPS per channel
- SAR Architecture; No minimum sample rate

Analog Outputs:

- Two Single-Ended Analog Outputs with dedicated 16-Bit DAC per channel
- Simultaneous Output clocking rates to 2.0 MSPS per channel
- Selectable Direct-Write or FIFO-Buffered access
- Outputs-Disconnect feature ensures quiet, zeroed outputs during power-up and autocalibration
- Buffer Configurable as Open for data streaming, or Circular for periodic functions

Common Analog I/O Features:

- Selectable Input/Output Ranges: ±10V, ±5V, ±2.5V
- Independent 2.0 Megasample input and output FIFO data buffers
- Hardware Clock and Sync I/O for multiboard operation
- Timing Controlled by internal rate generator, by software clocking, or externally

8-Bit Buffered TTL Digital Output Port:

- Eight TTL digital output channels
- 8x256K-sample data FIFO
- Clocking rates from Zero to 2MHz; Internal or external clock source

General:

- 8-Bit Bidirectional TTL digital I/O port
- DMA Engine minimizes bus congestion
- Internal Power Conversion; Single 5-Volt power requirement
- Independent 24-Bit frequency dividers
- Internal Autocalibration
- 66 MHz 32-Bit PCI Support, with universal 5V/3.3V signaling
- Single-Width PMC form factor with integral EMI shield
- Extended-temperature version available

TYPICAL APPLICATIONS:

✓ High Performance Data Acquisition	✓ Event Capture	✓ Robotics
✓ Arbitrary Waveform Generation	✓ Ultrasound	✓ Positioning Systems

****** *PRELIMINARY* ******

REV: 052517

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FUNCTIONAL DESCRIPTION

The 16-Bit 66-16AISS2AO2A2M analog I/O module samples and digitizes two input channels simultaneously at rates up to 2.0 million samples per second for each channel. The resulting 16-bit sampled data is available to the PCI bus through a 2 Megasample FIFO buffer. Sampling can be controlled in groups of either 1 or 2 channels, and the sample clock can be generated (a) from an internal rate generator, (b) through software, or (c) by external hardware. Both burst and continuous sampling modes are supported. Input ranges are software-selectable as ±10V, ±5V, or ±2.5V, and can be assigned independently to either input channel.

Two analog output channels provide software-selected output ranges of ±2.5V, ±5V or ±10V, and are accessed either directly through dedicated control registers, or output data can be routed through a 2 Megasample FIFO buffer for waveform generation. The output ranges are selected independently from the input channel ranges. An outputs-disconnect feature can be invoked on-demand, and automatically zeroes the outputs during power-up and autocalibration sequences.

A buffered digital output port provides Byte-wide TTL output data through an 8-Bit by 256K deep FIFO that can be clocked at any rate up to 2MHz. A second Byte-wide TTL port is bidirectional and non-buffered, and can be read-accessed or write-accessed directly from the host bus.

On-demand autocalibration determines and applies offset and gain correction values for all input and output channels. A selftest input switching network routes output channels or calibration reference signals to the analog inputs, and permits board integrity to be verified by the host.

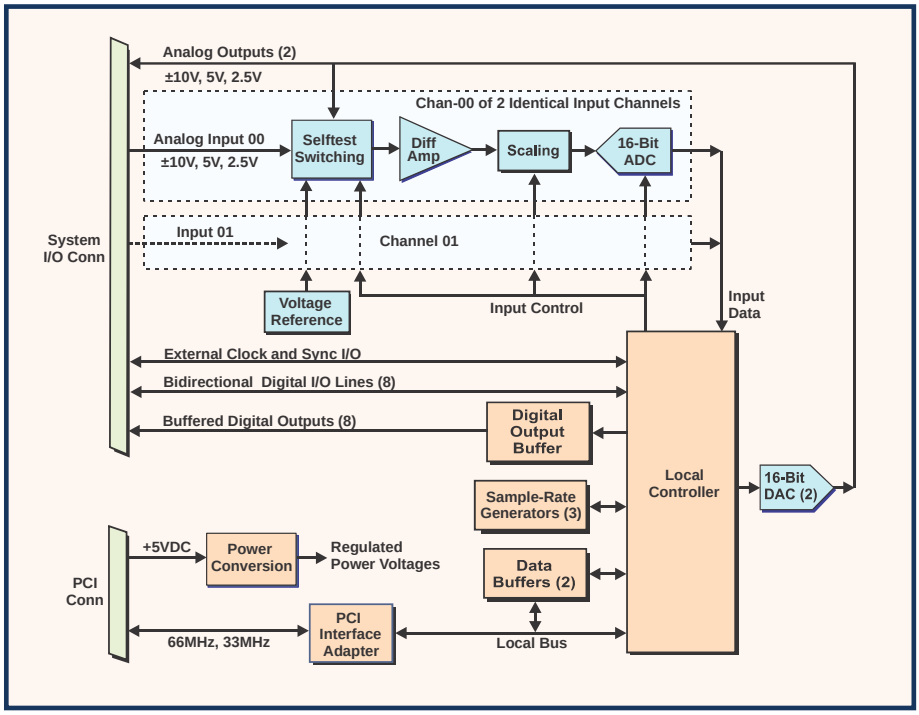

Figure 1. 66-16AISS2AO2A2M; Functional Organization

This product is functionally compatible with the IEEE PCI local bus specification Revision 2.3, and supports the "plug-n-play" initialization concept. System connections are made at the front panel through a high-density dual-ribbon 80-pin connector. Power requirements consist of +5 VDC in compliance with the PCI specification, and analog power voltages are generated internally. All operational parameters are software configurable. Operation over the specified temperature range is achieved with conventional air cooling.

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PERFORMANCE SPECIFICATIONS

At +25 ^{O}C, with specified operating voltages

Analog Input Characteristics:

Configuration:	Two differential analog input channels; Dedicated 16-Bit ADC per channel.
Voltage Ranges:	Independently assignable between two groups of input channels as: ±10V, ±5V or ±2.5V full scale.
Input Impedance:	2 Megohms Line-Line in parallel with 40pF.
Bias Current:	100 nanoamps typical all ranges
Crosstalk Rejection:	84dB, DC-10kHz. 70dB at 100kHz.
Signal/Noise Ratio (SNR):	82dB typical; 10Hz to 500kHz
Common Mode Rejection:	65dB DC-10kHz; 53dB at 100kHz. Typical with CMV = ±10V, Vin = Zero.
Overvoltage Protection:	±25V with power applied, ±15 Volts with power removed.

Analog Input Transfer Characteristics:

Resolution:	16 Bits (0.0015 percent of FSR)		
Sample Rate:	Zero to 2.0 MSPS per channel		
Sampling Mode::	Simultaneous; all active input channels		
DC Accuracy:	Range	Midscale Accuracy	Fullscale Accuracy
(Maximum composite error after autocalibration)	±10V	± 2mV	± 5mV
	±5V	± 1mV	± 3mV
	±2.5V	± 0.8mV	± 2mV
Small Signal Bandwidth:	Zero to 5MHz, -3dB, all ranges		
Settling Time:	500ns to 0.1%; halfscale step; typical; all ranges.		
Power Bandwidth:	3MHz, 10Vp-p, -3dB		
Integral Nonlinearity:	±0.007 percent FSR (FSR = fullscale range; e.g.: 20V on the ±10Vrange).		
Differential Nonlinearity:	±0.003 percent FSR.		

Analog Input Operating Modes and Controls

Input Data Buffer:	2.0 Megasample FIFO
Sample Clock Sources:	Internal rate generator; External Hardware Clock I/O, Software clock.
Sampling Modes:	Continuous sampling, and triggered burst.
Internal Rate Generators:	Two independent rate generators, one for ADC clocking; one for burst triggering. Both programmable from 3-2,000,000 sample clocks per second, using 24-Bit dividers from the master clock frequency.
External Clock I/O:	TTL, bidirectional. Zero to 2,000,000 sample clocks per second.
Principal Status Register:	Consolidates critical status flags at a single Longword location.
Input Data Format:	16 Bits. Selectable as offset binary or two's complement. First-channel and end of-burst tagged.

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Analog Output Characteristics:

Configuration:	Two single-ended 16-Bit analog output channels.
Voltage Ranges:	±10, ±5 or ±2.5 Volts; Independent of analog input ranges.
Output Resistance:	1.0 Ohm maximum at I/O connector pins. (>10K if outputs disconnected).
Output protection:	Withstands sustained short-circuiting to ground
Outputs-Disconnect	Disconnects the output drivers from the system I/O connector.
Load Current:	Zero to ±3ma per channel
Load Capacitance:	Stable with any load capacitance
Noise:	2.0mV-RMS, 10Hz-100KHz typical
Glitch Impulse:	7 nV-s, typical on ±5V range

Analog Output Transfer Characteristics:

Resolution:	16 Bits (0.0015 percent of FSR)		
Output Access:	Direct register access or 256K-Sample FIFO buffer.		
DC Accuracy:	Range	Midscale Accuracy	±Fullscale Accuracy
(Max error, no-load)	±10V	±4mV	±8mV
	±5V	±2mV	±6mV
	±2.5V	±1.5mV	±4mV
Settling Time:	1.5us to 0.1 percent, typical with halfscale step, no-load.		
Crosstalk Rejection:	70 dB minimum, DC-100 kHz		
Integral Nonlinearity:	±0.007 percent of FSR, maximum		
Differential Nonlinearity:	±0.002 percent of FSR, maximum		
Output Data Format:	16 Bits. Selectable as offset binary or two's complement.		

Analog Output Operating Modes and Controls

Output Data Buffer:	2.0 Megasample FIFO
Sample Clock Sources:	Internal rate generator; External Clock I/O, Software clock.
Burst Triggering Sources:	TTL external Trigger I/O (shared with analog inputs), Software trigger.
Clocking Modes:	Continuous or periodic clocking, and triggered burst.
Internal Rate Generator:	Programmable from 3-2,000,000 output clocks per second. Divides Master Clock frequency to clocking rate using a 24-bit divider.
External Clock I/O:	TTL, bidirectional. Zero to 2,000,000 sample clocks per second.

Bidirectional Digital I/O Port:

8-Bit TTL bidirectional port. Standard TTL levels. Direct register read/write access.
±10 mA loading when configured as outputs. Inputs pulled up to +3.3V through 33K.

Buffered Digital Output Port:

8-Bit TTL output port, driven through an 8-Bit by 256K deep FIFO. Standard TTL levels. ±10 mA loading. Clocked to 5 MSPS an internal 24-bit divider from the master clock (40.32MHz), or to 1 MSPS from an external source. Also clocked by a S/W clock control bit.

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PCI Compatibility:

Conforms to PCI Specification 2.3, D32 read/write, 33/66MHz, universal (5V/3.3V) signaling, Supports block-mode and demand-mode DMA data transfers in two channels as bus master.

Power Requirements

+5VDC ±0.25 VDC at 1.5 Amp maximum, 1.1 Amp typical.

Maximum Power Dissipation: Side-1: 6.5 Watts. Side 2: 1.0 Watt.

Mechanical Characteristics

Height:	13.5 mm (0.53 in)
Depth:	149.0 mm (5.87 in)
Width:	74.0 mm (2.91 in)
Shield:	Side-1 is protected by an EMI shield.

Environmental Specifications

Ambient Temperature Range:

Standard Temperature:	Operating: 0 to +70 Degrees Celsius * Storage: -40 to +85 Degrees Celsius
Extended Temperature:	Operating: -40 to +85 Degrees Celsius * Storage: -40 to +85 Degrees Celsius
	* Air temperature at board surface.
Relative Humidity:	0 to 95%, non-condensing
Altitude:	Operation to 10,000 ft.
Cooling:	Conventional air cooling; 150 LFPM

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ORDERING INFORMATION

Specify the basic product model number followed by an option suffix "-A-B-C-D", as indicated below. For example, model number **PMC66-16AISS2AO2A2M-2-2 -40.320M** describes a PMC module with two input channels, two output channels, a 40.320MHz master clock frequency, and no custom features.

Basic Model Number	Form Factor
PMC66-16AISS2AO2A2M	PMC (Native)
PCI66-16AISS2AO2A2M[1]	PCI, short length
Cpci66-16AISS2AO2A2M[1]	cPCI, 3U
PCIe66-16AISS2AO2A2M[1]	PCI Express
PC104P66-16AISS2AO2A2M	PC104-*Plus*
PCIe10466-16AISS2AO2A2M[1,2]	PCIe, one-lane on PC/104 form factor

[1] Module installed and tested on an adapter, with mechanical and functional equivalency. Contact factory for availability in native form factors.

[2] PCIe104 supports only the PCIe bus.

Optional Parameter	Value	Specify Option As:
Number of Input Channels	**2 Input Channels**	**A = 2**
	1 Input Channel [1]	**A = 1**
Number of Output Channels	**2 Output Channels**	**B = 2**
	No Analog Outputs [1]	**B = 0**
Master Clock Frequency [1,2]	**40.32MHz**	**C = 40.32M**
Custom Feature	**---**	**D** [3]

[1] Contact Sales for availability.
[2] Custom frequencies available from 40-42MHz.
[3] Numeric code, determined by specific feature. Blank or zero (0) if no custom feature applies.

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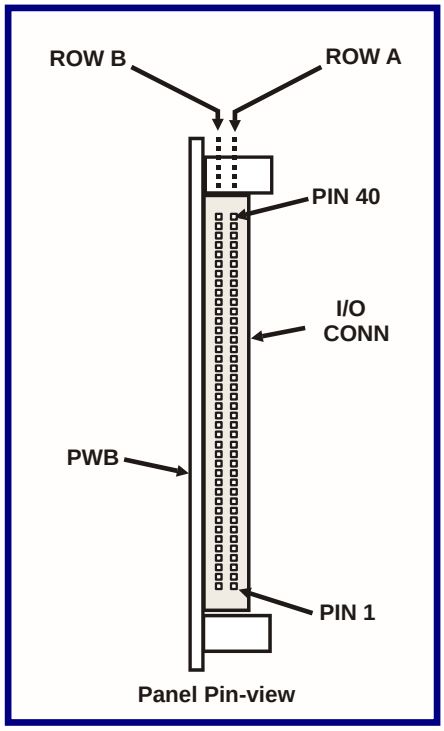
SYSTEM INTERFACE CONNECTOR

Table 1. System I/O Connector

ROW-A	
PIN	SIGNAL
1	OUTPUT RTN
2	ANA OUT 00
3	OUTPUT RTN
4	ANA OUT 01
5	OUTPUT RTN
6	INPUT RTN
7	INPUT RTN
8	INPUT RTN
9	INP00 LO
10	INP00 HI
11	INPUT RTN
12	INPUT RTN
13	INP01 LO
14	INP01 HI
15	INPUT RTN
16	INPUT RTN
17	VTEST RTN
18	VTEST
19	INPUT RTN
20	INPUT RTN
21	DIGITAL RTN
22	DIG OUT 00 *
23	DIGITAL RTN
24	DIG OUT 01 *
25	DIGITAL RTN
26	DIG OUT 02 *
27	DIGITAL RTN
28	DIG OUT 03 *
29	DIGITAL RTN
30	DIG OUT 04 *
31	DIGITAL RTN
32	DIG OUT 05 *
33	DIGITAL RTN
34	DIG OUT 06 *
35	DIGITAL RTN
36	DIG OUT 07 *
37	DIGITAL RTN
38	DIG OUT CLK INP *
39	DIGITAL RTN
40	DIGITAL RTN

ROW-B	
PIN	SIGNAL
1	INPUT RTN
2	INPUT RTN
3	INPUT RTN
4	INPUT RTN
5	INPUT RTN
6	INPUT RTN
7	INPUT RTN
8	INPUT RTN
9	INPUT RTN
10	INPUT RTN
11	INPUT RTN
12	INPUT RTN
13	INPUT RTN
14	INPUT RTN
15	INPUT RTN
16	INPUT RTN
17	INPUT RTN
18	INPUT RTN
19	DIGITAL RTN
20	DIO 00 **
21	DIGITAL RTN
22	DIO 01 **
23	DIGITAL RTN
24	DIO 02 **
25	DIGITAL RTN
26	DIO 03 **
27	DIGITAL RTN
28	DIO 04 **
29	DIGITAL RTN
30	DIO 05 **
31	DIGITAL RTN
32	DIO 06 **
33	DIGITAL RTN
34	DIO 07 **
35	DIGITAL RTN
36	OUTPUT CLK I/O
37	DIGITAL RTN
38	TRIGGER I/O
39	DIGITAL RTN
40	INPUT CLK I/O



* Buffered digital output port.
** Bidirectional digital I/O port.

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