66-16AI64SSC

64-Channel, 16-Bit Simultaneous Sampling PMC Analog Input Board

With 200 KSPS Sample Rate per Channel and 66 MHz PCI Support

Available in PMC, PCI, cPCI and PC104-*Plus* and PCI Express form factors as:

PMC66-16AI64SSC:	**PMC**, Single-width
PCI66-16AI64SSC:	**PCI**, short length
Cpci66-16AI64SSC:	**cPCI,** 3U
PC104P66-16AI64SSC:	**PC104-*Plus***
PCIe66-16AI64SSC:	**PCI Express**
PCIe10466-16AI64SSC:	**PCIe, one-lane on PC/104 form factor**

See Ordering Information for details. Call for availability of other form factors, such as XMC, CCPMC, etc. PMC66-16AI64SSA also is described in this specification.

Features

- **64 Analog Inputs with Dedicated 200KSPS 16-Bit ADC per Channel**
- **Simultaneous Sampling of all Inputs; Minimum Data Skew**
- **Sampling Rates to 200 KSPS per Channel (12.8 MSPS Aggregate Rate)**
- **D32; 66MHz, 33MHz PCI Compatibility, with Universal 5V/3.3V Signaling**
- **Increased Throughput Capacity with Local Data Packing**
- **Continuous, Burst and Single-Sample Clocking Modes**
- Selectable Differential Processing Simulates Differential Operation of Channel Pairs
- Input Ranges: ±10V, ±5V, ±2.5V, 0/+5V, 0/+10V; Software-Selectable
- Hardware Sync I/O for Multiboard Operation
- 1 MByte FIFO Data Buffer; 512 K-Samples in packed-data mode.
- A low-latency feature provides 64 registers that duplicate the last sample from all A/D converters (PMC66-16AI64SSC only).
- 2-Channel DMA Engine
- Sampling Controlled by Internal Rate Generator, by Software Trigger, or Externally
- On-Demand Internal Autocalibration of all Channels
- Completely Software-Configurable; No Field Jumpers
- I/O available as either an 80-Pin connector for IDC cables, or a 68-Pin MDR (Mini-D Ribbon) connector.

Typical Applications

✓ High-Density Analog Inputs	✓ Industrial Robotics	✓ Acoustic Sensor Arrays
✓ Analog Event Capture	✓ Biometric Signal Analysis	✓ Dynamic Test Systems

- PRELIMINARY -

Rev: 102715

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The 16-Bit PMC66-16AI64SSC analog input module samples and digitizes 64 input channels simultaneously at rates up to 200,000 samples per second for each channel. Each input channel contains a dedicated 16-Bit sampling ADC, and the resulting 16-bit sampled data is available to the PCI bus through a 1 MByte FIFO buffer. The 32-Bit local data path supports full D32 local-bus data packing. Throughput capacity is further enhanced with 66MHz PCI support and increased local clocking frequency. All operational parameters are software configurable.

Inputs can be sampled in groups of 2, 4, 8, 16, 32 or 64 channels; or any single channel can be sampled continuously. The sample clock can be generated from an internal rate generator, or by software or external hardware. Input ranges are software-selectable as ±10V, ±5V or ±2.5V.

An on-demand autocalibration feature determines offset and gain correction values for each input channel, and applies the corrections subsequently during acquisition. A selftest switching network routes calibration reference signals to each channel through internal selftest switches, and permits board integrity to be verified by the host..

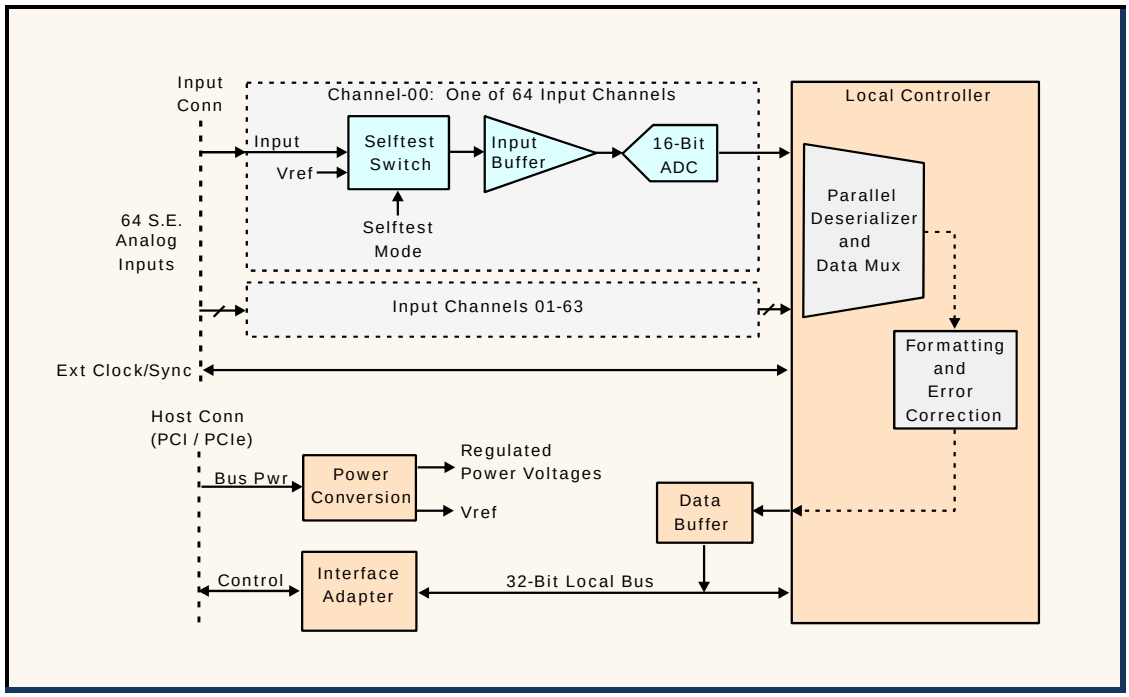

Figure 1. PM66-16AI64SSC; Functional Organization

This product is designed for minimum off-line maintenance. On-demand autocalibration eliminates the need for disconnecting or removing the module from the system for calibration. System connections are made at the front panel through either a high-density 80-Pin connector for IDC cables, or a 68-pin MDR connector. Power requirements consist of +5 VDC, in compliance with the PCI specification, and operation over the specified temperature range is achieved with conventional convection cooling.

Note: This specification encompasses the legacy product PMC66-16AI64SSA, but not all featres described here are available with the PMC66-16AI64SSA.

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Performance Specifications

At +25 ^{O}C, with specified operating conditions, and with differential processing deselected

Input Characteristics:

Configuration:	64 single-ended analog input channels; Dedicated 16-Bit ADC per channel. Optional 32-Channel version available.
Voltage Ranges:	Software configurable as ±10V, ±5V, ±2.5V, 0/+5V or 0/+10V full scale
Input Impedance:	750 KOhms, typical.
Bias Current:	1ua maximum, ±2.5V range; 4ua maximum ±10V range
Crosstalk Rejection:	85dB typical, DC-50kHz
Input Noise:	0.5 mVRMS; typical, all ranges; 0.01-50kHz (1.0mVRMS with differential processing selected)
Overvoltage Protection:	±40 Volts with power removed; ±25V with power applied.

Transfer Characteristics:

Resolution:	16 Bits (0.0015 percent of FSR)
Maximum Sample Rate:	200 KSPS per channel
Input Bandwidth (-3dB):	DC to 120 kHz typical
Channels per Sample:	Lowest 2, 4, 8, 16, 32 or 64 channels; or any single channel.

DC Accuracy: (Maximum composite error after autocalibration)

Range	Zero-Input *	Fullscale *
±10V	± 1.5mv	± 2.8mv
±5V	± 1.4mv	± 2.5mv
±2.5V	± 0.9mv	± 1.5mv
0/+10V	± 1.8mv	± 3.0mv
0/+5V	± 1.2mv	± 2.7mv

* Averaged values, referred to inputs. Typical values are approximately one-half the maximum values shown here.

Integral Nonlinearity:	±0.008 percent of FSR, maximum
Differential Nonlinearity:	±0.004 percent of FSR, maximum

Analog Input Operating Modes and Controls

Input Data Buffer:	1 MByte Fifo; 512 K-Samples in packed-data mode. An optional 'Low-Latency' array of 64 data registers is available, in addition to the FIFO.
Sample Clock Sources:	Internal rate generator; External Hardware Sync I/O, Software clock. Continuous, Burst and Single-Sample Clocking Modes.
Rate Generator:	Programmable from 0.01-200,000 sample clocks per second. Divides the local master clock to the sample rate. (See ordering information).
External TTL Sync:	Bidirectional TTL line; Zero to 200,000 sample clocks per second.
Auxiliary Sync I/O:	Four independent bidirectional "PXI" lines in both PMC-P1/P2 and edge-board header; Zero to 200,000 sample clocks per second.
Input Data Format:	Nonpacked Mode: 16-Bit data word plus single-bit Channel-00 tag. Packed Mode: Lword sync code followed by packed channel data. Even-numbered channels occupy lower word (D00-15), odd channels occupy upper word (D16-31).
Data Format:	Selectable as offset binary or two's complement.
Differential Processing:	Selectable processing options process input data as 63 pseudo-differential channels (common return) or as 32 full-differential channels.

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PCI Compatibility:

Conforms to PCI Specification 2.3, with 66MHz/33MHz, D32 and universal signaling (5/3.3 Volt).
Single multifunction interrupt.
DMA transfers as bus master with two DMA channels.

Power Requirements

+5VDC ±0.2 VDC at 1.2 Amp maximum, 0.8 Amp typical.

Maximum Power Dissipation: Side-1: 5.0 Watts. Side 2: 1.0 Watt.

Physical Parameters

Mechanical Characteristics (PMC Form Factor)

Height:	13.5 mm (0.53 in)
Depth:	149.0 mm (5.87 in)
Width:	74.0 mm (2.91 in)
Shield:	Side-1 is protected by an EMI shield.

Environmental Specifications

Ambient Temperature Range:

Standard Temperature:	Operating: 0 to +70 Degrees Celsius * Storage: -40 to +85 Degrees Celsius
Extended Temperature:	Operating: -40 to +80 Degrees Celsius * Storage: -40 to +85 Degrees Celsius
	* Air temperature at board surface.
Relative Humidity:	0 to 95%, non-condensing
Altitude:	Operation to 10,000 ft.
Cooling:	Conventional air cooling; 150 LFPM

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Ordering Information

Specify the basic product model number followed by an option suffix "-A-B-C-D-E", as indicated below. For example, model number PMC66-16AI64SSC-64-49.152M-50K-LL-MDR describes a board with 64 input channels, a 49.152MHz master clock frequency, 50kHz input filter, Low-Latency feature, and a 68-pin MDR (Mini-D Ribbon) I/O connector.

Basic Model Number	Form Factor
PMC66-16AI64SSC	PMC (Native)
PCI66-16AI64SSC [1]	PCI, short length
Cpci66-16AI64SSC [1]	cPCI, 3U
PCIe66-16AI64SSC [1]	cPCI, 3U
PC104P66-16AI64SSC	PC104-*Plus*
PCIe10466-16AI64SSC [1,2]	PCIe, one-lane on PC/104 form factor

[1] Module installed and tested on an adapter, with mechanical and functional equivalency. Contact factory for availability in native form factors.

[2] PCIe104 supports only the PCIe bus.

Optional Parameter	Value	Specify Option As:
Number of Input Channels	64 Channels	A = 64
	32 Channels	A = 32
Master Clock Frequency	45.000 MHz	B = 45.000M
	49.152 MHz	B = 49.152M
	50.000 MHz	B = 50.000M
Custom Feature	No custom features	C = Blank or Zero [1]
	Input Filter = 50kHz	C = 50K
Data Latency	Standard latency	D = Blank or Zero [1]
	Low-Latency [2]	D = LL
I/O Connector	80-Pin; for flat Cables	E = 80P
	68-pin MDR (Mini-D Ribbon) [3]	E = MDR

[1] Insert a 'zero' for 'No custom features' or 'Standard Latency' if subsequent option fields are used.

[2] The low-latency option provides 64 data registers that duplicate the most recent data written to the buffer. ***Not available with the legacy PMC66-16AI64SSA.***

[3] Call for availability of alternative 68-Pin SCSI connector configurations.

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- 80-Pin System I/O Connector -

Table 1. 80-Pin I/O Connector for Flat Cables

ROW-A		ROW-B	
PIN	SIGNAL	PIN	SIGNAL
1	INP00	1	INP32
2	INP01	2	INP33
3	INP02	3	INP34
4	INP03	4	INP35
5	INPUT RTN	5	INPUT RTN
6	INP04	6	INP36
7	INP05	7	INP37
8	INP06	8	INP38
9	INP07	9	INP39
10	INPUT RTN	10	INPUT RTN
11	INP08	11	INP40
12	INP09	12	INP41
13	INP10	13	INP42
14	INP11	14	INP43
15	INPUT RTN	15	INPUT RTN
16	INP12	16	INP44
17	INP13	17	INP45
18	INP14	18	INP46
19	INP15	19	INP47
20	INPUT RTN	20	INP48
21	INP16	21	INPUT RTN
22	INP17	22	INP49
23	INP18	23	INP50
24	INP19	24	INP51
25	INPUT RTN	25	INP52
26	INP20	26	INP53
27	INP21	27	INPUT RTN
28	INP22	28	INP54
29	INP23	29	INP55
30	INPUT RTN	30	INP56
31	INP24	31	INP57
32	INP25	32	INP58
33	INP26	33	INPUT RTN
34	INP27	34	INP59
35	INPUT RTN	35	INP60
36	INP28	36	INP61
37	INP29	37	INP62
38	INP30	38	INP63
39	INP31	39	SYNC I/O RTN
40	INPUT RTN	40	SYNC I/O

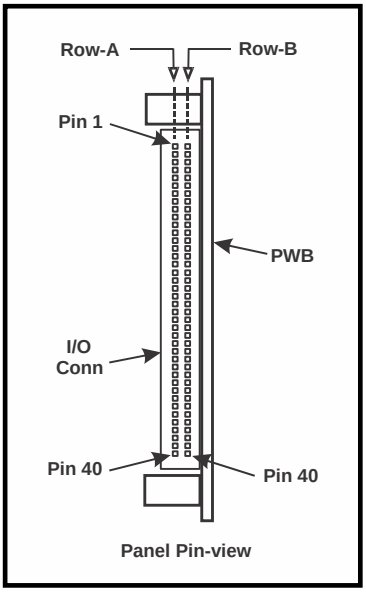

Figure 2. 80-Pin System Connector

System Mating Connector:

Standard 80-pin 0.050" dual-ribbon socket connector:

Robinson Nugent P50E-080S-TG, or equivalent.

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(Continued)

- 68-Pin MDR (Mini-D Ribbon) System I/O Connector -

Table 2. 68-Pin MDR I/O Connector

PIN	SIGNAL	PIN	SIGNAL
1	INP00	35	INP32
2	INP01	36	INP33
3	INP02	37	INP34
4	INP03	38	INP35
5	INP04	39	INP36
6	INP05	40	INP37
7	INP06	41	INP38
8	INP07	42	INP39
9	INP08	43	INP40
10	INP09	44	INP41
11	INP10	45	INP42
12	INP11	46	INP43
13	INP12	47	INP44
14	INP13	48	INP45
15	INP14	49	INP46
16	INP15	50	INP47
17	INPUT RTN	51	INP48
18	INPUT RTN	52	INP49
19	INP16	53	INP50
20	INP17	54	INP51
21	INP18	55	INP52
22	INP19	56	INP53
23	INP20	57	INP54
24	INP21	58	INP55
25	INP22	59	INP56
26	INP23	60	INP57
27	INP24	61	INP58
28	INP25	62	INP59
29	INP26	63	INP60
30	INP27	64	INP61
31	INP28	65	INP62
32	INP29	66	INP63
33	INP30	67	SYNC I/O
34	INP31	68	SYNC I/O RTN

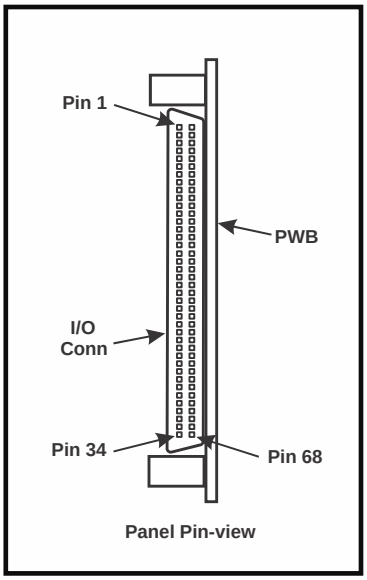

Figure 3. 68-Pin MDR Connector

System Mating Connector (Prelim):
68-pin MDR Connector:
3M# 10168-6000EC,
with plastic shielded shell:
3M# 10368-3210-006.

Board Connector (Ref, Prelim):
68-pin MDR Connector:
3M# 10268-5JBEPC.

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