General Standards Corporation

High Performance Bus Interface Solutions

Rev: 120708

PMC66-18AO8

18-Bit Eight-Output 500KSPS
Precision Wideband PMC Analog Output Board

REFERENCE MANUAL

PRELIMINARY DRAFT

TABLE OF CONTENTS

`TABLE OF CONTENTS (Continued)

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TABLE OF CONTENTS (Continued)

LIST OF TABLES

LIST OF ILLUSTRATIONS

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SECTION 1.0

INTRODUCTION

The PMC66-18AO8 is a precision 18-Bit analog output PMC that provides eight simultaneously clocked output channels. The outputs can be clocked synchronously or independently at rates up to 500 KSPS per channel, and are supported by a 256K-Sample FIFO data buffer. Both continuous and burst clocking modes are supported, and the output ranges are software-selectable as ±10V, ±5V or ±2.5V. Clocking and triggering rates can be derived from internal rate generators, or from external clock and trigger sources to support the synchronous operation of multiple boards.

The analog outputs use a weighted-DAC R-2R configuration which minimizes latency and has no minimum clocking rate. The outputs can be software-configured for either single-ended or 3-wire differential operation.

On-demand autocalibration determines and applies error correction for all analog output channels, and a selftest switching network permits board integrity to be verified by the host. Eight bidirectional digital I/O lines are programmable as inputs or outputs.

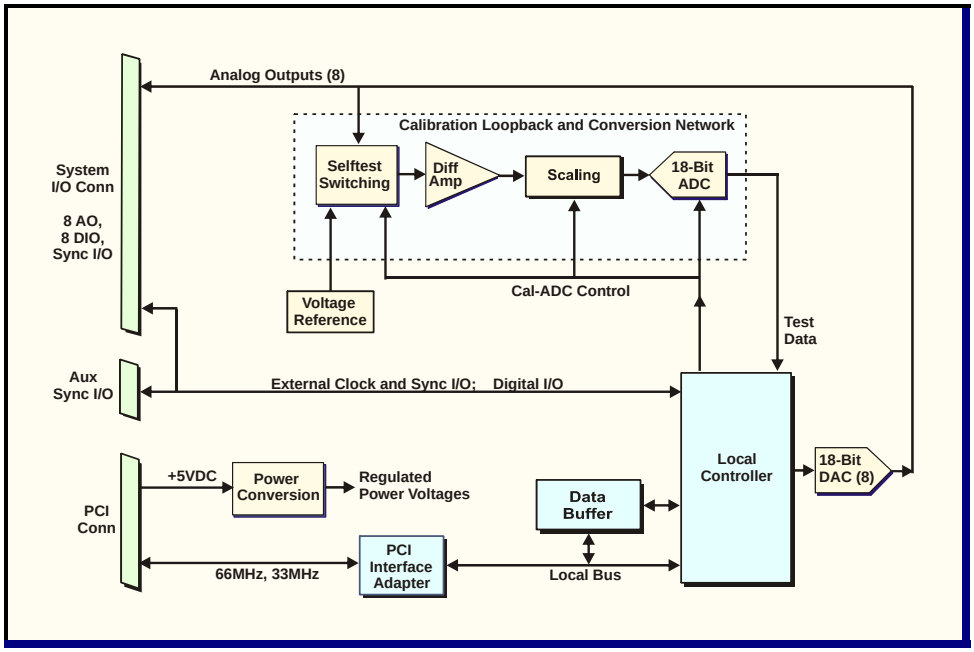

Figure 1.1-1. Functional Organization

This product complies with the IEEE PCI local bus specification Revision 2.3. System connections are made at the front panel through a high-density dual-ribbon 68-pin connector. Power requirements consist of +5 VDC in compliance with the PCI specification, and analog power voltages are generated internally. Operation over the specified temperature range is achieved with conventional air cooling.

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SECTION 2.0

INSTALLATION AND MAINTENANCE

2.1 Board Configuration

This product has no field-alterable configuration features, and is completely configured at the factory.

2.2 Installation

2.2.1 Physical Installation

To minimize the opportunity for accidental damage before installation, the board should be stored in the original protective shipping package. System power must be turned OFF before proceeding with the installation.

CAUTION: This product is susceptible to damage from electrostatic discharge (ESD). Before removing the board from the conductive shipping package, ensure that the work surface, the installer and the host board have been properly discharged to ground.

After removing the board from the shipping package, position the board with the two PCI connectors facing the mating connectors J1, J2 on the host board (Figure 2.2-1). Then carefully press the board into position on the host. Verify that the mezzanine connectors have mated completely and that the board is seated firmly against the host board. Attach the board to the host with 2.5 x 6.5mm panhead screws. Pass the screws through the host board into the corresponding mounting holes in the standoffs and front-panel bezel. Tighten the screws carefully to complete the installation. Do not overtighten.

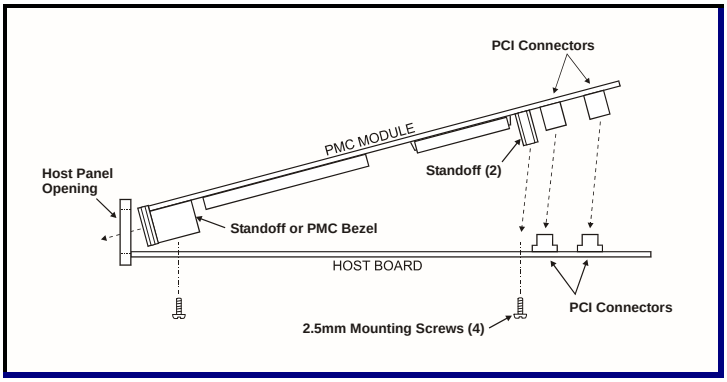

Figure 2.2-1. Mechanical Installation

2.2.2 Input/Output Cable Connections

System cable signal pin assignments are listed in Table 2.2-1. The I/O connector is designed to mate with a 68-pin dual-ribbon connector, equivalent to AMP #749621-7. The AMP displacement connector accepts two 34-wire 0.050-inch ribbon cables, with the pin numbering convention shown in Table 2.2-1 and in Figure 2.2-2. Contact the factory if preassembled cables are required.

Table 2.2-1. System I/O Connections

ROW-A			ROW-B	
PIN	SIGNAL		PIN	SIGNAL
1	OUTPUT 00 LO		1	DIGITAL RTN
2	OUTPUT 00 HI		2	DIGIO 00
3	OUTPUT RTN 00		3	DIGITAL RTN
4	OUTPUT RTN 00		4	DIGIO 01
5	OUTPUT 01 LO		5	DIGITAL RTN
6	OUTPUT 01 HI		6	DIGIO 02
7	OUTPUT RTN 01		7	DIGITAL RTN
8	OUTPUT RTN 01		8	DIGIO 03
9	OUTPUT 02 LO		9	DIGITAL RTN
10	OUTPUT 02 HI		10	DIGIO 04
11	OUTPUT RTN 02		11	DIGITAL RTN
12	OUTPUT RTN 02		12	DIGIO 05
13	OUTPUT 03 LO		13	DIGITAL RTN
14	OUTPUT 03 HI		14	DIGIO 06
15	OUTPUT RTN 03		15	DIGITAL RTN
16	OUTPUT RTN 03		16	DIGIO 07
17	OUTPUT 04 LO		17	DIGITAL RTN
18	OUTPUT 04 HI		18	DIGITAL RTN
19	OUTPUT RTN 04		19	CLOCK INPUT LO *
20	OUTPUT RTN 04		20	CLOCK INPUT HI *
21	OUTPUT 05 LO		21	DIGITAL RTN
22	OUTPUT 05 HI		22	DIGITAL RTN
23	OUTPUT RTN 05		23	CLOCK OUTPUT LO *
24	OUTPUT RTN 05		24	CLOCK OUTPUT HI *
25	OUTPUT 06 LO		25	DIGITAL RTN
26	OUTPUT 06 HI		26	DIGITAL RTN
27	OUTPUT RTN 06		27	TRIGGER INPUT LO *
28	OUTPUT RTN 06		28	TRIGGER INPUT HI *
29	OUTPUT 07 LO		29	DIGITAL RTN
30	OUTPUT 07 HI		30	DIGITAL RTN
31	OUTPUT RTN 07		31	TRIGGER OUTPUT LO *
32	OUTPUT RTN 07		32	TRIGGER OUTPUT HI *
33	OUTPUT RTN 07		33	DIGITAL RTN
34	OUTPUT RTN 07		34	DIGITAL RTN

(All output returns "OUTPUT RTN XX' are connected together internally)

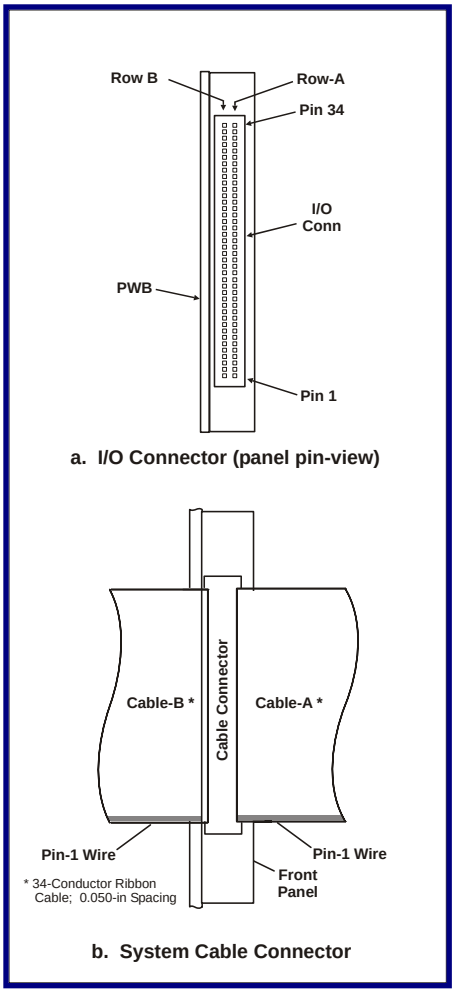

Figure 2.2-2. System I/O Connector

System Cable Mating Connector:
68-pin 0.050" Subminiature connector with metal shield:
AMP #749621-7 or equivalent.

I/O Connector Installed on Board (Ref)**:**
Amp # 787170-7.

Table 2.2-2. Sync-I/O Connector

PIN	SIGNAL
1	AUX CLOCK I/O LO *
2	AUX CLOCK I/O HI *
3	DIGITAL RTN
4	DIGITAL RTN
5	AUX TRIGGER I/O LO *
6	AUX TRIGGER I/O HI *

Recommended Sync-I/O mating cable connector is:
Molex# 51146-0600.

***** (Table 2.2.1 and Table 2.2.2) Edge-detected LVDS or TTL. When TTL sync I/O is selected, 'HI' pins use TTL signal levels, and 'LO' pins are left disconnected. Software-selected assertion on LOW or HIGH transition.

2.3 System Configuration

2.3.1 Analog Outputs

2.3.1.1 Output Configurations

The eight analog output channels can be software-configured either as 3-wire balanced differential outputs or as single-ended outputs.

Balanced differential outputs (Figure 2.3-1a) provide the highest immunity to system noise and interference, and are recommended for systems in which the loads will accept differential inputs. Each of the HI and LO outputs carries one-half of the output signal, with the two halves operating as complementary signals of equal amplitude and opposite polarity. Since radiated interference usually affects both output lines simultaneously, the coupled interference appears as a common mode signal which will be attenuated in a differential load.

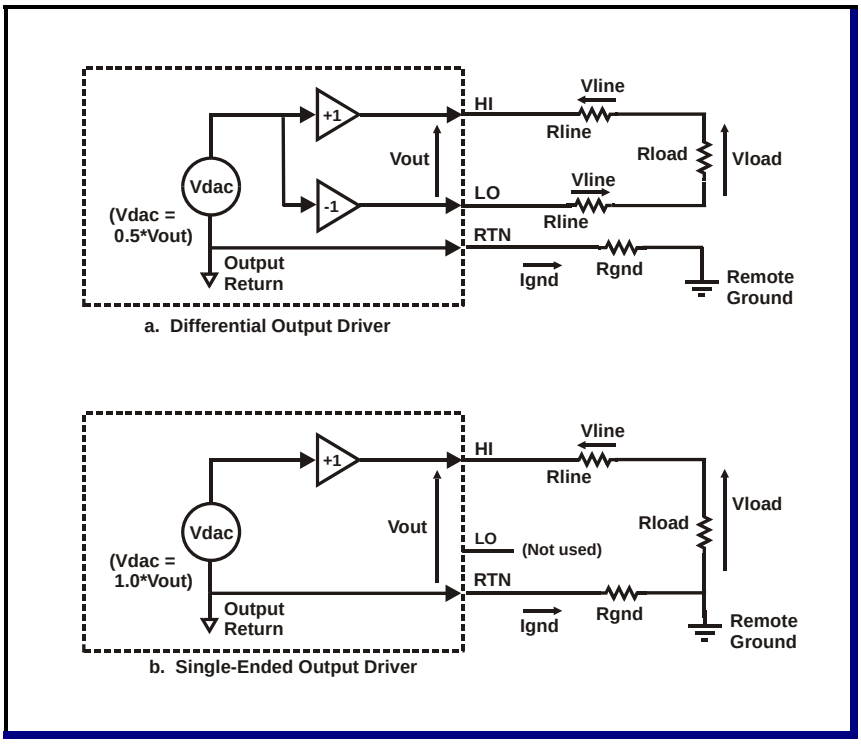

Figure 2.3-1. Output Configurations

For applications requiring single-ended outputs (Figure 2.3-1b), the output signal from each channel appears on the associated HI output pin, and is generated with reference to the output return pin. In general, single-ended outputs should drive only loads that are isolated from system ground. The best results are obtained when the loads also are isolated from each other

2.3.1.2 Loading Considerations

The voltage drop in the system I/O cable can be a significant source of error, especially with relatively long cables driving moderate or heavy loads. Figure 2.3-2 shows the effect of load current on the voltage drop in copper wire of various sizes. A 4.0 milliamp load for example, inserts a voltage drop of more than 0.25 millivolt *per foot* in #28 AWG ribbon cable; twice that if the return line also is considered. Several feet of ribbon cable therefore can produce significant errors with milliamp loads, especially in an 18-bit system, in which 1 LSB represents only 19 microvolts on a ±2.5 Volt range.

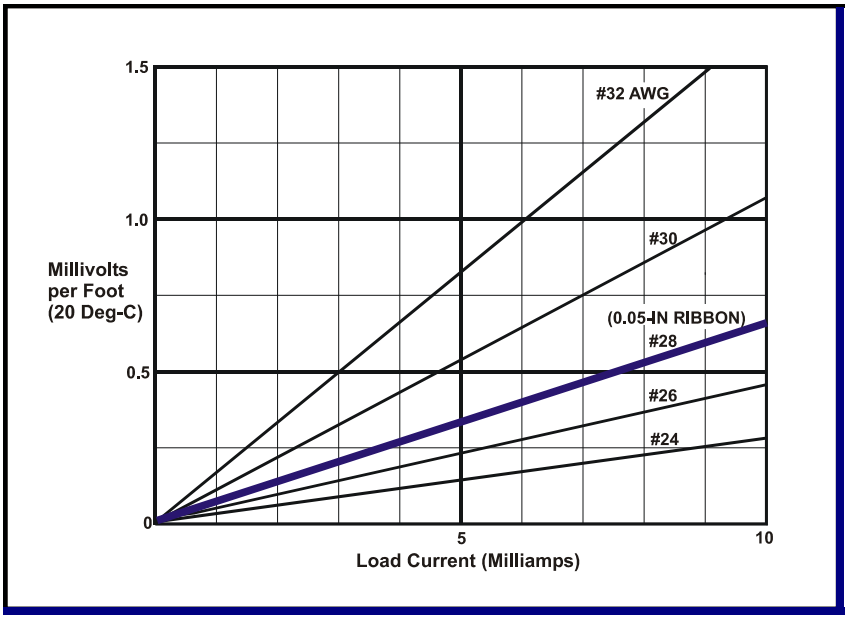

Figure 2.3-2. Line Loss versus Load Current

2.3.2 Multiboard Synchronization

If multiple boards are to be synchronized together, the input and output clock and/or trigger lines can be interconnected between boards in either a 'multidrop' configuration (Figure 2.3-3), or in a daisy-chained sequence (Figure 2.3-4). The multidrop arrangement eliminates the approximately 100ns delay incurred when passing through each board in a daisy-chain sequence, but limits the number of target boards to approximately four, depending upon cable lengths and quality. The number of target boards in a daisy-chain sequence is limited essentially only by the number of slots available in a backplane and the maximum acceptable total delay through the targets.

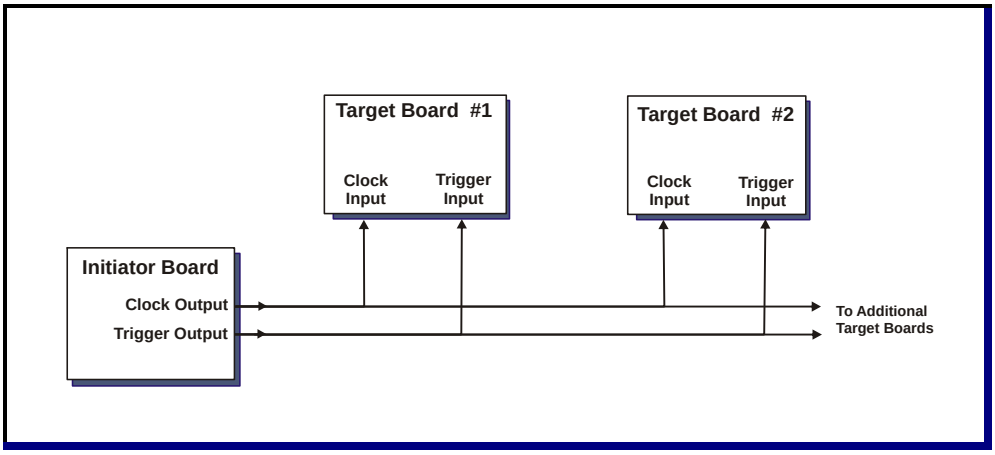

Figure 2.3-3. Multiboard Multidrop Synchronization

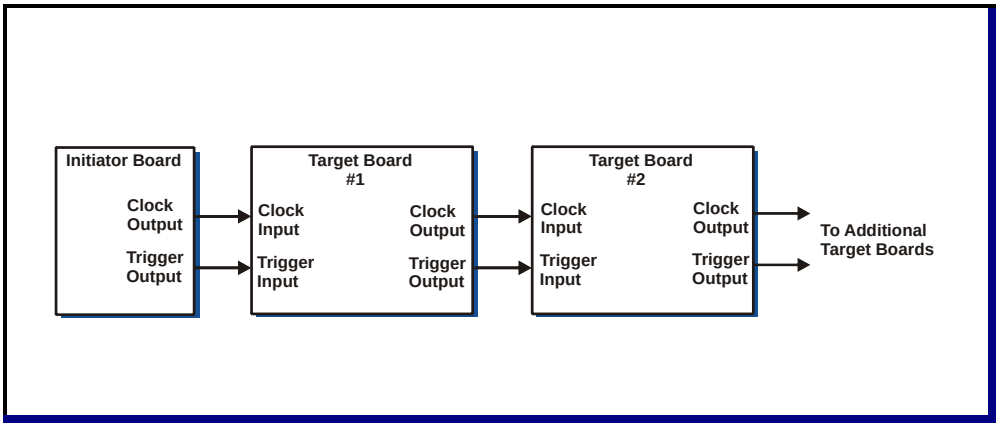

Figure 2.3-4. Multiboard Daisy-Chain Synchronization

The board that initiates the clock and trigger signals is software-designated as the **initiator**, and the clock and trigger receivers are designated as **targets**. For optimum reliability, the initiator and all targets all should reside in the same backplane. Clock and trigger signaling is software-selectable as either LVDS or standard TTL. ***LVDS signaling can extend the I/O signals beyond a single backplane, but is limited to the daisy-chain configuration.***

2.3.3 External Sync I/O

An initiator (Paragraph 2.3.2) can be replaced with an external source of synchronization signals if the following conventions are observed:

- Logic levels are selectable as either standard TTL or as LVDS. TTL Input loading is less than 0.2ma. Maximum output loading for TTL ouputs is 10mA.
- Clocks and triggers are edge-detected and are asserted LOW (i.e.: falling edge).
- Minimum input pulse width is 120ns.

External devices can be synchronized to an initiator board by recognizing a clock or trigger event as either a TTL or LVDS pulse with a minimum width of 150ns. Logic polarity is software-selectable for rising or falling edge assertion.

2.4 Maintenance

This product requires no scheduled maintenance other than periodic verification and possible adjustment of the range references. The optimum verification interval will vary with upon the specific application, but in most instances an interval of one year should be sufficient.

In the event of a suspected malfunction, all associated system parameters, such as power voltages, control bus integrity, and system interface signal levels, should be evaluated before troubleshooting of the board itself is attempted. A board that has been determined to be defective should be returned to the factory for detailed problem analysis and repair.

2.5 Reference Verification

All analog channels are calibrated to a single internal voltage reference by an embedded autocalibration utility. The voltage reference is scaled for each of three basic output ranges, and a separate adjustment is provided for each range. The procedure presented here describes the verification and adjustment of the range references.

2.5.1 Equipment Required

Table 2.5-1 lists the equipment required for verifying or adjusting the internal reference. Alternative equivalent equipment may be used.

Table 2.5-1. Reference Verification Equipment

Equipment Description	Manufacturer	Model
Digital Multimeter, 5-1/2 digit, 0.002% accuracy for DC voltage measurements at ±10 Volts. Input impedance 10 Megohms or greater.	Hewlett Packard	34401A
Host board with available PMC site	(Existing host)	---
Test cable; suitable for connecting the digital multimeter to the system I/O connector.	---	---

2.5.2 Verification and Adjustment

The following procedure describes the verification of the three internal range references. Adjustment of the references, if necessary, is performed with three internal trimmer that are located as shown in Figure 2.5-1.

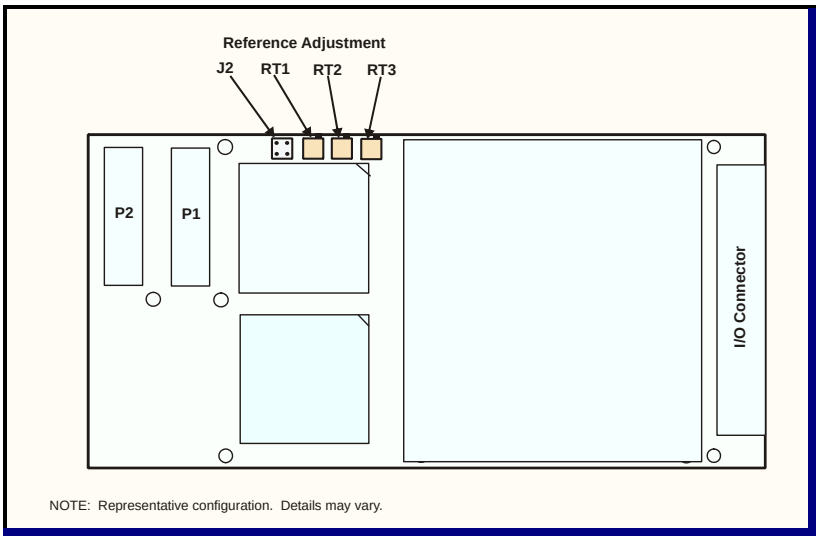

Figure 2.5-1. Reference Adjustment Access

This procedure assumes that the board under test is installed in an operational PMC host.

1. Connect the digital multimeter between Pins 3(+) and 4(-) in the J2 test connector.
2. If power has been removed from the board, apply power now. Wait at least 15 minutes after power is applied before proceeding.
3. Select the ±2.5V output range in the Output Configuration control register (Table 3.4-1).
4. For each output range listed in Table 2.5-2, select the same range in the Output Configuration register and verify that the voltage displayed by the multimeter conforms to the Range Reference indicated for the range. If a reference does not conform to the table, adjust the associated trimmer to obtain a nominal in-range value.
5. Verification and adjustment is completed. Remove all test connections.

Table 2.5-2. Range Reference Voltages

Output Range	Range Reference	Adjustment Trimmer
±2.5V	+2.47500VDC ±0.00020VDC	RT1
±5V	+4.95000VDC ±0.00040VDC	RT2
±10V	+9.99000VDC ±0.00070VDC	RT3

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SECTION 3.0

CONTROL SOFTWARE

3.1 Introduction

The PMC66-18AO8 is compatible with the PCI Local Bus specification Revision 2.3, and supports auto configuration at the time of power-up. A PLX™ PCI-9056 adapter controls the PCI interface. Configuration-space registers are initialized internally to support the location of the board on any 32-longword boundary in memory space. After initialization is completed, communication between the PCI bus and the local bus takes place through the control and data registers listed in Table 3.1-1. All data transfers are long-word D32. DMA access is supported for data transfers to the analog output data buffers. To ensure compatibility with subsequent controller revisions, reserved control bits should be written LOW (zero), and maintenance registers should not be modified.

Table 3.1-1. Control and Status Registers

OFFSET (Hex)	REGISTER	MODE	DEFAULT	PRIMARY FUNCTION	REF
0000	BOARD CONTROL	RW	2200 0000h	Board Control Register (BCR).	3.2
0004	DIGITAL I/O PORT	RW	0000 0X0Xh	Digital I/O port data.	3.12
0008-0010	(Reserved)	RO	0000 0000h	---	---
0014	SELFTEST CONFIGURATION	RW	0000 0000h	Selftest node selection.	3.14
0018	SELFTEST DATA BUFFER	RO	000X XXXXh	Selftest FIFO data buffer..	3.14
001C	AUXILIARY SYNC I/O CONTROL	RW	0000 0000h	Controls AUX Clock and Trigger I/O	3.18
0020-002C	(Reserved)	RO	0000 0000h	---	---
0030	PRIMARY STATUS	RW	0000 0000h	Principal status-flag register	3.15
0034	ASSEMBLY CONFIGURATION	RO	00XX XXXXh	Options and firmware revision.	3.17
0038	Autocal Values *	RW	0000 XXXXh	Autocal value readback.	---
003C	BUFFERED OUTPUT OPERATIONS	RW	0000 1400h	Buffered Analog Outputs Control	3.4
0040	OUTPUT BUFFER THRESHOLD	RW	0003 FFFEh	Output buffer status flag threshold.	3.5.5
0044	OUTPUT BUFFER SIZE	RO	0000 0000h	Number of data values in the output buffer.	3.5.5
0048	ANALOG OUTPUT BUFFER	WO	0000 0000h	Analog Output Data Buffer.	3.5
004C	RATE GENERATOR C	RW	0000 0180h	Rate-C generator divider; 24 bits.	3.7.1.2 3.11
0050	RATE GENERATOR D	RW	0000 2760h	Rate-D generator divider; 24 bits.	3.8.3 3.11
0054	OUTPUT CONFIGURATION	RW	0000 00FFh	Analog output configuration.	3.4
0056-007C	(Reserved)	---	---	---	---

* Maintenance register; Shown for reference only.

3.2 Board Control Register (BCR)

Most common board functions such as initialization and autocalibration are controlled through the board control register (BCR) shown in Table 3.2-1. Specific control bits are cleared automatically after the associated operations have been completed. Read-only status flags indicate the states of specific operational functions.

3.3 Configuration and Initialization

3.3.1 Board Configuration

During *board configuration*, initial values for both the PCI configuration registers and the internal control logic are extracted from internal nonvolatile read-only memory. This process is initiated by a PCI bus reset, and should be required only once after the initial application of power. While the PCI configuration registers are being loaded, the response to PCI target accesses is RETRY's. Configuration operations are executed in the sequence shown in Table 3.3-1.

3.3.2 Initialization

Internal control logic can be initialized without invoking a full reconfiguration by setting the INITIALIZE control bit HIGH in the BCR. This action initializes the internal logic, but does not affect the PCI configuration registers and does not reconfigure the internal control logic. Initialization requires 3 milliseconds or less for completion, and produces the following default conditions:

- The BCR is initialized; all register defaults are invoked. (Paragraph 3.3).
- All analog output channels are active. (3.4.1).
- Analog output range is ±2.5V. (3.4.2).
- Clock and trigger sources are internal. (3.7.1, 3.8.2),
- The analog output and selftest data buffers are reset to empty. (3.5.5, 3.14),
- Data coding is offset binary. (3.5.3).
- The Digital I/O port is configured as eight input lines. (3.12).
- The Hardware output configuration is single-ended. (3.4.4).
- Rate-C generator is adjusted to 105 kHz, and is disabled. (3.7.1.2).
- Rate-D generator is adjusted to 4 kHz, and is disabled. (3.8.3).
- Analog outputs are at midrange (zero). (3.4.2).

Table 3.2-1. Board Control Register (BCR)

Offset: 0000h **Default: 2200 0000h**

BIT	MODE [1]	DESIGNATION	DEF	DESCRIPTION	REF
D00	R/W	INITIATE SELFTEST [2]	0	Initiates a selftest cycle, in which data from the selected selftest measurement node is acquired.	3.14
D01	RO	SELFTEST DATA READY	0	LOW initially and during selftest data acquisition. HIGH when data acquisition is completed.	3.14
D02	RW	CLEAR SELFTEST BUFFER [2]	0	Clears (empties) the selftest data buffer	3.14
D03-D04	RW	(Reserved)	0	---	---
D05	RW	DIFFERENTIAL SYNC IO	0	Selects LVDS external sync I/O levels when HIGH.	2.3.3
D06-D17	RW	(Reserved)	0	---	---
D18	RW	SIMULTANEOUS OUTPUTS	0	When HIGH, all outputs update simultaneously in response to an output clock. When LOW, each output is updated immediately when new data is received.	3.7.2
D19	RW	(Reserved)	0	---	---
D20	RW	OUTPUT SW CLOCK [2,3]	0	Produces a single analog output clock. Overrides existing output clocking source.	3.7.1
D21	RW	ENABLE RATE-C GENERATOR	0	Enables the Rate-C generator for analog outputs.	3.7.1.2
D22	R/W	ENABLE RATE-D GENERATOR	0	Enables the Rate-D generator for analog outputs.	3.8.3
D23	R/W	OUTPUT SW TRIGGER [3]	0	Output Burst S/W Trigger. See also Table 3.4-2.	3.8.2
D24	RW	(Reserved)	0	---	---
D25	RW	OFFSET BINARY	1	Selects offset-binary analog I/O data format when HIGH, or two's complement when LOW.	3.5.3
D26-D27	RO	(Reserved)	0	---	---
D28	RW	AUTOCAL [2]	0	Initiates an autocalibration operation when asserted. Clears automatically upon completion,	3.7.1.2 3.11
D29	RO	AUTOCAL PASS	1	Set HIGH at reset or autocal initialization. A HIGH state after autocal confirms a successful calibration.	3.13
D30	RO	(Reserved)	0	---	---
D31	RW	INITIALIZE [2]	0	Initializes the board. Sets all register defaults.	

Notes: 1. RW = Read/Write, RO = Read-Only. 2. Clears automatically. 3. Duplicated elsewhere.

Table 3.3-1. Configuration Operations

Operation	Maximum Duration
PCI configuration registers are loaded from internal ROM	3 ms
Internal control logic is configured from internal ROM	300 ms
Internal control logic is initialized	3 ms

3.4 Output Configuration

The eight analog output channels are accessed through a dedicated 256 K-Sample analog output buffer. Once the outputs have been configured through the Output Configuration register (Table **3.4-1**), output operations are controlled through the BCR and the Buffered Operations register (Table **3.4-2**).

Table 3.4-1. Output Configuration Register

Offset: 0054h **Default: 0000 00FFh**

BIT	MODE	DESIGNATION	DEF	DESCRIPTION	REF
D00	RW	OUTPUT 00	1	Analog output Active Channel selection mask.	3.4.1
D01	RW	OUTPUT 01	1	HIGH to enable.	
D02	RW	OUTPUT 02	1		
D03	RW	OUTPUT 03	1		
D04	RW	OUTPUT 04	1	(D04-D07 are LOW in the 4-channel	
D05	RW	OUTPUT 05	1	configiuration.)	
D06	RW	OUTPUT 06	1		
D07	RW	OUTPUT 07	1		
D08-D10	RW	OUTPUT RANGE	0	Analog Output Range: 0 => ±2.5V. 1 => ±5V. 2 => ±10V 3-7 => (Reserved).	3.4.2
D11	RW	CLOCK AND TRIGGER OUT	0	Enables the Analog Output Clock and Trigger external outputs,	3.7.1 3.8.2
D12-D13	RW	CLOCK SOURCE	0	Analog Output clock source: 0 => Rate-C Generator. 1 => (Reserved) 2 => Analog Output External Clock input 3 => (Reserved).	3.7.1
D14-D15	RW	TRIGGER SOURCE	0	Analog Output trigger source: 0 => Rate-D Generator. 1 => (Reserved). 2 => Analog Output External Trigger input 3 => (Reserved).	3.8.2
D16	RW	DIFFERENTIAL CONFIG	0	Analog Output Configuration: 0 => Single-ended outputs. 1 => Differential outputs.	3.4.4
D17	RW	INVERT EXT SYNC *	0	Inverts the logic polarities of the external clock and trigger inputs and outputs.	3.7.1 3.8.2
D18	RW	Maintenance Utility **	0	---	---
D19-D31	RO	(Reserved)	0000h	---	---

* Does not affect the Auxiliary Sync I/O logic polarities (3.18).

** Maintenance control bit. Shown for reference only. Always write LOW.

Table 3.4-2. Buffered Output Operations Register

Offset: 003Ch **Default: 0000_1400h**

BIT	MODE	DESIGNATION	DEF	DESCRIPTION	REF
D00-D04	R/W	(Reserved)	0h	---	---
D05	R/W	ENABLE OUTPUT CLOCKING	0	Enables output clocking when HIGH. Disables clocking when LOW. Default is LOW (clocking disabled).	3.7
D06	RO	OUTPUT CLOCK READY	0	Indicates when HIGH that an output clock will be accepted. If LOW, indicates that the output will not respond to a clock.	3.7
D07	R/W	OUTPUT SW CLOCK *	0	Produces a single output clock event when asserted. Independent of clocking mode. Duplicated in the BCR.	3.7.1
D08	R/W	CIRCULAR BUFFER	0	Selects circular buffer configuration if HIGH, or open self-flushing buffer configuration if LOW. Access for loading new data into the circular buffer must be requested by asserting LOAD REQUEST. Default is LOW; i.e. open buffer.	3.5.6 3.5.7
D09	R/W	LOAD REQUEST *	0	When set HIGH, requests loading access to the circular buffer. Initializes LOW.	3.6.3
D10	RO	LOAD READY	1	Set HIGH when the frame index passes through zero, if both CIRCULAR BUFFER and LOAD REQUEST are HIGH. When HIGH, indicates that the circular buffer is ready to accept new data. Available also in the PSR. Defaults HIGH.	3.6.3
D11	R/W	CLEAR OUTPUT BUFFER *	0	Resets the output buffer to empty.	3.5.5
D12	RO	AO BUFFER EMPTY	1	Indicates the analog output buffer is empty.	3.5.5
D13	RO	OUTPUT BUFFER THRESHOLD	0	Analog output buffer threshold flag. Duplicated in the AO Buffer Threshold register.	3.5.5
D14	RO	(Reserved)	0	Inactive; Returns zero.	---
D15	RO	AO BUFFER FULL	0	Indicates the output buffer is full.	3.5.5
D16	R/W	AO BUFFER OVERFLOW	0	Set HIGH when data is written to a full buffer. **	3.5.5
D17	R/W	FRAME OVERFLOW	0	Set HIGH when data is written to a closed buffer. **	3.6.3
D18	RO	BURST READY	0	If HIGH, indicates that a burst trigger will be accepted. If LOW, indicates that the output will not respond to a trigger.	3.8.2
D19	R/W	ENABLE OUTPUT BURST	0	Enables analog output burst operation.	3.8.1
D20	R/W	OUTPUT SW TRIGGER *	0	Produces a single output trigger event when asserted. Clears LOW automatically when the triggered burst is completed. Independent of triggering mode. Duplicated in the BCR.	3.8.2
D21-D31	RO	(Reserved)	0	Inactive. Returns all-zero.	---

* Clears LOW automatically when operation is completed.
** Remains HIGH until cleared by a direct write as LOW, or by initialization.

3.4.1 Channel Selection

An output channel is selected as *active* by setting the corresponding OUTPUT_XX selection bit HIGH in the Output Configuration register. A channel is deselected to the *inactive* state by clearing the corresponding selection bit.

An active *channel group* consists of a single set of output values for all active channels. Only active output channels receive data from the output buffer. A channel that is deselected to the inactive state retains the last value that was received while the channel was still active. During initialization, all channels are designated as active and are set to an approximately zero output level.

3.4.2 Voltage Range Selection

An output voltage range of ±10V, ±5V or ±2.5V is assigned by the OUTPUT RANGE control field in the Output Configuration register. The default output range is ±2.5V, and all ***outputs initialize to midrange (zero)***.

For maximum accuracy, autocalibration should be performed after a new output range is selected.

3.4.3 Clock and Trigger Sources

The clock and trigger source fields determine the origins of the analog output clock and trigger functions, and are described later in Sections **3.7.1** and **3.8.2**, respectively.

3.4.4 Hardware Configuration

The analog outputs can be configured for either single-ended (default configuration) or balanced-differential operation, as selected in the DIFFERENTIAL CONFIG control field, and must agree with the system wiring configuration (Section **2.3.1.1**).

3.5 Output Buffer

Analog output data from the PCI bus flows directly into the 256 K-sample analog output FIFO data buffer (Table **3.5-1**). From the buffer, the data passes through a short formatting pipeline to the analog output DAC channels.

NOTE: The output buffer capacity of 256 K-Samples is distributed among all active output channels. The capacity in samples-per-channel is:

Sample Capacity per Channel = 256K / Number of active channels.

3.5.1 Data Frame

A *data frame* consists of an integral number of channel groups. For triggered bursts, or for function concatenation, the last active channel in the last channel group is designated with an *end-of-frame* (EOF) flag. The EOF designation is applied by setting the EOF flag HIGH when loading the last channel value into the buffer. Thereafter, the EOF flag follows the last channel value through the buffer.

Table 3.5-1. Analog Output Buffer

Offset: 0048h **Default: N/A (Write-Only; Returns all-zero)**

BIT	MODE*	DESIGNATION	DESCRIPTION
D00	WO	DATA 00	Least significant data bit
D01-D16	WO	DATA 01 - DATA 16	Intermediate data bits
D17	WO	DATA 17	Most significant data bit
D18	WO	EOF FLAG	End-of-frame (EOF) flag.
D19-D31	WO	---	(Inactive)

* WO indicates write-only access. Read-access returns all-zero value.

3.5.2 Output Data Format

Analog output data values are written in 32-bit Lword-serial sequence from the PCI bus to the Analog Output Buffer. Bits D17..0 represent the output data value. Bit D18 designates the last value in a data frame, and is the end-of-frame (EOF) flag. The output buffer appears to the PCI bus as a 32-Bit single register, and a read-access to this register returns an all-zero value.

3.5.3 Output Data Coding

Analog output data is arranged as 18 active right-justified data bits with the coding conventions shown in Figure **3.5-1**. The default format is offset binary. Two's complement format is selected by clearing the OFFSET BINARY control bit LOW in the BCR. Unless indicated otherwise, offset binary coding is assumed throughout this document.

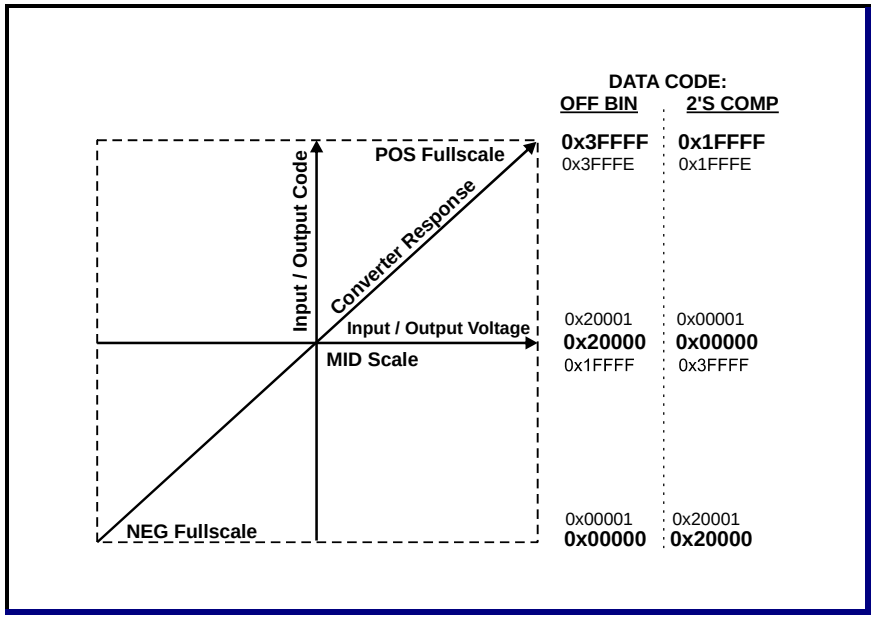

Figure 3.5-1. Analog Data Coding Formats; 18 Bit Data

3.5.4 Buffer Loading

Channel data values are loaded into the output buffer in ascending order of the active channels. The channel groups are loaded contiguously, beginning with the first group to be transferred to the outputs, and proceeding sequentially to the last group. Figure 3.5-2 illustrates a loading example that implements two output channels, with 100 values per channel. Each channel group in this example consists of active channels 0 and 5.

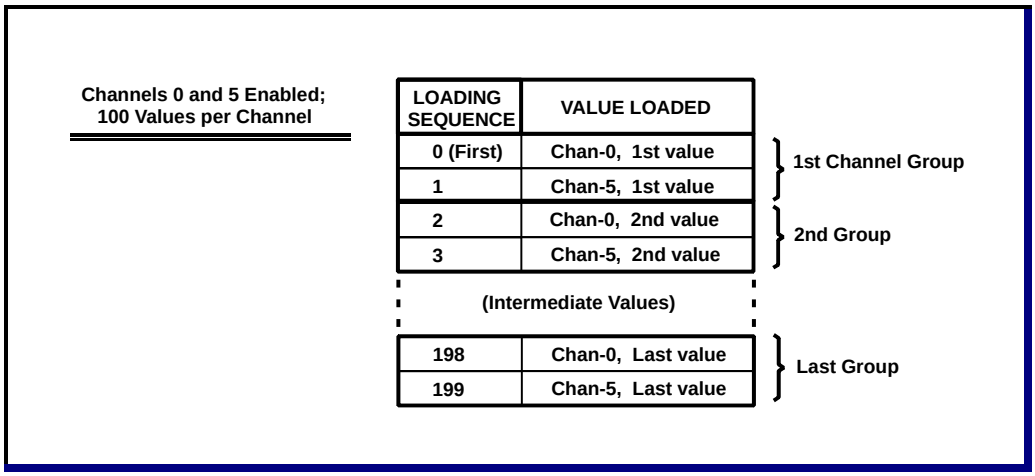

Figure 3.5-2. Typical Buffer Loading Sequence

NOTE: Data can be loaded from the PCI bus to the output buffer only if the buffer is open; that is, not circular (3.5-7).

3.5.5 Output Buffer Control

The Buffered Output Operations register (Table 3.4-2) controls and monitors the flow of data through the analog output data buffer. Asserting the CLEAR OUTPUT BUFFER control bit HIGH clears, or empties, the buffer.

The AO BUFFER OVERFLOW flag is set HIGH if data is written to a full buffer, and the FRAME OVERFLOW flag indicates that an attempt was made to write data to a closed buffer. Both flags indicate data loss. Each of these flags, once set, remains HIGH until written LOW directly from the bus, or by initialization .

The AO BUFFER EMPTY flag indicates that the buffer contains no output data. The AO BUFFER FULL flag is asserted when the buffer is full. Data written to a full output buffer is discarded.

The Output Buffer Size register shown in Table 3.5-2 contains the number of output data values present in the buffer, and is updated continuously.

Table 3.5-2. Output Buffer Size Register

Offset: 0044h **Default: 0000 0000h**

DATA BIT	MODE*	DESIGNATION	DEF	DESCRIPTION
D00-D18	RO	BUFFER SIZE	0 0000h	Number of values in the output buffer
D19-D31	RO	(Inactive)	0	---

The Output Buffer Threshold register (Table 3.5-3) specifies the buffer size value above which the OUTPUT BUFFER THRESHOLD FLAG is asserted HIGH. This status flag is duplicated in the Buffered Output Operations register.

Table 3.5-3. Output Buffer Threshold Register

Offset: 0040h **Default: 0003 FFFEh**

BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00-D18	RW	OUTPUT BUFFER THRESHOLD	3 FFFEh	Specifies the number of values in the output buffer, above which the threshold flag is asserted HIGH.
D19	RO	(Reserved)	0	---
D20	RO	OUTPUT BUFFER THRESHOLD FLAG	0	HIGH when the number of values in the output buffer *exceeds* the specified buffer threshold.
D21-D31	RO	(Reserved)	0	---

3.5.6 Open Buffer

If the CIRCULAR BUFFER control bit is LOW in the buffer operations register, the output buffer operates in the open mode. Data in an open buffer is discarded as it is used. Consequently, the buffer is self-flushing, and will empty itself unless it is replenished from the PCI bus. This mode of operation permits the continuous flow of data from the PCI bus to the analog outputs.

The open-buffer configuration also can be used to produce a one-shot waveform, provided the particular waveform is to be used only once. Figure 3.5-3 illustrates the movement of a single data frame through an open buffer.

3.5.7 Circular Buffer

Data in a circular (closed) buffer is retained indefinitely. This configuration generally is implemented to produce either periodic waveforms of constant frequency, or one-shot transient waveforms that will be used repeatedly but not necessarily periodically. While closed, the buffer is not accessible from the PCI bus.

In Figure 3.5-4 a single data frame is loaded into the buffer. The buffer is then closed (CIRCULAR BUFFER set HIGH) and clocking is enabled. The data frame subsequently circulates in the buffer while passing data values to the output channels.

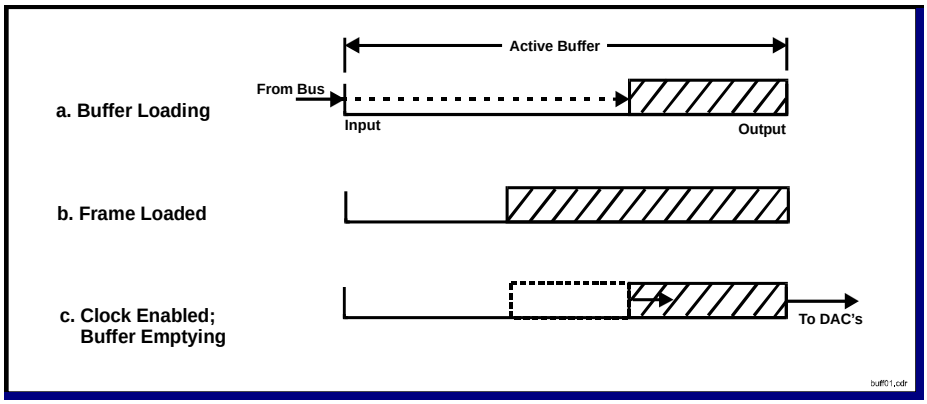

Figure 3.5-3. Open Buffer Data Flow

An end-of-frame (EOF) flag identifies the end-point, or last value in a data frame, and is set HIGH when the last value is loaded. Multiple contiguous burst functions, or frames, can reside in the buffer simultaneously.

NOTE: Disable output clocking before loading the buffer for circular operation.

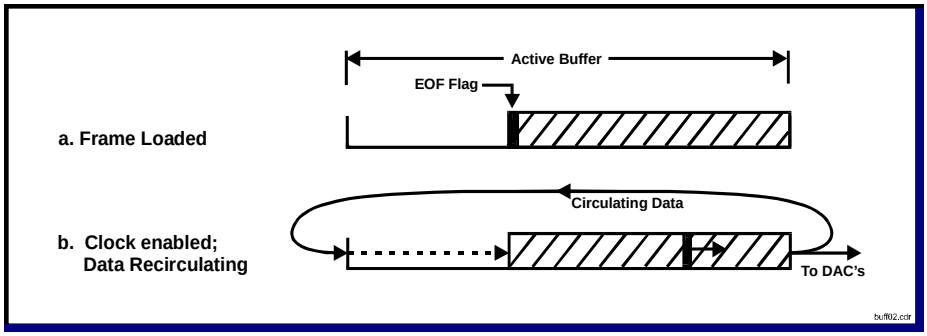

Figure 3.5-4. Circular Buffer Data Flow

3.6 Function Generation

3.6.1 Periodic and One-Shot Functions

Periodic waveforms are produced when the buffer is configured for continuous clocking and circular operation. In this mode, the contents of the buffer are scanned continuously as long as clocking is enabled and a clock is present. The data frame is recirculated through the buffer repeatedly.

If triggered-burst sampling is used in conjunction with a circular buffer, a *one-shot waveform* is produced that contains all values within a single data frame. The triggered burst is initiated by a software or hardware trigger, and terminates automatically when the end-of-frame (EOF) flag is encountered. Because the buffer is circular, the waveform is retained in the buffer and can be reproduced repeatedly by subsequent triggers.

3.6.2 Multiple Functions

When multiple functions are loaded into the buffer as contiguous data frames, and if triggered-burst sampling is selected, the functions will be generated sequentially in response to a series of burst triggers. If the buffer is open, the functions are flushed from the buffer as they are clocked to the analog outputs. However, if the buffer is closed (circular), the functions are retained in the buffer, and the series of functions is repeated indefinitely. .

3.6.3 Function Sequencing (Concatenation)

A new function (data frame) can be concatenated to the end of an existing function in a circular buffer, while the existing function is being flushed from the buffer. During this operation, the existing function is flushed from the buffer as it is clocked to the outputs, and is replaced by the new function. When the last value of the existing function is clocked out of the buffer, the buffer closes and the new function seamlessly begins circulating in the buffer and producing an output.

Introduction of a new function commences by setting the LOAD REQUEST flag HIGH in the buffered output operations register, and by then waiting for the LOAD READY flag to be asserted. (In effect, LOAD REQUEST is an "interrupt request" to the buffer). The LOAD READY flag indicates that the buffer has opened, and that the existing function is being flushed from the buffer, beginning with the first value in the function's data frame.

After LOAD READY goes HIGH, the new function is written to the buffer and is terminated with an EOF flag attached to the final value. When the last value in the original function is clocked from the buffer, the accompanying EOF flag causes the buffer to close, and clears both the LOAD READY flag and the LOAD REQUEST control bit. Notice that the loading of the new function into the buffer must be completed before the existing function terminates.

In Figure 3.5-5, an existing function is replaced by a new function while the existing ('old') function is flushed from the buffer.

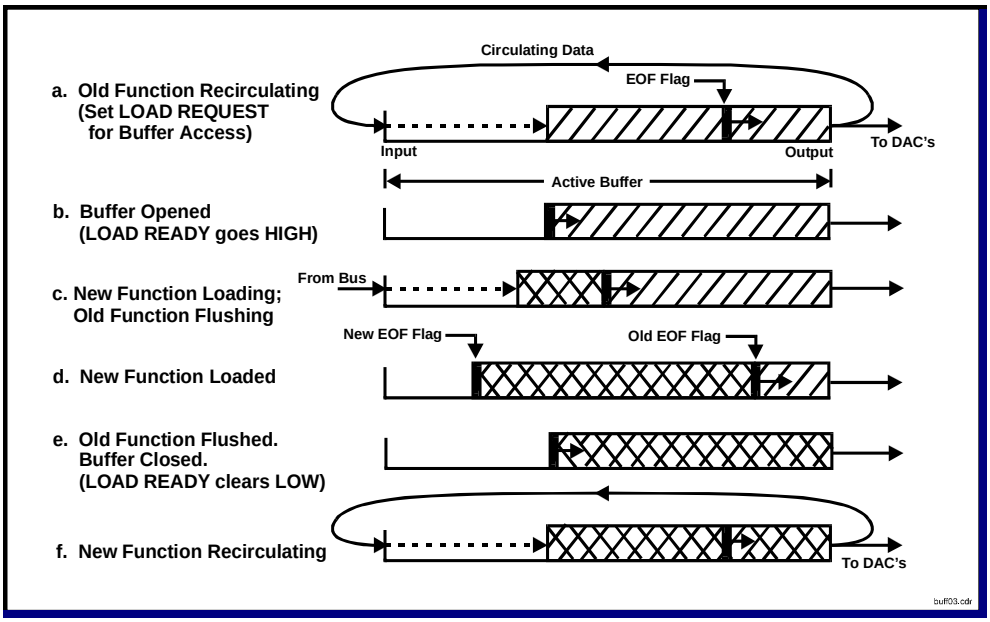

Figure 3.5-5. Function Sequencing (Concatenation)

NOTE: If the loading of a new function extends beyond the LOAD-READY interval, the FRAME OVERFLOW flag is set HIGH in the Buffer Operations register, indicating data loss. Once set, this flag remains HIGH until written LOW directly from the bus, or by initialization

After loading the new function, allow the LOAD REQUEST control bit to be cleared automatically. This bit should not be cleared from the PCI bus.

3.7 Output Clocking

Each occurrence of the output clock updates either one or all of the active output channels, depending on whether sequential or simultaneous clocking is selected in the BCR.

Output clocking is enabled by setting the ENABLE OUTPUT CLOCKING control bit HIGH in the Buffered Output Operations register and enabling the associated clock source. The OUTPUT CLOCK READY status bit indicates that an output clock will be accepted. This status bit is LOW during reset operations or autocalibration.

3.7.1 Clock Source

The source of the analog output clock is controlled by the CLOCK SOURCE control field in the Output Configuration register, and the default source is the internal Rate-C generator. A software clock can be applied at any time by setting the OUTPUT SW CLOCK control bit HIGH in either the Buffered Output Operations register or the BCR. This bit overrides the existing CLOCK SOURCE selection, and clears automatically.

If the CLOCK AND TRIGGER OUT control bit is set HIGH in the Output Configuration register, the CLOCK OUTPUT and TRIGGER OUTPUT pins in the I/O connector each generates an output pulse when the corresponding internal clock or trigger occurs. If this bit is LOW (default), the CLOCK OUTPUT and TRIGGER OUTPUT pins produce no output.

3.7.1.1 External Clock

The external clock source at the CLOCK INPUT system I/O connector input can have any frequency up to the maximum value specified for the output clocking rate. When the external clock source is selected, sampling occurs on a HIGH-to-LOW transition of the external analog output clock.

NOTE: Logic polarities of all external clock and trigger inputs and outputs are inverted if the INVERT EXT SYNC control bit is HIGH in the Output Configuration register.

3.7.1.2 Internal Clocking Rate Generator

The internal Rate-C generator provides an output clocking rate that is adjustable as described in Paragraph 3.11. The Rate-C generator is enabled by setting the ENABLE RATE-C GENERATOR control bit HIGH in the BCR.

3.7.2 Simultaneous Clocking

Simultaneous sampling is selected by setting the SIMULTANEOUS OUTPUTS control bit HIGH in the BCR. If simultaneous sampling is selected, the analog values in each successive channel group appear simultaneously at the outputs, with minimum time-skew between channels. Upon each occurrence of the sampling clock, an entire active channel group is transferred from the output buffer, and all outputs are updated simultaneously. In this mode, the effective sample rate for each channel equals the output clocking rate.

3.7.3 Sequential Operation

Sequential sampling is selected when the SIMULTANEOUS OUTPUTS control bit in the board control register is LOW. At each clock occurrence in sequential operation, a single channel value is transferred from the buffer to the associated output channel, and the channel is updated immediately. Channel values are read from the buffer beginning with the lowest-numbered active channel in a channel group, and proceeding upward through the highest-numbered active channel. When operating in this mode, the effective sample rate for each channel equals the output clocking rate *divided by the number of active channels*.

3.8 Clocking Mode

3.8.1 Continuous Clocking

If the ENABLE OUTPUT BURST control bit in the Buffered Output Operations register is LOW (default), the *continuous clocking* mode is selected and data is transferred continuously from the buffer to the analog outputs, assuming that the buffer is not empty and that an output clock is present. EOF flags are ignored when operating in this mode.

3.8.2 Data Bursts

If the ENABLE OUTPUT BURST control bit in the Buffered Output Operations register is HIGH, burst operation is selected. During a *triggered output burs*t, data is transferred continuously from the output buffer to the analog outputs until either the ***buffer goes empty, or an end-of-frame (EOF) flag is encountered***. In the triggered-burst clocking mode, an internal or external output trigger initiates the transfer of data from the output buffer to the output channels. The BURST READY status flag indicates that a burst trigger will be accepted, and is LOW during each burst.

NOTE: Logic polarities of all external clock and trigger inputs and outputs are inverted if the INVERT EXT SYNC control bit is HIGH in the Output Configuration register.

The source of the output trigger is controlled by the TRIGGER SOURCE control field in the Output Configuration register, and the default source is the internal Rate-D generator. A software trigger can be applied at any time by setting the OUTPUT S/W TRIGGER control bit HIGH in either the Buffer Operations register or the BCR. This bit overrides the existing CLOCK TRIGGER selection, and clears automatically. The OUTPUT SW TRIGGER bit goes HIGH during the burst, and clears automatically when the burst is completed.

If the CLOCK AND TRIGGER OUT control bit is set HIGH in the output configuration register, the TRIGGER OUTPUT signal in the I/O connector produces an output pulse when the corresponding internal clock or trigger occurs. If this bit is LOW (default), TRIGGER OUTPUT produces no output.

Multiple burst functions can exist simultaneously within the buffer if the end-of-frame (EOF) flag is used (3.5-2). The EOF flag defines the last output value in each data burst. After a burst is triggered, data values from the buffer are clocked to the analog outputs at the selected sample rate until the EOF flag is encountered. The burst then terminates, and clocking of the buffer ceases until a subsequent trigger occurs.

3.8.3 Internal Trigger Rate Generator

The internal Rate-D generator provides an internal trigger that is adjustable as described in Paragraph 3.11. The Rate-D generator is enabled by setting the ENABLE RATE-D GENERATOR control bit HIGH in the BCR.

3.9 Multiboard Synchronization

Boards that are configured for *synchronous clocking* update their outputs simultaneously in response to a common *clock* signal. Boards that are configured for *synchronous burst triggering* initiate data bursts simultaneously in response to a common *trigger* signal. Multiple boards can be arranged to operate with:

a. Independent clocking and burst triggering
b. Synchronous burst triggering (Common burst trigger)
c. Synchronous clocking (Common DAC clock)
d. Synchronous clocking and burst triggering (Common trigger and DAC clock).

As many as four boards can be synchronized together when connected in the Multidrop configuration (Figure 2.3-3) or any number can be synchronized together in the Daisy-Chain configuration (Figure 2.3-4).

NOTE: For multiboard synchronization, an analog output clock or trigger initiator must have the CLOCK AND TRIGGER OUT control bit asserted. Likewise, all targets that drive other targets in a daisy-chain multiboard configuration must have this bit asserted.

3.10 Buffer DMA Operation

DMA transfers to the analog output buffer are supported with the board operating as a bus master. Table 3.10-1 illustrates a typical PCI register configuration that controls a non-chaining, non-incrementing '***block-mode'*** Channel-0 DMA transfer, in which a PCI interrupt is generated when the transfer has been completed. Bit 02 (0000 0004h) in the PCI Command register must be set HIGH to select the bus mastering mode. Refer to a PCI-9056 reference manual for a detailed description of these registers. DMA Channels 00 and 01 are available.

For most applications, the DMA Command Status register would be initialized to the value 0000 0001h, and then changed to 0000 0003h to initiate a transfer. For DMA transfers from the selftest data buffer (3.14), the DMA Descriptor Counter register value must be modified to 0000 000Ah, to specify a transfer direction from the Local bus to the PCI bus, and the DMA Local Address must be changed to 0018h.

Table 3.10-1. Typical Output Buffer DMA Register Configuration

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Analog Output Buffer local address (Analog output buffer)	0000 0048h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction; PCI bus to Local bus (Analog outputs)	0000 0000h
A8h	DMA Command Status	Command and Status Register	0000 0001h 0000 0003h (See Text)

* Determined by specific transfer requirements.

3.11 Rate Generators

Two rate generators supply independent frequencies for output clocking and burst control (Table 3.11-1). The Rate-C Generator generates an internal clock for the analog outputs. The Rate-D generator controls output burst triggering.

Each generator is enabled by the associated ENABLE RATE-C/D GENERATOR control bit in the BCR. The generators are disabled when these bits are LOW.

Table 3.11-1. Rate Generator Registers (Rate-C,D)

Offset: 004Ch (Rate-C), 0050h (Rate-D) **Default: 0000 0180 (Rate-C), 0000 2760h (Rate-D)**

DATA BIT	MODE*	DESIGNATION	DEFAULT	DESCRIPTION
D00-D23	R/W	Ndiv	---	Rate generator frequency control
D24-D31	RO	(Inactive)	0	---

* R/W = Read/Write, RO = Read-Only.

The frequency **Fgen** (Table 3.11-2) of each generator is calculated as:

Fgen = Fclk / Ndiv,

where **Fclk** is the master clock frequency for the board, and **Ndiv** is the value written to the Rate-C/D Generator register. **Fgen** and **Fclk** are both expressed in the same frequency units. **Fclk** is assumed here to be 40.320 MHz, but custom frequencies are available. If the master clock is provided with a custom frequency, **Fclk** equals the custom frequency. For an external clock or trigger input frequency, **Fclk** equals the external frequency, ***Fgen should not exceed the maximum clocking rate listed in the product specification.***

Table 3.11-2. Typical Rate Generator Frequency Selection

Ndiv		FREQUENCY Fgen (40.320 MHz Master Clock)*
(Dec)	(Hex)	(Hz)
126	007E	320,000
127	007F	317,480
128	0080	315,000
---	---	Fgen (Hz) = Fclk (Hz) / Ndiv **

* ±0.003 percent. ** Fclk = master clock frequency; e.g.: 40.32MHz.

The maximum recommended analog output clocking rate is 500,000 clocks per second.

3.12 Digital I/O Port

The digital I/O port consists of eight bidirectional TTL I/O lines, with the corresponding data bits shown in Table 3.12-1. The DIO lines are arranged as two 4-bit nibbles, with the direction of each nibble controlled independently of the other. A nibble is an input to the board if the associated DIO 00 03 OUTPUT control bit is LOW, or is an output if the bit is HIGH. Logic polarities are retained, with a HIGH level at a connector pin associated with a HIGH level for the corresponding bit in the register. All digital I/O lines default to inputs.

Table 3.12-1. Digital I/O Port Register

Offset: 0004h **Default: 0000 0X0Xh**

DATA BIT	MODE*	DESIGNATION	DEFAULT	DESCRIPTION
D00	RW	DIO 00 DATA	X	Digital I/O Data; Bits 00-03
D01	RW	DIO 01 DATA	X	
D02	RW	DIO 02 DATA	X	
D03	RW	DIO 03 DATA	X	
D04-D06	RW	(Reserved)	0h	---
D07	R/W	DIO 00_03 OUTPUT	0	DATA 00-03 direction control; High for output.
D08	RW	DIO 04 DATA	X	Digital I/O Data; Bits 04-07
D09	RW	DIO 05 DATA	X	
D10	RW	DIO 06 DATA	X	
D11	RW	DIO 07 DATA	X	
D12-D14	RW	(Reserved)	0h	---
D15	RW	DIO 04_07 OUTPUT	0	DATA 04-07 direction control; High for output.
D16-D31	RO	(Reserved)	0h	Read back as all-zero.

3.13 Autocalibration

To obtain maximum measurement accuracy, autocalibration should be performed after:

- Power warmup,
- PCI bus reset,
- Analog output range change.
- Changing the output configuration between single-ended and differential.

The analog outputs are autocalibrated on the selected output range.

NOTE: Analog outputs are active during autocalibration, and can vary between positive and negative fullscale during the calibration sequence.

Autocalibration is invoked by setting the AUTOCAL control bit HIGH in the BCR. The control bit returns LOW automatically at the end of autocalibration. Autocalibration can be invoked at any time, and has a maximum duration of eight seconds. Completion of the operation can be detected either by monitoring the "Autocal completed" status flag in the Primary Status register (Table 3.15-1), or by simply waiting for a time interval sufficient to ensure that autocalibration has been completed.

To compensate for component aging, and to minimize the effects of temperature on accuracy, the autocalibration function determines the optimum calibration values for current conditions, and stores the necessary correction values in internal volatile memory. If a board is defective, the autocalibration process may be unable to successfully calibrate all outputs. If this situation occurs, the AUTOCAL PASS status bit in the BCR is cleared LOW at the end of the autocalibration interval, and remains LOW until a subsequent initialization or autocalibration occurs. AUTOCAL PASS is initialized HIGH, and remains HIGH unless an autocalibration failure occurs.

3.14 Selftest

A local selftest network permits various analog nodes to be monitored with an internal 18-Bit A/D converter. During each selftest acquisition cycle, 128 measurements are acquired from a selected node and stored in a FIFO Selftest Data buffer. The buffer supports block-mode DMA transfers (3.10).

The measurement node is selected with the SELFTEST MEASUREMENT NODE control field in the Selftest Configuration register shown in Table 3.14-1. A selftest acquisition cycle is initiated by setting the INITIATE SELFTEST control bit HIGH in the BCR. The INITIATE SELFTEST bit clears automatically.

NOTE: Before initiating a selftest acquisition cycle, a settling delay of 50 milliseconds or more should be inserted after the selection of a measurement node, or after modifying the output level of a selected analog output channel, whichever occurs *last*. The delay is not required for subsequent acquisition cycles from the same node.

Table 3.14-1. Selftest Configuration Register

Offset: 0014h **Default: 0000 0000h**

BIT	MODE	DESIGNATION	DEFAULT	DESCRIPTION
D00-D03	RW	SELFTEST MEASUREMENT NODE	0h	Measurement Node: 0 => ZERO Selftest. 1 => +VREF Selftest. 2-7 => (Reserved). 8 => Output Channel 00 * 9 => Output Channel 01 10 => Output Channel 02 11 => Output Channel 03 12 => Output Channel 04 13 => Output Channel 05 14 => Output Channel 06 15 => Output Channel 07
D04-D31	RO	(Reserved)	0h	---

* Differential/single-ended measurement configuration is selected automatically to conform to the selected analog output configuration.

When the acquisition cycle is completed, the SELFTEST DATA READY flag in the BCR goes HIGH, indicating that the Selftest Data Buffer (Table 3.14-2) contains the preselected number of measurements from the selected node. The SELFTEST DATA READY, which defaults LOW, returns LOW also when data is read from the buffer or when the buffer is cleared. Assertion of the SELFTEST DATA READY status bit can be selected as an event in the Primary Status Register (3.15).

The selftest ADC is sampled at 50KSPS during the acquisition cycle, so each 128-sample cycle has a duration of approximately 2.6 milliseconds.

Table 3.14-2. Selftest Data Buffer

Offset: 0018h **Default: 000X XXXXh**

BIT	MODE*	DESIGNATION	DESCRIPTION
D00	RO	DATA 00	Least significant data bit
D01-D16	RO	DATA 01 - DATA 16	Intermediate data bits
D17	RO	DATA 17	Most significant data bit
D18-D31	RO	(Reserved)	---

* WO indicates write-only access. Read-access returns all-zero value.

The selftest data buffer is cleared (emptied) during initialization, and also can be cleared by setting the CLEAR SELFTEST BUFFER control bit HIGH in the BCR. The CLEAR SELFTEST BUFFER control bit clears automatically.

NOTE: Inherent selftest accuracy is: ±0.00008*Vsig ±0.000015*Vfsr ±0.1mV.

E.g.: for a +5V signal on the ±10V range:

Accuracy = ±0.00008*5V ±0.000015*20V ±0.1mV = ±0.80mV.

The maximum error experienced in selftest measurements should equal the output accuracy listed in the product specification, plus the selftest error as calculated here.

3.15 Primary Status Register

Critical status flags are consolidated into a single Primary Status register (Table 3.15-1), which is organized into a selection field and a response field. A response status bit is asserted if the selected event occurs after it has been selected. The response bit remains high until it is cleared from the PCI bus, either by clearing the response bit *or by clearing the associated selection bit*.

NOTE: Response status bits can *only* be cleared LOW from the PCI bus. A "one" written to a response bit is ignored.

The response bit for an event indicated as 'edge-detected' is set HIGH when the event transitions from false to true. Once asserted, an edge-detected response bit remains in that state until cleared from the bus, regardless of subsequent changes in the associated event state.

Real-time access to an edge-detected signal is available by reading the source of the edge-driven response bit (e.g.: BURST READY in the Buffered Operations register is the signal that drives the "Analog Output Burst Ready" response bit in the PSR).

Table 3.15-1 Primary Status Register

Offset: 0x0030 **Default: 0000 0000h**

SELECTION BIT [1]	CRITICAL EVENT	RESPONSE BIT [2]	REFERENCE PARAGRAPH
D00	Autocal completed [3]	D16	3.13
D01	(Reserved)	D17	---
D02	(Reserved)	D18	---
D03	(Reserved)	D19	---
D04	(Reserved)	D20	---
D05	Selftest Data Ready [3]	D21	3.14
D06	(Reserved)	D22	---
D07	(Reserved)	D23	---
D08	Digital I/O Port DIO 00 LOW-to-HIGH transition [3]	D24	3.12
D09	Output Buffer threshold flag HIGH-to-LOW transition [3]	D25	3.5.5
D10	Output Buffer threshold flag LOW-to-HIGH transition [3]	D26	3.5.5
D11	Output Load-Ready Flag HIGH-to-LOW transition [3]	D27	3.6.3
D12	Output Load-Ready Flag LOW-to-HIGH transition [3]	D28	3.6.3
D13	Analog Output Burst Ready [3]	D29	3.8.2
D14	Output Buffer Overflow or Frame Overflow [3]	D30	3.5.5
D15	(Reserved)	D31	---

1. Event selection. Enables assertion of the corresponding response bit when the selected event occurs.
2. Event response. Asserted HIGH when a selected event occurs. Edge-detected response bits remain HIGH until cleared LOW.
3. Edge-detected event.

3.16 Buffered Analog Output Application Examples

Specific operating modes and procedures vary widely according to the unique requirements of each application. The examples presented in this section illustrate basic operating modes, and can be modified or combined for more complex operations.

References to *functions* in these examples generally apply to a single output channel for simplicity of explanation. However, each active channel represents an independent set of function values, and all channels share a common output clock.

Table 3.16-1. Summary of Operation Examples

Operation Example	Description
Sequential Direct Outputs	Each value written to the output data buffer updates the associated analog output channel when clocked, independently of the other channels.
Simultaneous Direct Outputs	Data values accumulate in the output data buffer until an entire channel group has been loaded. When the last channel is loaded, all active output channels update simultaneously when clocked.
Continuous Function	An extension of Simultaneous Direct Outputs, in which the buffer is not allowed to become either empty or full.
Periodic Function	A single function is generated repeatedly in each active channel.
Function Burst	One or more functions are generated as discrete data bursts. The burst cycle is repeated indefinitely if the circular-buffer mode is selected.
Function Sequencing	An existing active function is replaced seamlessly by a new function.

Each of the examples in this section assumes that the initial operations listed in Table 3.16-2 have already been performed.

Table 3.16-2. Initial Operations

Operation	Default Value	Applicable Paragraph
The board has been reset or initialized.	---	3.3.2
The active channel group has been defined .	All channels active	????
The required output coding has been selected.	Offset binary	????

The remaining operational parameters are assumed to be in the following *default* states initially:

Parameter	Default
Buffer mode:	Open
Buffer status:	Empty
Sample rate:	105KSPS
Clocking mode:	Sequential

Parameter	Default
Clock source:	Rate-C Generator
Clock status:	Disabled
Trigger source:	Rate-D Generator
Trigger status:	Disabled

3.16-1 Sequential Direct Outputs

Table 3.16-3. Sequential Direct Outputs Example

Operation	PCI Bus Action	Board Response
Select the clocking rate.	Write the required sample clocking rate to the Rate-C generator control register.	The output clocking rate is selected.
Enable clocking	Set the ENABLE OUTPUT CLOCKING control bit HIGH in the buffer operations register. Set the ENABLE RATE-C GENERATOR control bit HIGH in the BCR.	Clocking is enabled at the default rate.
Load the output value for the first active channel.	Write the first value to the output data buffer.	Output value appears immediately (when clocked) at the analog output.
Load the output values for the remaining active channels.	Write the remaining active channel values to the output data buffer.	Remaining active analog outputs are updated in ascending sequence.
Repeat the above operations for subsequent channel groups.	Continue to write output values to the output data buffer.	Each value written to the buffer is transferred immediately to the associated analog output when clocked

Notes:
1. End-of-frame (EOF) flags are ignored when operating in the open-buffer mode. Only D17..0 are active in the output buffer.
2. Data written to the buffer at rates above 500KSPS will accumulate in the buffer.
3. Access to an individual output channel is accomplished by first selecting (enabling) only the specific channel, and by then writing the output value to the buffer.

3.16-2 Simultaneous Direct Outputs

Table 3.16-4. Simultaneous Direct Outputs Example (Single Group)

Operation	PCI Bus Action	Board Response
Select simultaneous clocking.	Set SIMULTANEOUS OUTPUTS in the BCR.	Simultaneous clocking is selected.
Select the clocking rate.	Write the required sample clocking rate to the Rate-C generator control register.	The output clocking rate is selected.
Enable clocking	Set the ENABLE OUTPUT CLOCKING control bit HIGH in the buffer operations register. Set the ENABLE RATE-C GENERATOR control bit HIGH in the BCR.	Clocking is enabled at the default rate.
Clear the output buffer.	Set the CLEAR OUTPUT BUFFER bit in the output operations register.	The output buffer clears to empty.
Load the output value for the first active channel.	Write the first value to the output data buffer.	First value is retained in the buffer.
Load the output values for the remaining active channels.	Write the remaining active channel values to the output data buffer.	Remaining values are accumulated in the buffer. When the last value is loaded, all values are extracted from the buffer and appear simultaneously at the associated output channels.
Repeat the above operations for subsequent channel groups.	Continue to write output values to the output data buffer.	All active channels are updated simultaneously when the last value in each group is written to the buffer.

Notes: 1. Data written to the buffer at rates above 500KSPS will accumulate in the buffer.

3.16-3 Continuous Function

Table 3.16-5. Continuous Function Example

Operation	PCI Bus Action	Board Response
Select simultaneous clocking.	Set SIMULTANEOUS OUTPUTS in the board control register.	Simultaneous clocking is selected.
Set the buffer threshold flag to 1/4 of the expected block size.	Write 1/4 block size to the threshold register (Table 3.14-5).	The threshold flag will go LOW when the buffer contents drop below the threshold.
Select the clocking rate.	Write the required sample clocking rate to the Rate-C generator control register.	The output clocking rate is selected.
Enable clocking	Set the ENABLE OUTPUT CLOCKING control bit HIGH in the buffer operations register. Set the ENABLE RATE-C GENERATOR control bit HIGH in the BCR.	Clocking is enabled at the selected rate. The internal rate generator is enabled, if internal clocking is required.
Clear the output buffer.	Set the CLEAR OUTPUT BUFFER bit in the output operations register.	The output buffer clears to empty.
Write a block of values to all active channels. To avoid discontinuities in the output functions, the effective loading rate for channel groups must be greater than the sample (clocking) rate times the number of active channels. Maximum loading rate is 40MSPS during DMA transfers.	Write function values for all active channels to the output data buffer.	All active channels produce their respective output functions.
Wait for the buffer threshold flag to go LOW. (See Note 1).	Monitor the analog output buffer threshold flag until LOW.	The output buffer empties to less than 1/4-full status.
Repeat the previous two steps to sustain function generation.		All output functions proceed continuously.

Notes:
1. Response to the flag must be fast enough to prevent the buffer from going empty.

3.16.4 Periodic Function

Table 3.16-6. Periodic Function Example

Operation	PCI Bus Action	Board Response
Select simultaneous clocking.	Set SIMULTANEOUS OUTPUTS in the board control register.	Simultaneous clocking is selected.
Clear the output buffer.	Set the CLEAR OUTPUT BUFFER bit in the output operations register.	The output buffer clears to empty.
Load the function values for all active channels. (Note 1) Set the end-of-frame (EOF) flag.	Write all function values for all active channels to the output buffer. Set the EOF flag HIGH when writing the data value for the last channel in the last group.	Function values for all active channels accumulate in the buffer. The EOF flag is set HIGH in the buffer location that contains the last channel value in the last channel group.
Select the clocking rate.	Write the required sample clocking rate to the Rate-C generator control register.	The output clocking rate is selected.
Select the circular buffer mode.	Set CIRCULAR BUFFER in the buffer operations register.	The output buffer is closed (circular).
Enable the sample clock.	Set ENABLE OUTPUT CLOCKING in the buffer operations register. Set the ENABLE RATE-C GENERATOR control bit HIGH in the BCR.	Clocking is enabled. All active channels produce their respective functions repeatedly until the clock is disabled or the operating mode is changed. All outputs update simultaneously at the sample clock rate.

Notes:
1. To generate periodic functions simultaneously in multiple channels, all functions must be commensurate. That is, the functions in all channels must have frequencies that are exact integer multiples of the frequency of the lowest-frequency channel. Conversely, the period of the lowest-frequency channel must be an exact integer multiple of the period of each of the other channels.

3.16.5 Function Burst

Table 3.16-7. Function Burst Example

Operation	PCI Bus Action	Board Response
Select simultaneous clocking.	Set SIMULTANEOUS OUTPUTS in the board control register.	Simultaneous clocking is selected.
Clear the output buffer.	Set the CLEAR OUT BUFFER bit in the output operations register.	The output buffer clears to empty.
Load the function values for all active channels. Set the end-of-frame (EOF) flag.	Write all function values for all active channels to the output buffer. Set the EOF flag HIGH when writing the data value for the last channel in the last group.	Function values for all active channels accumulate in the buffer. The EOF flag is set HIGH in the buffer location that contains the last channel value in the last channel group.
If more than one burst-function is required, repeat the previous operations for each additional function.	---	If required, additional burst functions accumulate in the output buffer.
Select the clocking rate.	Write the required sample clocking rate to the Rate-C generator control register.	The output clocking rate is selected.
Select the triggering rate.	Write the required triggering rate to the Rate-D generator control register.	The burst triggering rate is selected.
Select triggered-burst mode.	Set ENABLE OUTPUT BURST in the buffer operations register.	The triggered-burst operating mode is selected.
Prepare the buffer operations register for burst mode:	Write to the buffer operations register:	---
If the burst functions will be used repeatedly, select the circular buffer mode.	To select the circular buffer mode, set CIRCULAR BUFFER.	If required, the output buffer is closed (circular), and all functions will be retained in the buffer indefinitely.
Enable the sample clock.	Set ENABLE OUTPUT CLOCKING.	Output clocking is enabled.
Enable the internal rate generators.	Set the ENABLE RATE-C and RATE-D GENERATOR control bits in the BCR.	Required internal rate generators are enabled.
For external burst triggering, or internal rate-generator triggering, no further bus activity is required.	---	All active output channels produce a single burst in response to each trigger.

3.16.6 Function Sequencing (Concatenation)

Table 3.16-8. Function Sequencing (Concatenation) Example

Operation	PCI Bus Action	Board Response
Establish a periodic function as described in Paragraph 3.15.4. The following operations will replace the original ('old') function in each channel with a new function.	---	Each active output is producing a specific output function or waveform. The output buffer is circular (closed), and is not accessible from the bus.
Request buffer access	Set LOAD REQUEST in the buffer operations register.	The board will assert the LOAD READY flag when the EOF flag in the original function occurs.
Wait for the buffer to open.	Monitor the LOAD READY status flag. The buffer is open when this flag goes HIGH.	The EOF flag in the existing function set causes the LOAD READY bit in the buffer operations register to be asserted. The buffer is now open, and the original functions are being flushed from the buffer.
Load the new function for each active channel into the buffer. Set the end-of-frame (EOF) flag.	Write the function values for all active channels to the output buffer. Set the EOF flag HIGH when writing the data value for the last channel in the last group.	New function values for all active channels reside in the buffer. The EOF flag is set HIGH in the buffer location that contains the last channel value in the last channel group. The original functions are still active, and the remaining values are flushed from the buffer as they are sent to the output channels.
(None required)	No further attention is required from the PCI bus.	The buffer returns to circular (closed) mode after the last data value in the original function set leaves the buffer. The new function then commences seamlessly and circulates within the buffer. Both the Load Request control bit and the Load Ready flag are cleared automatically when the buffer closes.

3.17 Assembly Configuration Register

The read-only Assembly Configuration register (Table 3.17-1) contains the existing firmware revision and a status field that indicates the availability of optional features.

Table 3.17-1. Assembly Configuration Register

Offset: 0000 0034h **Default: 00XX XXXXh**

BIT FIELD	DESCRIPTION
D00-D11	Firmware Revision
D12-D15	(Reserved bit field)
D16	Number of analog output channels: 0 => 8 output channels. 1 => 4 output channels.
D17-D18	Master Clock frequency: 0 => 40.320 MHz. 1 => (Reserved) 2 => (Reserved) 3 => (Reserved)
D19-D20	Custom Features: 0 => No custom features. 1 => (Reserved) 2 => (Reserved) 3 => (Reserved)
D21-D31	(Reserved bit field; returns all-zero).

3.18 Auxiliary External Clock andTrigger I/O

Two auxiliary external connections provide an alternate method of synchronizing sample clocking and burst triggering to external events. These TTL or LVDS connections are available as AUX CLOCK I/O and AUX TRIGGER I/O (Table 2.2-2), and when active *as inputs*, replace the corresponding external CLOCK I/O and SYNC I/O inputs in the system I/O connector. The AUX I/O signals are accessible through a 6-Pin connector on the back (Side-2) of the board.

AUX clock and trigger signals are designated independently through the Auxiliary Sync I/O Control register as inputs, outputs, or inactive, as indicated in Table 3.18-1. When an AUX signal is designated as an ***input***, the signal replaces the corresponding CLOCK INPUT or TRIGGER INPUT input from the system connector. In order for the input to be acknowledged, ***Analog Output External Clock/Trigger input*** must be selected in the corresponding clock or sync control field in the Output Configuration register (Table 3.4-1).

Active AUX ***outputs*** produce an output pulse for each internal output clock or burst trigger, and are active in both target and initiator clock and sync modes.

AUX *inputs* are edge-detected as LOW-to-HIGH transitions if the INVERT INPUTS control bit is LOW, or as HIGH-to-LOW transitions if the bit is HIGH. Minimum HIGH and LOW level durations are 100ns if the NOISE SUPPRESSION control bit is LOW, or 1.5us if the bit is HIGH. AUX *output pulses* are positive (i.e.: baseline level is LOW) if the INVERT OUTPUTS control bit is LOW, or negative (baseline HIGH) if the control bit is HIGH. Output pulse width is typically 130ns if the NOISE SUPPRESSION control bit is LOW, or 2.0us if the bit is HIGH.

To increase the reliability of external clocking or triggering in high-noise environments, selectable noise suppression increases the debounce or detection interval for active inputs, and increases the pulse width of active outputs.

Table 3.18-1. Auxiliary Sync I/O Control

Offset: 0000 001Ch **Default: 0000 0000h**

Data Bit	Mode	Designation	Default	Description
D00-01	R/W	AUX CLOCK Control Mode	0	AUX CLOCK I/O Control Mode: 0 => Inactive 1 => Active Input (LO-to-HI edge) 2 => Active Output (Positive pulse) 3 => (Reserved)
D02-03	R/W	AUX SYNC Control Mode	0	AUX SYNC I/O Control Mode *
D04-05	R/W	(Reserved)	0	---
D06-07	R/W	(Reserved)	0	---
D08	R/W	INVERT INPUTS	0	Active inputs are detected on the LO-to-HI edge when this bit is LOW, or on the HI-to-LO edge when this bit is HIGH.
D09	R/W	INVERT OUTPUTS	0	Active outputs produce HIGH pulses when this bit is LOW, or LOW pulses when this bit is HIGH.
D10	R/W	NOISE SUPPRESSION	0	When LOW, input debounce time is 90 ns-120ns and output pulse width is approximately 135ns. When HIGH, input debounce time is 1.3us, and output pulse width is 1.8us.
D11-31	RO	(Reserved)	0	Read-back as all-zero.

* Same configuration as the AUX CLOCK I/O control mode.

SECTION 4.0

PRINCIPLES OF OPERATION

4.1 General Description

Eight 18-bit analog output channels (Figure 4.1-1) provide software-selected output ranges of ±10V, ±5V and ±2.5V, and are accessed from the PCI bus through a dedicated 256K-sample FIFO buffer. An 8-Bit digital port is configured as two independently controlled sets of four bidirectional I/O lines.

A PCI interface adapter provides the interface between the controlling PCI bus and an internal local controller, and supports universal signaling. +5 VDC power from the PCI bus is converted into regulated power voltages for the internal analog networks.

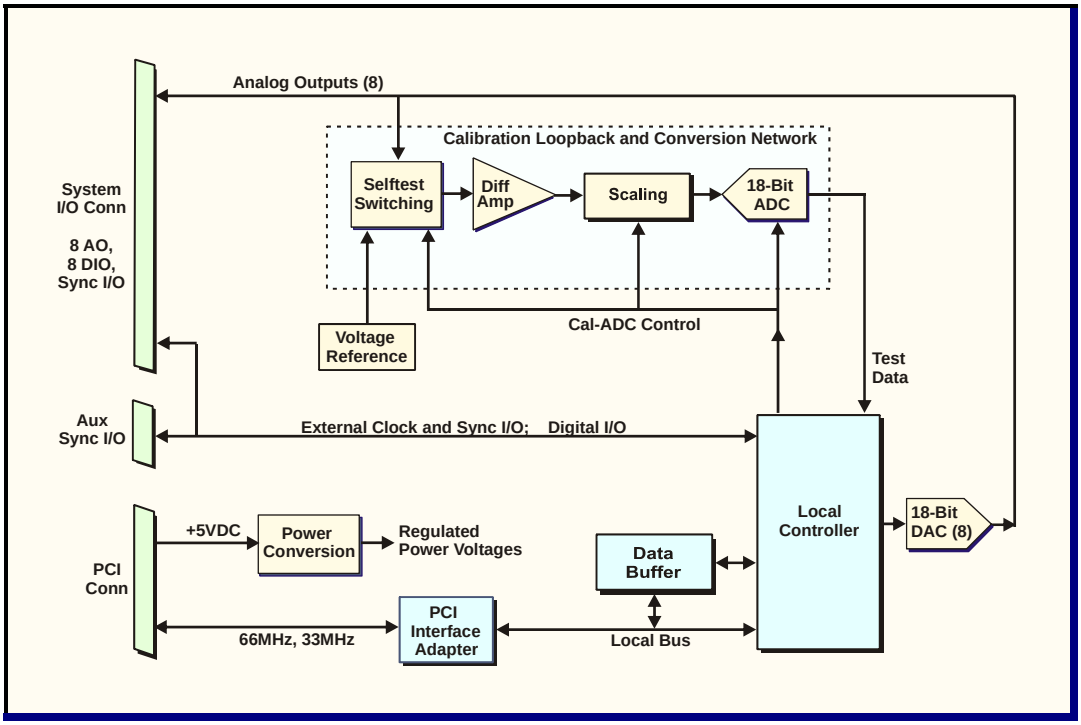

Figure 4.1-1. Functional Block Diagram

Selftest switches provide test signals for autocalibration of all output channels, and are configured automatically to accept either differential or single-ended system outputs.

Analog output clocking on multiple target boards can be synchronized to a single software-designated initiator board.

4.2 Analog Outputs

Eight independent 18-bit DAC's are controlled through a dedicated 256 Ksample FIFO buffer. The buffer can be operated either open for data streaming, or closed (circular) for periodic function generation. Function concatenation from the PCI bus is supported. The output configuration can be selected as either single-ended or balanced differential.

Each 18-bit DAC consists of a 2-bit high-order DAC and a 16-Bit low-order DAC. The 2-bit DAC has a weighting factor equal to four times that of the 16-Bit DAC, which effectively serves as a 16-bit vernier for each of the upper four states. All four states of the 2-Bit DAC are calibrated individually during autocalibration, and then are dynamically corrected in real-time during operation. The 16-bit DAC is calibrated to occupy precisely one state of the 2-Bit DAC.

Output clocking and triggering can be supplied: (a) from two internal 24-Bit analog output rate generators, (b) from the analog input rate generators, or (c) from an external source. Triggered bursts, or functions, are supported. The output burst size is controlled by a tag-bit attached to the last output value in a sequence. If the tag-bit is not attached, a burst will operate continuously after a trigger, or until the buffer goes empty.

4.3 Autocalibration

Autocalibration is an embedded firmware utility that calibrates all analog output channels to a single internal voltage reference. The utility can be invoked at any time by the control software.

The internal voltage reference is used to calibrate the span of an internal 18-Bit A/D converter, and a zero-reference is used to calibrate the offset value. The A/D converter then is used to calibrate all eight output channels as they are driven to the same two calibration points. Correction values are retained until the autocalibration sequence is repeated, or until power is removed.

4.4 Power Control

Regulated power voltages of ±5 VDC and ±14 VDC are required for the analog networks, and are derived from the +5-Volt input provided by the PCI bus, both by switching preregulators and by linear postregulators.

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APPENDIX A

LOCAL REGISTER QUICK REFERENCE

APPENDIX A
LOCAL REGISTER QUICK REFERENCE

This appendix summarizes the local registers and principal control-bit fields described in Section 3.

Table 3.1-1. Control and Status Registers

OFFSET (Hex)	REGISTER	MODE	DEFAULT	PRIMARY FUNCTION	REF
0000	BOARD CONTROL	RW	2200 0000h	Board Control Register (BCR).	3.2
0004	DIGITAL I/O PORT	RW	0000 0X0Xh	Digital I/O port data.	3.12
0008-0010	(Reserved)	RO	0000 0000h	---	---
0014	SELFTEST CONFIGURATION	RW	0000 0000h	Selftest node selection.	3.14
0018	SELFTEST DATA BUFFER	RO	000X XXXXh	Selftest FIFO data buffer..	3.14
001C	AUXILIARY SYNC I/O CONTROL	RW	0000 0000h	Controls AUX Clock and Trigger I/O	3.18
0020-002C	(Reserved)	RO	0000 0000h	---	---
0030	PRIMARY STATUS	RW	0000 0000h	Principal status-flag register	3.15
0034	ASSEMBLY CONFIGURATION	RO	00XX XXXXh	Options and firmware revision.	3.17
0038	Autocal Values *	RW	0000 XXXXh	Autocal value readback.	---
003C	BUFFERED OUTPUT OPERATIONS	RW	0000 1400h	Buffered Analog Outputs Control	3.4
0040	OUTPUT BUFFER THRESHOLD	RW	0003 FFFEh	Output buffer status flag threshold.	3.5.5
0044	OUTPUT BUFFER SIZE	RO	0000 0000h	Number of data values in the output buffer.	3.5.5
0048	ANALOG OUTPUT BUFFER	WO	0000 0000h	Analog Output Data Buffer.	3.5
004C	RATE GENERATOR C	RW	0000 0180h	Rate-C generator divider; 24 bits.	3.7.1.2 3.11
0050	RATE GENERATOR D	RW	0000 2760h	Rate-D generator divider; 24 bits.	3.8.3 3.11
0054	OUTPUT CONFIGURATION	RW	0000 00FFh	Analog output configuration.	3.4
0056-007C	(Reserved)	---	---	---	---

* Maintenance register; Shown for reference only.

Table 3.2-1. Board Control Register (BCR)

Offset: 0000h **Default: 2200 0000h**

BIT	MODE [1]	DESIGNATION	DEF	DESCRIPTION	REF
D00	R/W	INITIATE SELFTEST [2]	0	Initiates a selftest cycle, in which data from the selected selftest measurement node is acquired.	3.14
D01	RO	SELFTEST DATA READY	0	LOW initially and during selftest data acquisition. HIGH when data acquisition is completed.	3.14
D02	RW	CLEAR SELFTEST BUFFER [2]	0	Clears (empties) the selftest data buffer	3.14
D03-D04	RW	(Reserved)	0	---	---
D05	RW	DIFFERENTIAL SYNC IO	0	Selects LVDS external sync I/O levels when HIGH.	2.3.3
D06-D17	RW	(Reserved)	0	---	---
D18	RW	SIMULTANEOUS OUTPUTS	0	When HIGH, all outputs update simultaneously in response to an output clock. When LOW, each output is updated immediately when new data is received.	3.7.2
D19	RW	(Reserved)	0	---	---
D20	RW	OUTPUT SW CLOCK [2,3]	0	Produces a single analog output clock. Overrides existing output clocking source.	3.7.1
D21	RW	ENABLE RATE-C GENERATOR	0	Enables the Rate-C generator for analog outputs.	3.7.1.2
D22	R/W	ENABLE RATE-D GENERATOR	0	Enables the Rate-D generator for analog outputs.	3.8.3
D23	R/W	OUTPUT SW TRIGGER [3]	0	Output Burst S/W Trigger. See also Table 3.4-2.	3.8.2
D24	RW	(Reserved)	0	---	---
D25	RW	OFFSET BINARY	1	Selects offset-binary analog I/O data format when HIGH, or two's complement when LOW.	3.5.3
D26-D27	RO	(Reserved)	0	---	---
D28	RW	AUTOCAL [2]	0	Initiates an autocalibration operation when asserted. Clears automatically upon completion,	3.7.1.2 3.11
D29	RO	AUTOCAL PASS	1	Set HIGH at reset or autocal initialization. A HIGH state after autocal confirms a successful calibration.	3.13
D30	RO	(Reserved)	0	---	---
D31	RW	INITIALIZE [2]	0	Initializes the board. Sets all register defaults.	

Notes: 1. RW = Read/Write, RO = Read-Only. 2. Clears automatically. 3. Duplicated elsewhere.

Table 3.3-1. Configuration Operations

Operation	Maximum Duration
PCI configuration registers are loaded from internal ROM	3 ms
Internal control logic is configured from internal ROM	300 ms
Internal control logic is initialized	3 ms

Table 3.4-1. Output Configuration Register

Offset: 0054h **Default: 0000 00FFh**

BIT	MODE	DESIGNATION	DEF	DESCRIPTION	REF
D00	RW	OUTPUT 00	1	Analog output Active Channel selection mask.	3.4.1
D01	RW	OUTPUT 01	1	HIGH to enable.	
D02	RW	OUTPUT 02	1		
D03	RW	OUTPUT 03	1		
D04	RW	OUTPUT 04	1	(D04-D07 are LOW in the 4-channel	
D05	RW	OUTPUT 05	1	configiuration.)	
D06	RW	OUTPUT 06	1		
D07	RW	OUTPUT 07	1		
D08-D10	RW	OUTPUT RANGE	0	Analog Output Range: 0 => ±2.5V. 1 => ±5V. 2 => ±10V 3-7 => (Reserved).	3.4.2
D11	RW	CLOCK AND TRIGGER OUT	0	Enables the Analog Output Clock and Trigger external outputs,	3.7.1 3.8.2
D12-D13	RW	CLOCK SOURCE	0	Analog Output clock source: 0 => Rate-C Generator. 1 => (Reserved) 2 => Analog Output External Clock input 3 => (Reserved).	3.7.1
D14-D15	RW	TRIGGER SOURCE	0	Analog Output trigger source: 0 => Rate-D Generator. 1 => (Reserved). 2 => Analog Output External Trigger input 3 => (Reserved).	3.8.2
D16	RW	DIFFERENTIAL CONFIG	0	Analog Output Configuration: 0 => Single-ended outputs. 1 => Differential outputs.	3.4.4
D17	RW	INVERT EXT SYNC *	0	Inverts the logic polarities of the external clock and trigger inputs and outputs.	3.7.1 3.8.2
D18	RW	Maintenance Utility **	0	---	---
D19-D31	RO	(Reserved)	0000h	---	---

* Does not affect the Auxiliary Sync I/O logic polarities (3.18).

** Maintenance control bit. Shown for reference only. Always write LOW.

Table 3.4-2. Buffered Output Operations Register

Offset: 003Ch **Default: 0000_1400h**

BIT	MODE	DESIGNATION	DEF	DESCRIPTION	REF
D00-D04	R/W	(Reserved)	0h	---	---
D05	R/W	ENABLE OUTPUT CLOCKING	0	Enables output clocking when HIGH. Disables clocking when LOW. Default is LOW (clocking disabled).	3.7
D06	RO	OUTPUT CLOCK READY	0	Indicates when HIGH that an output clock will be accepted. If LOW, indicates that the output will not respond to a clock.	3.7
D07	R/W	OUTPUT SW CLOCK *	0	Produces a single output clock event when asserted. Independent of clocking mode. Duplicated in the BCR.	3.7.1
D08	R/W	CIRCULAR BUFFER	0	Selects circular buffer configuration if HIGH, or open self-flushing buffer configuration if LOW. Access for loading new data into the circular buffer must be requested by asserting LOAD REQUEST. Default is LOW; i.e. open buffer.	3.5.6 3.5.7
D09	R/W	LOAD REQUEST *	0	When set HIGH, requests loading access to the circular buffer. Initializes LOW.	3.6.3
D10	RO	LOAD READY	1	Set HIGH when the frame index passes through zero, if both CIRCULAR BUFFER and LOAD REQUEST are HIGH. When HIGH, indicates that the circular buffer is ready to accept new data. Available also in the PSR. Defaults HIGH.	3.6.3
D11	R/W	CLEAR OUTPUT BUFFER *	0	Resets the output buffer to empty.	3.5.5
D12	RO	AO BUFFER EMPTY	1	Indicates the analog output buffer is empty.	3.5.5
D13	RO	OUTPUT BUFFER THRESHOLD	0	Analog output buffer threshold flag. Duplicated in the AO Buffer Threshold register.	3.5.5
D14	RO	(Reserved)	0	Inactive; Returns zero.	---
D15	RO	AO BUFFER FULL	0	Indicates the output buffer is full.	3.5.5
D16	R/W	AO BUFFER OVERFLOW	0	Set HIGH when data is written to a full buffer. **	3.5.5
D17	R/W	FRAME OVERFLOW	0	Set HIGH when data is written to a closed buffer. **	3.6.3
D18	RO	BURST READY	0	If HIGH, indicates that a burst trigger will be accepted. If LOW, indicates that the output will not respond to a trigger.	3.8.2
D19	R/W	ENABLE OUTPUT BURST	0	Enables analog output burst operation.	3.8.1
D20	R/W	OUTPUT SW TRIGGER *	0	Produces a single output trigger event when asserted. Clears LOW automatically when the triggered burst is completed. Independent of triggering mode. Duplicated in the BCR.	3.8.2
D21-D31	RO	(Reserved)	0	Inactive. Returns all-zero.	---

* Clears LOW automatically when operation is completed.
** Remains HIGH until cleared by a direct write as LOW, or by initialization.

Table 3.5-1. Analog Output Buffer

Offset: 0048h **Default: N/A (Write-Only; Returns all-zero)**

BIT	MODE*	DESIGNATION	DESCRIPTION
D00	WO	DATA 00	Least significant data bit
D01-D16	WO	DATA 01 - DATA 16	Intermediate data bits
D17	WO	DATA 17	Most significant data bit
D18	WO	EOF FLAG	End-of-frame (EOF) flag.
D19-D31	WO	---	(Inactive)

* WO indicates write-only access. Read-access returns all-zero value.

Table 3.5-2. Output Buffer Size Register

Offset: 0044h **Default: 0000 0000h**

DATA BIT	MODE*	DESIGNATION	DEF	DESCRIPTION
D00-D18	RO	BUFFER SIZE	0 0000h	Number of values in the output buffer
D19-D31	RO	(Inactive)	0	---

Table 3.5-3. Output Buffer Threshold Register

Offset: 0040h **Default: 0003 FFFEh**

BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00-D18	RW	OUTPUT BUFFER THRESHOLD	3 FFFEh	Specifies the number of values in the output buffer, above which the threshold flag is asserted HIGH.
D19	RO	(Reserved)	0	---
D20	RO	OUTPUT BUFFER THRESHOLD FLAG	0	HIGH when the number of values in the output buffer *exceeds* the specified buffer threshold.
D21-D31	RO	(Reserved)	0	---

Table 3.10-1. Typical Output Buffer DMA Register Configuration

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Analog Input Buffer local address (Analog input buffer)	0000 0018h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction; PCI bus to Local bus (Analog outputs)	0000 0000h
A8h	DMA Command Status	Command and Status Register	0000 0001h 0000 0003h (See Text)

* Determined by specific transfer requirements.

Table 3.11-1. Rate Generator Registers (Rate-C,D)

Offset: 004Ch (Rate-C), 0050h (Rate-D) **Default: 0000 0180 (Rate-C), 0000 2760h (Rate-D)**

DATA BIT	MODE*	DESIGNATION	DEFAULT	DESCRIPTION
D00-D23	R/W	Ndiv	---	Rate generator frequency control
D24-D31	RO	(Inactive)	0	---

* R/W = Read/Write, RO = Read-Only.

Table 3.11-2. Typical Rate Generator Frequency Selection

Ndiv		FREQUENCY Fgen (40.320 MHz Master Clock)*
(Dec)	(Hex)	(Hz)
126	007E	320,000
127	007F	317,480
128	0080	315,000
---	---	Fgen (Hz) = Fclk (Hz) / Ndiv **

* ±0.003 percent. ** Fclk = master clock frequency; e.g.: 40.32MHz.

Table 3.12-1. Digital I/O Port Register

Offset: 0004h **Default: 0000 0X0Xh**

DATA BIT	MODE*	DESIGNATION	DEFAULT	DESCRIPTION
D00	RW	DIO 00 DATA	X	Digital I/O Data; Bits 00-03
D01	RW	DIO 01 DATA	X	
D02	RW	DIO 02 DATA	X	
D03	RW	DIO 03 DATA	X	
D04-D06	RW	(Reserved)	0h	---
D07	R/W	DIO 00_03 OUTPUT	0	DATA 00-03 direction control; High for output.
D08	RW	DIO 04 DATA	X	Digital I/O Data; Bits 04-07
D09	RW	DIO 05 DATA	X	
D10	RW	DIO 06 DATA	X	
D11	RW	DIO 07 DATA	X	
D12-D14	RW	(Reserved)	0h	---
D15	RW	DIO 04_07 OUTPUT	0	DATA 04-07 direction control; High for output.
D16-D31	RO	(Reserved)	0h	Read back as all-zero.

Table 3.14-1. Selftest Configuration Register

Offset: 0014h **Default: 0000 0000h**

BIT	MODE	DESIGNATION	DEFAULT	DESCRIPTION
D00-D03	RW	SELFTEST MEASUREMENT NODE	0h	Measurement Node: 0 => ZERO Selftest. 1 => +VREF Selftest. 2-7 => (Reserved). 8 => Output Channel 00 * 9 => Output Channel 01 10 => Output Channel 02 11 => Output Channel 03 12 => Output Channel 04 13 => Output Channel 05 14 => Output Channel 06 15 => Output Channel 07
D04-D31	RO	(Reserved)	0h	---

* Differential/single-ended measurement configuration is selected automatically to conform to the selected analog output configuration.

Table 3.14-2. Selftest Data Buffer

Offset: 0018h **Default: 000X XXXXh**

BIT	MODE*	DESIGNATION	DESCRIPTION
D00	RO	DATA 00	Least significant data bit
D01-D16	RO	DATA 01 - DATA 16	Intermediate data bits
D17	RO	DATA 17	Most significant data bit
D18-D31	RO	(Reserved)	---

* WO indicates write-only access. Read-access returns all-zero value.

Table 3.15-1 Primary Status Register

Offset: 0x0030 **Default: 0000 0000h**

SELECTION BIT [1]	CRITICAL EVENT	RESPONSE BIT [2]	REFERENCE PARAGRAPH
D00	Autocal completed [3]	D16	3.13
D01	(Reserved)	D17	---
D02	(Reserved)	D18	---
D03	(Reserved)	D19	---
D04	(Reserved)	D20	---
D05	Selftest Data Ready [3]	D21	3.14
D06	(Reserved)	D22	---
D07	(Reserved)	D23	---
D08	Digital I/O Port DIO 00 LOW-to-HIGH transition [3]	D24	3.12
D09	Output Buffer threshold flag HIGH-to-LOW transition [3]	D25	3.5.5
D10	Output Buffer threshold flag LOW-to-HIGH transition [3]	D26	3.5.5
D11	Output Load-Ready Flag HIGH-to-LOW transition [3]	D27	3.6.3
D12	Output Load-Ready Flag LOW-to-HIGH transition [3]	D28	3.6.3
D13	Analog Output Burst Ready [3]	D29	3.8.2
D14	Output Buffer Overflow or Frame Overflow [3]	D30	3.5.5
D15	(Reserved)	D31	---

1. Event selection. Enables assertion of the corresponding response bit when the selected event occurs.
2. Event response. Asserted HIGH when a selected event occurs. Edge-detected response bits remain HIGH until cleared LOW.
3. Edge-detected event.

Table 3.17-1. Assembly Configuration Register

Offset: 0000 0034h **Default: 00XX XXXXh**

BIT FIELD	DESCRIPTION
D00-D11	Firmware Revision
D12-D15	(Reserved bit field)
D16	Number of analog output channels: 0 => 8 output channels. 1 => 4 output channels.
D17-D18	Master Clock frequency: 0 => 40.320 MHz. 1 => (Reserved) 2 => (Reserved) 3 => (Reserved)
D19-D20	Custom Features: 0 => No custom features. 1 => (Reserved) 2 => (Reserved) 3 => (Reserved)
D21-D31	(Reserved bit field; returns all-zero).

Table 3.18-1. Auxiliary Sync I/O Control

Offset: 0000 001Ch **Default: 0000 0000h**

Data Bit	Mode	Designation	Default	Description
D00-01	R/W	AUX CLOCK Control Mode	0	AUX CLOCK I/O Control Mode: 0 => Inactive 1 => Active Input (LO-to-HI edge) 2 => Active Output (Positive pulse) 3 => (Reserved)
D02-03	R/W	AUX SYNC Control Mode	0	AUX SYNC I/O Control Mode *
D04-05	R/W	(Reserved)	0	---
D06-07	R/W	(Reserved)	0	---
D08	R/W	INVERT INPUTS	0	Active inputs are detected on the LO-to-HI edge when this bit is LOW, or on the HI-to-LO edge when this bit is HIGH.
D09	R/W	INVERT OUTPUTS	0	Active outputs produce HIGH pulses when this bit is LOW, or LOW pulses when this bit is HIGH.
D10	R/W	NOISE SUPPRESSION	0	When LOW, input debounce time is 100ns-135ns and output pulse width is 135ns. When HIGH, input debounce time is 1.5us, and output pulse width is 1.8us.
D11-31	RO	(Reserved)	0	Read-back as all-zero.

* Same configuration as the AUX CLOCK I/O control mode.

APPENDIX B

COMPARISON of PMC66-18AO8 and PCI66-18AISS8AO8

Appendix B

Comparison of PMC66-18AO8 and PMC66-16AISS16AO2

Operation of the PMC66-18AO8 is similar to that of the PCI66-18AISS8AO8. This appendix summarizes the principal similarities and differences between the two products, and is provided as a general guide rather than a comprehensive list of requirements.

B.1. Comparison of Features

Table B.1 compares principal PMC66-18AO8 and PCI66-18AISS8AO8 features. Modifications are shown in bold type.

Table B.1. PCI66-18AISS8AO8, PMC66-18AO8 Comparison

Feature	PCI66-18AISS8AO8	PMC66-18AO8
Form Factor	**PCI; Full-length**	**PMC; Single-width**
Output Channels	Eight 18-Bit Dac's; R-2R Hybrid	Eight 18-Bit Dac's; R-2R Hybrid
Output Clock Rates	Zero to 500KSPS/Chan	Zero to 500KSPS/Chan
Output Buffer	**512K-Sample FIFO**	**256K-Sample FIFO**
Output Ranges	±10V, ±5V, ±2.5V, 0/+10V, 0/+5V	±10V, ±5V, ±2.5V
Output Registers	None. Accessed through buffer	None. Accessed through buffer
Output Configuration	Single-Ended or Balanced Differential; Software-selectable	Single-Ended or Balanced Differential; Software-selectable
Input Channels	**Eight 18-Bit ADC's; SAR**	**None**
Function Generation	Yes	Yes
Rate Generators	**Four, with 24-Bit dividers**	**Two, with 24-Bit dividers**
Digital I/O Port	8-Bit Bidirectional TTL; Nibble oriented.	8-Bit Bidirectional TTL; Nibble oriented.
PCI Adapter	PCI-9056 (66MHz PCI)	PCI-9056 (66MHz PCI)
Interrupt	None. Replaced with a primary status register.	None. Replaced with a primary status register.
PCI Interface	PCI 2.3; 33MHz/66MHz	PCI 2.3; 33MHz/66MHz
DMA (Buffers)	Block mode	Block mode
Local Clock	40-45 MHz; Standard 40.32MHz	40-45 MHz; Standard 40.32MHz

B.2. Migration from PMC66-18AISS8AO8:

General:

- References to the analog input channels and current loop termination have been deleted.

Para 2.2.2. Input/Output Cable Connections:

- The system I/O connector has changed from 100 pins to 68 pins.

Table 3.1-1. Control and Status Registers:

- The Analog Input Config register has been replaced by the Selftest Control register.
- The Analog Input Buffer has been replaced by the Selftest Data Buffer.
- The following registers have been deleted:
  - Current Loop Select control register,
  - Rate-A/B Generators,
  - Analog Input Buffer Size, Burst Block Size and Buffer Threshold control/status registers.
- The following register has been added:
  - Auxiliary Sync I/O Control.
- One or more register default values have changed.

Table 3.2-1. Board Control Register (BCR):

- Control bits D00-02 have been reassigned as selftest control and status bits.

Table 3.4-1. Output Configuration Register:

- Output range and clock/trigger source bit-fields have been modified.

Paragraph 3.4.2. Voltage Range Selection:

- Unipolar ranges have been deleted.
- The default output range has been changed from ±10V to ±2.5V, to protect low-voltage loads when initializing.

Tables 3.5-2, 3.5-3. Output Buffer Size and Threshold registers:

- The value-range (bit-field width) for these registers have been reduced due to the reduced buffer size.

Table 3.14-1. Selftest Configuration Control Register:

- A new Selftest Configuration register replaces the Analog Input Configuration register.

Table 3.14-2. Selftest Data Buffer:

- A new Selftest Data Buffer replaces the Analog Input Data Buffer.

Table 3.17-2. Assembly Configuration Register:

- Modified to conform to PMC66-18AO8 options.

Para 3.18. Input/Output Cable Connections:

- Added auxiliary sync/I/O feature.

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