General Standards Corporation

High Performance Bus Interface Solutions

Rev: 031708

PC104P-24DSI12-4-16SDI

24-BIT, 4-CHANNEL DELTA-SIGMA, 200 KSPS ANALOG INPUT PCI BOARD

REFERENCE MANUAL

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SECTION 1.0

INTRODUCTION

1.1 General Description

The PC104P-24DSI12-4-16SDI board provides 24-bit analog input capability for the PC104-*Plus* bus at sample rates up to 200 KSPS per channel. In addition to providing four analog input channels, this product supports multiboard clocking and synchronization. The board is functionally and mechanically compatible with the IEEE PCI local bus specification Revision 2.3, and supports the "plug-n-play" initialization concept. Power requirements consist of +5 VDC in accordance with the PCI specification, and operation over the specified temperature range is achieved with minimal air cooling. Specific details pertaining to physical characteristics and performance are contained in the PC104P-24DSI12-4-16SDI product specification.

The board is designed for minimum off-line maintenance, and includes internal monitoring features that eliminate the need for disconnecting or removing the module from the system for calibration. All system input and output connections are made at the front panel through a 68-Pin dual-ribbon cable connector. Figure 1.1 shows the physical configuration of the board.

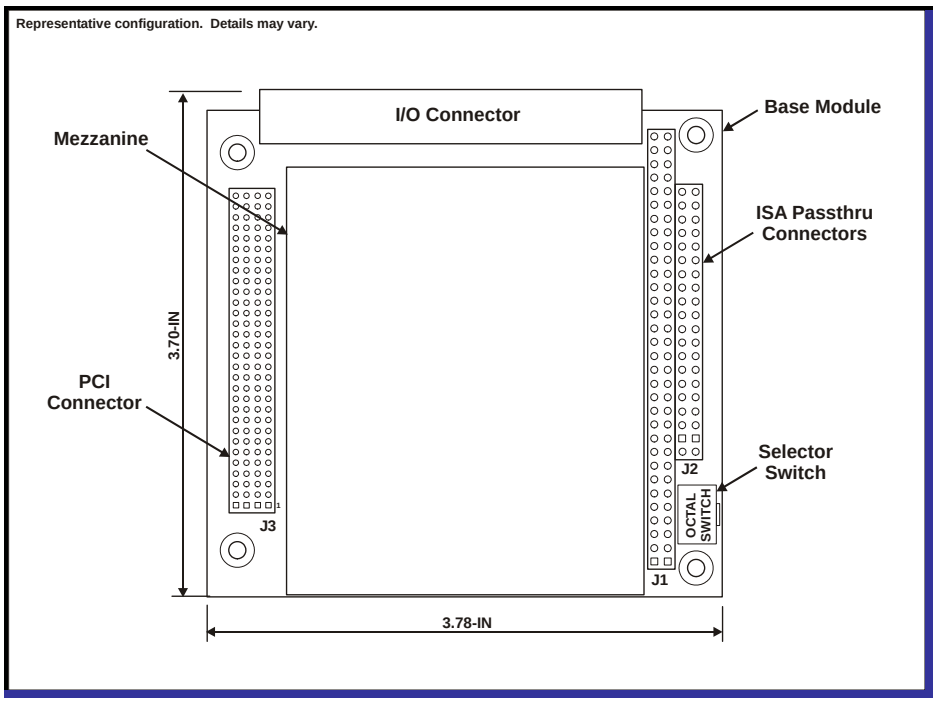

Figure 1.1. Physical Configuration

1.2 Functional Overview

A PCI interface adapter provides the interface between the controlling PCI bus and the internal local controller through a 32-bit local bus (Figure 1.2). Inputs are organized into two channel groups, either of which can be designated as either active or inactive independently of the other group. Each input channel provides configuration switches for selftest and autocalibration operations, as well as range-scaling and analog image filter networks. Each even-odd channel pair also contains a dual delta-sigma A/D converter (ADC) that provides two separate but synchronized conversion channels. An internal voltage reference can be applied to all channels to support selftest operations and autocalibration. Gain and offset trimming of the input channels is performed by automatically applying correction values obtained during autocalibration.

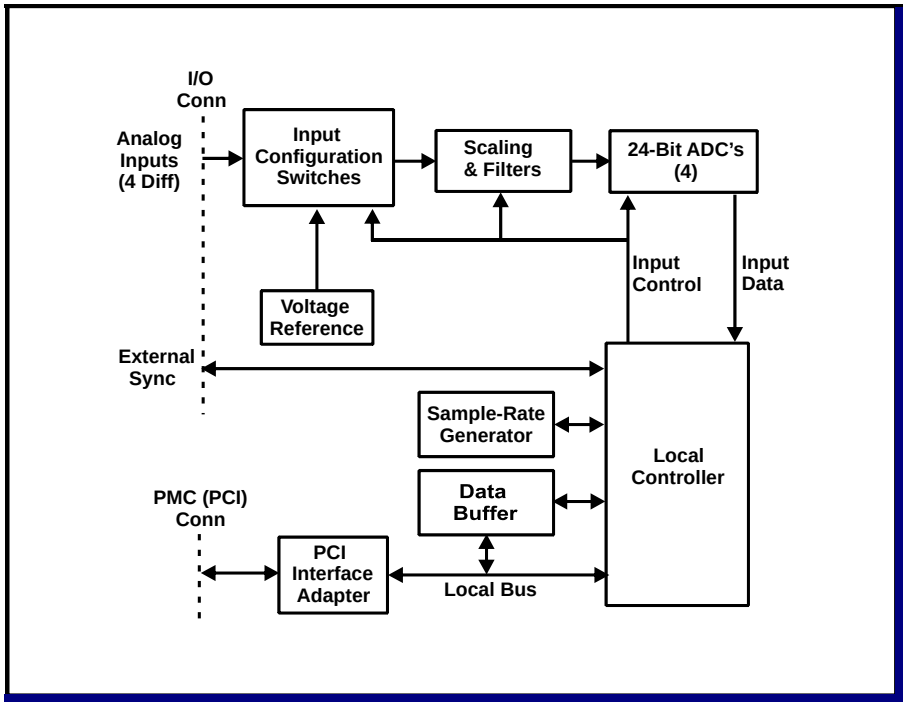

Figure 1.2. Functional Organization

Two internal sample-rate clock generator are divided down within the local controller to provide the ADC sample rates. Input bandwidth extends down to DC. Conversion data from all active channels is transferred to the PCI bus through a 256K-sample FIFO data buffer.

Multiple channels can be synchronized to perform sampling in "lockstep", either by a software command, or by external hardware sync and clock input signals. Hardware sync and clock input/output signals permit multiple boards to be connected together for phase-locked operation from a common clock.

SECTION 2.0
INSTALLATION AND MAINTENANCE

2.1 Board Configuration

With the single exception of a rotary selection switch, this product has no field-alterable configuration features, and is completely configured at the factory.

The selection switch (Figure 1.1-1) allows the board to be configured as one of four unique devices in a PC104-*Plus* stack. Positions 0 through 3 provide four unique bus-access configurations, while positions 4 through 7 are unused. The exact relationship or mapping of switch positions and slot-specific signals may vary among manufacturers of PC104-*Plus* motherboards.

2.2 Installation

2.2.1 Physical Installation

To minimize the opportunity for accidental damage before installation, the module should be stored in the original protective shipping envelope. System power must be turned OFF before proceeding with the installation.

CAUTION: This product is susceptible to damage from electrostatic discharge (ESD). Before removing the module from the conductive shipping envelope, ensure that the work surface, the installer and the host equipment have been properly discharged to ground.

After removing the module from the antistatic shipping container, align the PCI and ISA connector pins with the corresponding receptacles on either the host board if the module is the first module in the stack, or on the preceding module in the stack. Press the module carefully but firmly downward into position, and verify that the PCI and ISA connectors have mated completely and that the spacers are seated against the host or preceding module.

2.2.2 Input/Output Cable Connections

System cable signal pin assignments are listed in Table 2.2.2. Unused input pins may be left disconnected in most applications. However, if very long cables are used or if excessive cable noise is anticipated, the unused analog inputs should be grounded to the input return to minimize the injection of noise into the board.

The system I/O connector is designed to mate with a 68-pin dual-ribbon connector, equivalent to AMP #749621-7. This insulation displacement (IDC) cable connector accepts two 34-wire 0.050-inch ribbon cables, with the pin numbering convention shown in Table 2.2.2 and in Figure 2.2.2.

Table 2.2.2. System Connector Pin Assignments

ROW-A		ROW-B	
PIN	**FUNCTION**	**PIN**	**FUNCTION**
1	INPUT RETURN	1	INPUT RETURN
2	INPUT RETURN	2	INPUT RETURN
3	**INP CHAN 00 LO**	3	(No connect) *
4	**INP CHAN 00 HI**	4	(No connect) *
5	INPUT RETURN	5	INPUT RETURN
6	INPUT RETURN	6	INPUT RETURN
7	**INP CHAN 01 LO**	7	(No connect) *
8	**INP CHAN 01 HI**	8	(No connect) *
9	INPUT RETURN	9	INPUT RETURN
10	INPUT RETURN	10	INPUT RETURN
11	**INP CHAN 02 LO**	11	(No connect) *
12	**INP CHAN 02 HI**	12	(No connect) *
13	INPUT RETURN	13	INPUT RETURN
14	INPUT RETURN	14	INPUT RETURN
15	**INP CHAN 03 LO**	15	(No connect) *
16	**INP CHAN 03 HI**	16	(No connect) *
17	INPUT RETURN	17	INPUT RETURN
18	INPUT RETURN	18	INPUT RETURN
19	(No connect) *	19	(No connect) *
20	(No connect) *	20	(No connect) *
21	INPUT RETURN	21	INPUT RETURN
22	INPUT RETURN	22	INPUT RETURN
23	(No connect) *	23	(No connect) *
24	(No connect) *	24	(No connect) *
25	VTEST RETURN	25	INPUT RETURN
26	**VTEST**	26	INPUT RETURN
27	DIGITAL RETURN	27	DIGITAL RETURN
28	DIGITAL RETURN	28	DIGITAL RETURN
29	(No connect) *	29	(No connect) *
30	**EXT CLK INP**	30	**EXT CLK OUT**
31	DIGITAL RETURN	31	DIGITAL RETURN
32	DIGITAL RETURN	32	DIGITAL RETURN
33	(No connect) *	33	(No connect) *
34	**EXT SYNC INP**	34	**EXT SYNC OUT**

* "No-connect" pins should be open (unconnected) at the remote end of the system I/O cable.

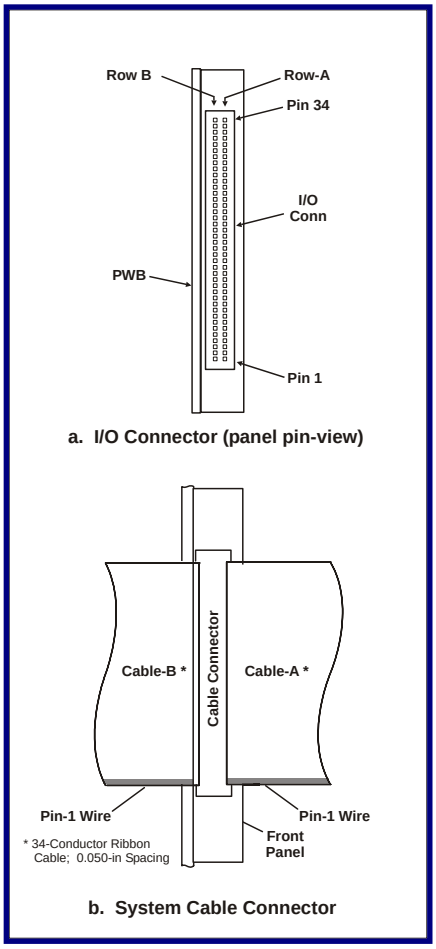

Figure 2.2.2. System I/O Connections

2.3 Analog Input Configuration

The analog inputs are configured as four differential input pairs. Differential operation provides the highest noise immunity, and is recommended for the majority of applications. Pull-down resistors are provided on all analog inputs. Although the input configuration is differential, single-ended signal sources can be accommodated as described in Paragraph 2.3.2.

2.3.1 Differential Inputs

Differential operation is essential when the input source returns are at different potentials. This operating mode also offers the highest rejection of the common mode noise that is characteristic of long unshielded cables. When operating in the differential mode, shown in Figure 2.3.1a, the wire pair from each signal source is connected between the HI(+) and LO(-) inputs of a single input channel. The input return should be connected to system ground (remote common) as closely as possible to the input sources. The average HI/LO signal level relative to the input return is the common mode voltage **Vcm** which, for optimum performance, must not exceed the maximum value indicated in the product specification.

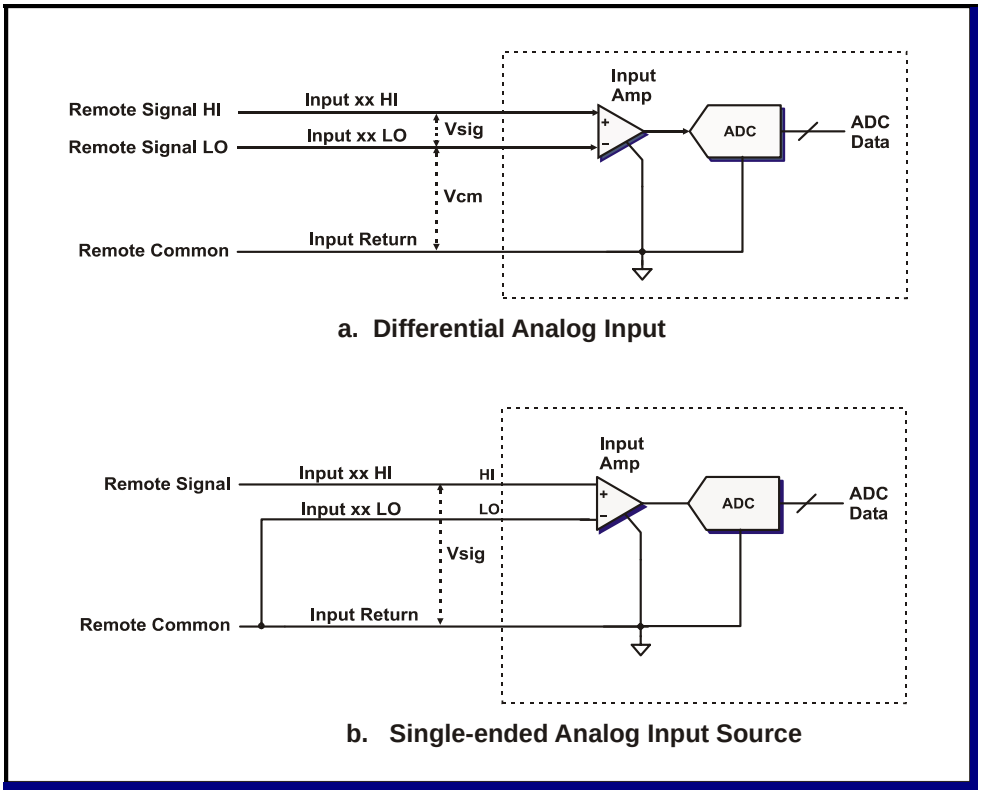

Figure 2.3.1. Input Configurations

2.3.2 Single-Ended Input Sources

Single-ended signal sources can be accommodated as shown in Figure 2.3.1b, with the signal line connected to INP CHAN XX HI, and the associated INP CHAN XX LO input connected to INPUT RETURN at the source. The single-ended operating connection provides suitable performance only when the input signal sources either are isolated from each other, or are common only to a single isolated signal return.

CAUTION: If a significant potential difference exists between the remote signal return and INPUT RETURN, a low impedance between the two returns can cause excessive current to flow. This in turn can cause erroneous measurements or possible damage to the board. Return-current should be controlled to less than a few milliamps for best performance, and to less than 100 milliamps to avoid damage.

2.4 Multiboard Clocking and Synchronization

Analog input converters on multiple boards can be:

a. Clocked from a single clock source (Multiboard clocking), and/or:

b. Synchronized to a common time reference (Multiboard synchronization).

Clocking multiple converters from a single source prevents the *sampling drift* that occurs when converters are clocked from different sources. *Synchronizing* the converters on multiple boards causes the converters to initiate conversions simultaneously, and can be used to eliminate *sampling skew* between channels.

2.4.1 Interboard Connections

Figure 2.4.1 illustrates how multiple PC104P-24DSI12-4-16SDI boards can be daisy-chained together in an initiator-target sequence to provide common clocking between boards. The CLOCK OUTPUT lines from an initiator are connected to the CLOCK INPUT lines on a target board, and the SYNC output and input pairs are connected similarly. Each target board can serve as an initiator for another target board, and multiple boards can be daisy-chained together for synchronous operation.

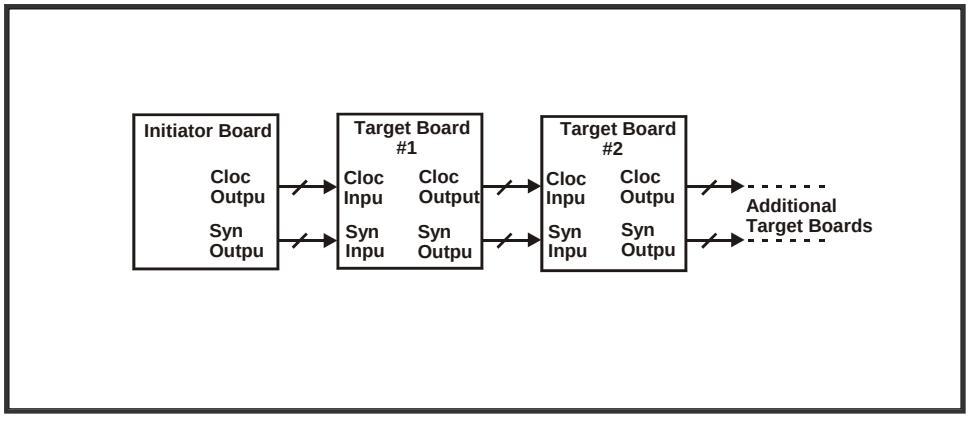

Figure 2.4.1. Multiboard Clock/Sync Connections

By using an external clock and sync distribution module, multiple boards can be interconnected in a 'star' configuration to eliminate the clock and sync propagation delay introduced by each board in a daisy chain configuration.

The clock output signal is generated internally on an initiator board, or is a duplicate of the clock input signal on a target board. Similarly, the sync output is the software-generated sync signal on an initiator board, or a duplicate of the sync input signal on a target board.

Note: External clocking can require frequencies up to 32MHz, which could restrict cable lengths for TTL signals.

Because each board provides active clock and sync outputs for the next board in the chain, the number of boards in the chain is limited only if the propagation delay of approximately 10 nanoseconds introduced by each board becomes significant through multiple boards. The external clock and sync I/O signals use TTL signaling. Cable-length between boards should not exceed one meter for general-purpose ribbon cable, while high-quality 100-Ohm cable can extend the length to 10 meters or more.

Application software controls the designation of each board as an initiator or a target, and also selects the channels on each board that will respond to the external clock. Although only software-designated channels respond to the external clock, all channels on all target boards respond to the external sync input.

2.4.2 Multiboard Synchronization

Boards that are interconnected for multiboard synchronization initiate internal *synchronization sequences* each time a sync pulse is generated by the initiator board. The sync I/O can also be used to reset (clear) the data buffers on target boards.

2.5 Maintenance

This product requires no scheduled hardware maintenance other than periodic reference verification. The optimum adjustment interval will vary, depending upon the specific application, but in most instances an interval of one year is recommended. In the event of a suspected malfunction, all associated system parameters, such as I/O cabling, power voltages, and control bus integrity should be evaluated before a board is returned to the factory for problem analysis and repair.

2.6 Reference Verification and Adjustment

All input and output channels are software-calibrated to an internal voltage reference by an embedded autocalibration software utility. This procedure describes the adjustment of the internal reference. For applications in which the system must not be powered down, the adjustment can be performed while the board is installed in an operating system.

2.6.1 Equipment Required

Table 2.6.1 lists the equipment requirements for calibrating the PC104P-24DSI12-4-16SDI board. Alternative equivalent equipment may be used.

Table 2.6.1. Reference Adjustment Equipment

EQUIPMENT DESCRIPTION	MANUFACTURER	MODEL
Digital Multimeter, 5-1/2 digit, 0.005% accuracy for DC voltage measurements at +10 Volts.	Hewlett Packard	34401A
Host system with PCI expansion slot	---	---
Cable connector, with test leads. (Not required if calibration test points are made permanently available at a system connection point)	AMP	749621-9

2.6.2 Adjustment Procedure

The following procedure describes the single adjustment that is necessary to ensure conformance to the product specification. Adjustment of the internal reference (Vtest) is performed with an internal trimmer that is accessible at the analog mezzanine.

This procedure assumes that the board is installed in an operating system, and that the ±5V input range is selected.

1. Connect the digital multimeter between the VTEST OUTPUT (+) and VTEST RETURN (-) pins in the system I/O connector. Refer to Table 2.2.2 for pin assignments.

2. If power has been removed from the board, apply power now and wait at least 15 minutes before proceeding.

3. Select the ±5V input range.

4. Verify that the digital multimeter indication is +4.9500 VDC ±0.0005 VDC. If the indication is not within this range, adjust the REFERENCE ADJUSTMENT trimmer until the digital multimeter indication is within the specified range.

SECTION 3.0

CONTROL SOFTWARE

3.1 Introduction

The PC104P-24DSI12-4-16SDI board is compatible with Revision 2.3 of the PCI Local Bus specification, and the PCI interface is controlled by a PLX™ PCI-9080 PCI adapter. Configuration-space registers are initialized internally to support the location of the board on any 32-longword boundary in memory space.

After initialization, communication between the PCI bus and the board takes place through the control and data registers shown in Table 3.1. All data transfers are long-word D32. Reserved bits in each register are ignored during write operations, and are forced LOW during read operations. To ensure compatibility of applications with subsequent product upgrades, reserved bits should be written LOW.

Table 3.1. Control and Data Registers

LOCAL ADDR	ACCESS MODE *	REGISTER	DEFAULT	DESCRIPTION
00	R/W	**Board Control (BCR)**	0000 383Ch *	Board Control Register (BCR)
04	R/W	**Rate Control A**	0000 0000h	Rate Generator-A control
08	R/W	**Rate Control B**	0000 0000h	Rate Generator-B control.
0C-10	RO	(Reserved)	0000 0000h	---
14	R/W	**Rate Assignments**	0000 0010h	Channel-group rate generator assignment
18	R/W	**Rate Divisors 00-01**	0000 0505h	Channels 00 thru 03 sample rate divisors.
1C	R/W	(Reserved)	0000 0505h	---
20	R/W	(Reserved)	0000 0505h	---
24-34	RO	(Reserved)	0000 0000h	---
38	R/W	**Buffer Threshold**	0000 FFFEh **	Input buffer control and status threshold
3C	RO	**Board Revision**	000X XXXXh	Firmware revision and option straps.
40	RO	**Buffer Size**	000X XXXXh	Number of samples in the input data buffer.
44	R/W	Autocal Values ***	---	---
48	RO (DMA)	**Input Data Buffer**	XXXX XXXXh	Input Data Buffer; Data and channel tag
34-7C	--	(Reserved)	---	---

* Changes to 0000 783Ch when the input buffer fills. R/W = Read/Write; RO = Read-Only.
** Changes to 0100 FFFEh when the buffer fills. *** Maintenance register; Shown for reference only.

3.2 Board Control Register

The Board Control Register (BCR) controls primary board functions, including analog input mode and analog input range. Table 3.2 provides a brief description of each bit field in the BCR, as well as indicating an associated section in the text.

Table 3.2. Board Control Register

Offset: 0000h **Default: 0000 383Ch ****

DATA BIT	MODE	DESIGNATION	DESCRIPTION	SECTION
D00	R/W	AIM0	Analog input mode. Selects system inputs or	3.4
D01	R/W	AIM1	selftest mode. Defaults to system inputs.	
D02	R/W	RANGE0	Analog input range selection.	3.4.2
D03	R/W	RANGE1	Defaults to (Reserved) range	
D04	R/W	OFFSET BINARY	Selects offset binary or two's complement input data format. Defaults HIGH to offset binary.	3.5.2.2
D05	R/W	INITIATOR	Selects INITIATOR or TARGET mode for external clock and sync signals. Defaults to Initiator mode.	3.6.3
D06	R/W	*SOFTWARE SYNC	Initiates a local ADC sync operation when asserted. Also generates an external sync output if INITIATOR mode is selected. Clears automatically.	3.6.3.2
D07	R/W	*AUTOCAL	Initiates an autocalibration operation when asserted. Clears automatically upon completion.	3.7
D08	R/W	INTERRUPT A0	Interrupt event selection. Default is zero.	3.8.1
D09	R/W	INTERRUPT A1		
D10	R/W	INTERRUPT A2		
D11	R/W	INTERRUPT REQUEST FLAG	Set HIGH when the board requests an interrupt. Clears the request when cleared LOW by the bus.	
D12	RO	AUTOCAL PASS	Set HIGH at reset or autocal initialization. Cleared LOW if autocalibration terminates unsuccessfully.	3.7
D13	RO	CHANNELS READY	LOW during any change in channel parameters. Asserted HIGH when ADC clocks are stabilized.	3.4.3
D14	RO	BUFFER THRESHOLD FLAG	Asserted HIGH when buffer contents exceed the assigned threshold.	3.5.3.1
D15	R/W	*INITIALIZE	Initializes the board when asserted HIGH.	3.3.2
D16	R/W	SYNCHRONIZE SCAN	Input channel data is acquired in discrete scans. All active channels must be synchronized and adjusted to a common sample rate.	3.10
D17	R/W	CLEAR BUFFER ON SYNC	Changes the context of the SOFTWARE SYNC control bit changes to CLEAR BUFFER.	3.5.3.2
D18	R/W	(Reserved)	---	---
D19	R/W	FORCE LOW FILTER	When HIGH, selects the low-frequency image filter. When LOW (default), image filter selection is automatic.	3.6.1.4
D20	R/W	TTL EXTERNAL SYNC IO	Enables TTL external sync and clock I/O when HIGH.	3.6.3
D21-31	RO	(Reserved)	---	---

* Cleared automatically. R/W = Read/Write; RO = Read-Only.

** Changes to 0000 783Ch when the input buffer fills.

3.3 Configuration and Initialization

3.3.1 Configuration

Configuration is initiated by a PCI bus RESET, and should be required only once after the initial application of power. During board configuration, initial values for both the PCI configuration registers and the internal control logic are extracted from internal nonvolatile read-only memory. While the PCI configuration registers are being loaded, the response to PCI target accesses is RETRY's. Configuration operations are executed in the sequence shown in Table 3.3.1.

Table 3.3.1. Configuration Operations

Operation	Maximum Duration
PCI configuration registers are loaded from internal EEPROM	3 ms
Internal control logic is configured from internal ROM	300 ms
Internal control logic is initialized	3 ms
A/D converters and clocks are initialized	**5 seconds**

Board configuration terminates with the PCI interrupts disabled. Attempts to access the local bus during configuration should be avoided until the PCI interrupts are enabled and the initialization-complete interrupt request is asserted.

3.3.2 Initialization

Internal control logic can be initialized without invoking configuration by setting the INITIALIZE control bit in the BCR. This action causes the internal logic to be initialized, but does not affect the PCI configuration registers and does not reconfigure the internal control logic. Initialization has a maximum duration of 5 seconds, and produces the following conditions:

- The Initiator mode is selected,
- Synchronous Scanning is disabled,
- The width of the buffer data field is adjusted to 16 bits,
- Both rate generator are adjusted to 15.6 MHz (Fgen = 7.68MHz),
- All rate divisor are preset to 5,
- The input voltage range is set to "Reserved" (Paragraph 3.4.2),
- Sample rates are 24 KSPS; i.e.: 7.68MHz / (64 *5).
- Channel groups 0 and 1 are controlled by rate generators A and B, respectively,
- The analog input buffer is reset to empty; buffer threshold equals 0000 FFFEh,
- ADC clocking is enabled; data is accumulating in the input buffer,
- All control registers are initialized; all defaults are invoked,
- The local interrupt request is asserted as an initialization-completed event.

Upon completion of initialization, the INITIALIZE control bit is cleared automatically.

3.4 Analog Input Configuration

Configuration of the analog input networks is controlled by the BCR bit field designated as AIM[1..0] as shown in Table 3.4. The analog input selection arranges all input channels in differential configuration during normal operation, or invokes one of two selftest modes.

Table 3.4. Analog Input Function Selection

AIM[..0]	FUNCTION OR MODE
0	Differential analog input mode.
1	(Reserved).
2	ZERO test. Internal ground reference is connected to all analog input channels.
3	+VREF test. Internal voltage reference is connected to all analog input channels.

3.4.1 Selftest Modes

Two selftest modes provide the ability to verify the accuracy of any or all input channels by replacing the system input connections with either a precision internal reference voltage (+VREF) or a zero reference (ZERO). The +VREF test produces a positive value equal to 99.00 percent of the selected input range (e.g. +4.950 Volts for the ±5 Volt range) from all input channels, and the ZERO test produces a value equivalent to 0.000 Volts. The accuracy expected of selftest measurements should correspond to the product accuracy specification.

NOTE: For maximum test accuracy, the internal reference voltage must be allowed to settle completely when the test mode is changed. After selecting either of these test modes, insert the indicated minimum settling delay before acquiring test values:

ZERO test: 100 milliseconds, +VREF test: 3 seconds.

3.4.2 Input Range Selection

Any one of two input voltage ranges can be selected for all channels. The RANGE[1..0] control field in the BCR selects the input range as shown in Table 3.4.2.

Table 3.4.2. Analog Input Range Selection

RANGE[1..0]	ANALOG INPUT RANGE
0	±2.5 Volts
1	±2.5 Volts
2	±5 Volts
3	(Reserved)

3.4.3 Settling Delays and the Channels Ready Flag

When a critical parameter such as input mode or sample rate is changed, a settling transition occurs during which input measurements are unpredictable. A settling delay is inserted automatically when any or all of these parameters are changed, and the CHANNELS READY status flag in the BCR goes LOW during the delay. A LOW-to-HIGH transition of this flag is selectable as an interrupt request "channels ready" event (Section 3.8.1). The CHANNELS READY flag goes low during the following operations for the approximate intervals indicated:

5 Seconds:	Board initialization (3.3),
1 us:	Buffer reset, if not in synchronous-scanning mode (3.5.3.2),
10 us-5 ms:	Buffer reset, if in synchronous-scanning mode (3.5.3.2),
500 ms:	Sample rate change ; i.e.: Nrate, Ndiv, Rate assignments (3.6).
1-500 ms:	ADC synchronization (3.6.2 and 3.10),
1-500 ms:	Synchronous-scan initiation (3.10),

3.5 Input Data Buffer

3.5.1 General Characteristics

Analog input samples accumulate in the analog input data FIFO data buffer, which has a capacity of 256K data values. Data accumulates in the buffer until extracted by the PCI bus from a single register location, indicated as INPUT DATA BUFFER in Table 3.1. Reading an empty buffer returns an indeterminate value.

3.5.2 Data Organization

Each value in the data buffer consists of a channel tag field, a zero-pad field, and a data field, as shown in Table 3.5.2. The width of the right-justified data field is adjustable from 16 bits to 24 bits by the buffer threshold register (Table 3.5.3), and the width of the zero-pad field is adjusted accordingly. The zero-pad field becomes a sign-extension field if two's complement data coding is selected.

Table 3.5.2. Input Data Buffer Organization

Offset: 0000 0048h **Default: XXXX XXXXh**

SELECTED DATA WIDTH	RESERVED (Zero)	CHANNEL TAG	ZERO-PAD	CHANNEL DATA VALUE
16 Bits	D[31..19]	D[18..16]	---	D[15..0]
18 Bits	D[31..29]	D[28..24]	D[23..18]	D[17..0]
20 Bits	D[31..29]	D[28..24]	D[23..20]	D[19..0]
24 Bits	D[31..29]	D[28..24]	---	D[23..0]

3.5.2.1 Channel Tags

If the input channels are not scan-synchronized (Paragraph 3.10), the order in which channel data accumulates in the buffer is not generally predictable. Therefore, a channel tag that identifies each input channel is attached to each data value in the buffer.

.

3.5.2.2 Input Data Format

Input data values can be represented either in offset binary format by asserting the OFFSET BINARY control bit HIGH (default state) in the BCR, or in two's complement format by clearing the control bit LOW. Both coding conventions are illustrated for 16-Bit data in Table 3.5.2.2.

Table 3.5.2.2. Analog Input Data Coding; 16-Bit Data Field

	DIGITAL VALUE (Hex)	
ANALOG INPUT LEVEL	**OFFSET BINARY**	**TWO'S COMPLEMENT**
Positive Full Scale minus 1 LSB	FFFFh	7FFFh
Zero plus 1 LSB	8001h	0001h
Zero	8000h	0000h
Zero minus 1 LSB	7FFFh	FFFFh
Negative Full Scale plus 1 LSB	0001h	8001h
Negative Full Scale	0000h	8000h

Positive Full Scale is a positive level that equals the selected input voltage range for the board (e.g.: +5.000 Volts for the ±5V range). *Negative Full Scale* is the negative equivalent of positive full-scale. *Full-scale Range* (FSR) is the total input voltage range. For 16-Bit data, one LSB equals the full-scale range divided by 65,536. (e.g.: 152.59 microvolts for the ±5V range).

3.5.3 Buffer Threshold Register

The buffer threshold register (Table 3.5.3) contains the threshold value for the buffer status flag, and also provides control bits for clearing or disabling the buffer and for selecting the number of bits in the data field.

Table 3.5.3. Buffer Threshold Register

Offset: 0000 0038h **Default: 0000 FFFEh**

BIT FIELD	MODE	DESIGNATION	FUNCTION
D[17..00]	R/W	BUFFER THRESHOLD	Buffer Flag Threshold (duplicated in the BCR)
D[18]	R/W	DISABLE BUFFER INPUT	Disables inputs to the data buffer.
D[19]	R/W	CLEAR BUFFER *	Clears (empties) the buffer
D[21..20]	R/W	DATA WIDTH	Controls the width of the buffer data field as: 0 => 16 bits 1 => 18 bits 2 => 20 bits 3 => 24 bits.
D[31..22]	RO	(Reserved)	---

* Clears automatically.

NOTE: Since delta-sigma ADC's perform conversions continuously, the initiation and termination of acquisition sequences is controlled by the buffer's 'Clear' and 'Disable' controls.

3.5.3.1 Status Flag and Threshold

The amount of data contained in the input buffer can be used to control the BUFFER THRESHOLD FLAG status bit, which can be selected as an interrupt request event. The interrupt request event can be selected to occur on either the rising or falling edge of the flag (Table 3.8.1).

The threshold flag is asserted HIGH when the number of samples in the buffer ***exceeds*** the BUFFER THRESHOLD value in the buffer threshold register. A buffer-empty event is produced when the threshold value is adjusted to equal 0000 0000h and the threshold flag undergoes a HIGH-to-LOW transition.

3.5.3.2 Buffer Clearing and Disabling

Asserting the CLEAR BUFFER control bit in the buffer threshold register resets (empties) the buffer, and holds the buffer in reset for approximately 10 microseconds to allow the internal data pipeline to empty. This bit clears automatically.

Asserting the DISABLE BUFFER INPUT control bit disables inputs to the buffer from the ADC input channels, and halts the accumulation of further input data. Input data already present in the buffer when this bit is asserted remains in the buffer.

Note: The buffer also can be cleared by writing a "one" to the SOFTWARE SYNC control bit in the BCR while the CLEAR BUFFER ON SYNC control bit is HIGH. See "Global Buffer Clear" in Section 3.10.

3.5.4 Buffer Size Register

This read-only register contains the number of analog input values currently stored in the input data buffer.

3.6 Input Sampling Control

The local controller establishes the following input sampling parameters:

a. Sample rate,
b. Interchannel phase, or skew,
c. Channel synchronization.

The effective input bandwidth is determined by the sample rate, while phase and synchronization control the relative timing of sampling between multiple channels. Phase and synchronization are considerations in applications that require consistent relative timing of sampling among multiple channels or multiple boards.

Clocking multiple converters from a single sample rate clock prevents the *sampling drift* that occurs when converters are clocked from different sources. *Synchronization* causes the converters in all channels to initiate conversions simultaneously, and can be used to eliminate *sampling skew* between channels.

3.6.1 Sample Rate Control

3.6.1.1 Rate Clock Organization

Sample rates are derived from two internal, independent rate generators, or from a single external hardware clock, as shown in Figure 3.6.1.1. All available input channels are divided equally into two sample groups, and the sample rates for all channels are controlled by the following operations:

a. Assignment of each group to an internal rate generator or to the external clock,
b. Rate generator frequency selection,
c. Rate divisor selection.

3.6.1.2 Rate Generator Assignment

A 4-bit code RATE SOURCE in the Rate Assignments register selects either an internal rate generator or the external sample rate clock as sample rate source. Group selection codes are arranged in the register as shown in Table 3.6.1.2-1, and use the assignment codes listed in Table 3.6.1.2-2. Channels in a group with a rate assignment of "none" are disabled and do not provide data to the input data buffer.

Note: If scan-synchronization is selected (Section 3.10), the ADC's in all channels are clocked by the Channel-00 ADC clock.

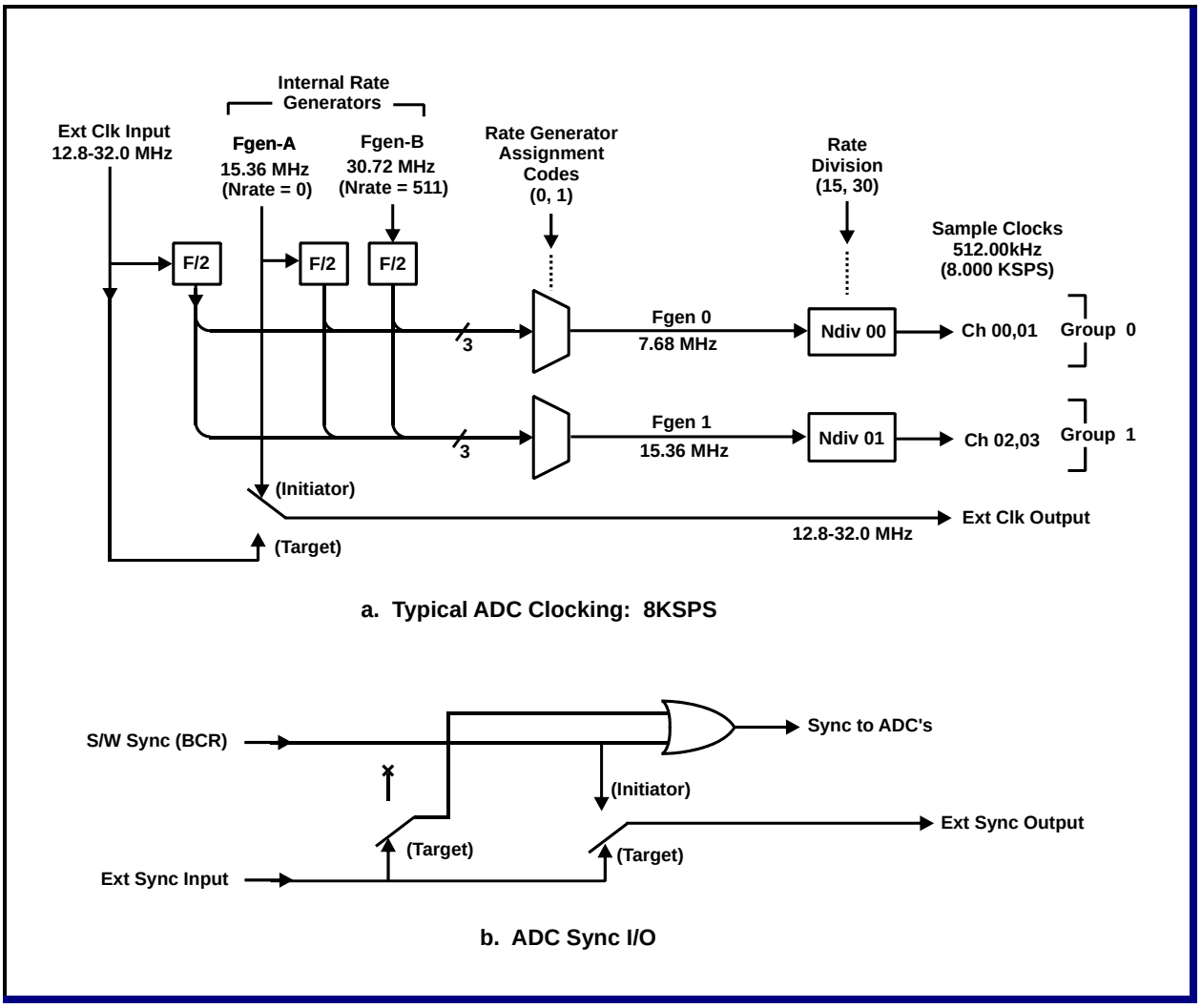

Figure 3.6.1.1. ADC Clock and Sync Organization

Table 3.6.1.1. Channel Groups

CHANNEL GROUP	INPUT CHANNELS
0	00, 01
1	02, 03

Table 3.6.1.2-1. Rate Assignments Register

Offset: 0000 0014h **Default: 0000 0010h**

BIT FIELD	DESIGNATION	CHANNEL GROUP
D[03..00]	GROUP 0 RATE SOURCE	0
D[07..04]	GROUP 1 RATE SOURCE	1
D[31..08]	(Reserved)	---

Table 3.6.1.2-2. Rate Generator Assignment Codes

ASSIGNMENT CODE	RATE CLOCK SOURCE
0	Rate Generator-A
1	Rate Generator-B
2	(Reserved)
3	(Reserved)
4	External Sample Clock (as Rate-A generator input)
5-7	None (Disabled)
8-15	(Reserved)

3.6.1.3 Sample Clock Generation

A rate divisor integer **Ndiv** controls a *rate divisor* for the rate generator or external clock input. Rate divisors are arranged in the Rate Divisor register as shown in Table 3.6.1.3.

Table 3.6.1.3. Rate Divisor Register

Offset: 0018h **Default: 0000 0505h**

	CHANNEL DIVISORS; Ndiv = 3-60
BIT FIELD:	**Rate Divisors 00-01**
D[07..00]	Channels 00,01
D[15..08]	Channels 02,03
D[31..16]	(Reserved)

NOTE: When operating a channel group above 50 KSPS, all channel divisors for that group must be adjusted to the same value; either "1" or "2."

The ADC sample rate **Fsamp** is determined by the rate generator frequency **Fgen** and a rate **DIVISOR** as: (all values in decimal)

$$\textbf{Fsamp = Fgen / (64 * Ndiv),} \qquad \textbf{(3-1)}$$

where **Fsamp** and **Fgen** are in kilohertz, where **Ndiv** can have any integer value from zero through 60, and **Fgen** has a range of:

7.68-15.36 MHz for Fsamp = 2 - 50 KSPS, Ndiv = 3-60,

6.40-12.80 MHz for Fsamp = 50 - 200 KSPS, Ndiv = 1, 2.

If the clock source is an internal rate generator, **Fgen** is determined by **Nrate** as described in Paragraph 3.6.1.4. If the source is the external clock input, then **Fgen** is determined by the external clock.

3.6.1.4 Rate Generator Control

Each of the internal Rate-A and Rate-B generators is a PLL-controlled oscillator locked to a stable reference frequency. The frequencies of these generators are controlled by the Rate Control A and Rate Control B registers listed in Table 3.1.

The frequency **Fgen** of each oscillator is related to a reference frequency **Fmin** and an integer **Nrate** as:

$$\textbf{Fgen (MHz) = Fmin * (1 + } \frac{\textbf{Nrate}}{\textbf{511}} \textbf{),} \qquad \textbf{(3-2)}$$

where **Fmin** is in Megahertz. **Nrate** is the value in the Rate-A or Rate-B control register, and can have any value from zero through 554. **Fmin** has a value of 7.68 MHz for divisors of 3-60, or 6.40 MHz for divisors of 1 and 2 (Table 3.6.1.4-1):

Table 3.6.1.4-1. Rate Generator Control

Fsamp Range	Ndiv	Nrate Range	Fgen Range	ADC Mode	Fmin
2-50 KSPS	3-60	0-554	7.68-16.00 MHz	Single speed	7.6800 MHz
50-100 KSPS	2	0-511	6.40-12.80 MHz	Dual speed	6.400 MHz
100-200 KSPS	1	0-511	6.40-12.80 MHz	Quad speed	6.400 MHz

The ADC's operate in one of three different clocking modes, with each mode determined by the assigned sample rate. In addition to establishing the sample rate division factor, the integer **Ndiv** also controls the ADC clocking mode.

Table 3.6.1.4-2 lists some examples of ADC clocking control parameters.

Table 3.6.1.4-2. ADC Clocking Control Examples

Rate Control (Nrate)	Channel Group Frequency (Fgen), MHz	Divisor (Ndiv)	Sample Rate (Fsamp), KSPS
0	7.680	**15**	**8.000 ***
511	15.360	**30**	**8.000 ***
511	15.360	**15**	**16.000**
511	15.360	**5**	**48.000**
426	14.083	**10**	**22.00 ****
426	14.083	**5**	**44.00 ****
0	6.400	**2**	**50.00**
511	12.800	**2**	**100.00**
511	12.800	**1**	**200.00**

* Telephony applications.
** Harmonically locked if all channels are assigned to the same rate generator.

NOTE: An inline analog image filter suppresses images of the sample rate that are generated by the ADC's internal digital filter. Two separate fixed-frequency filters are available in each channel, as identified in the product specification. If FORCE LOW FILTER is LOW in the BCR, selection of the filter is automatic, with the high-frequency filter selected for Ndiv values less than 8, and the low-frequency filter selected for values of 8 or greater. If FORCE LOW FILTER is HIGH, then the low-frequency filter is selected in all channels, regardless of the value for Ndiv

3.6.1.5 Harmonically Locked Channels

Channel groups operating at different frequencies that are exact submultiples of a common frequency perform conversions repetitively, relative to a sampling frame, and are *harmonically locked*.

3.6.2 Channel Synchronization

Due to the oversampling nature of delta-sigma conversion, each conversion represents a sampling interval consisting of multiple clock cycles, and simply operating all converters from a common clock does not ensure simultaneous, or skew-free, sampling. To ensure simultaneous sampling, the converters must be synchronized to perform conversions simultaneously relative to a common point in time. Thereafter, the converters will continue to sample simultaneously while operating from a common clock.

Synchronization is invoked by setting the SOFTWARE SYNC control bit HIGH in the BCR. Completion of the synchronization sequence is indicated by the CHANNELS READY flag in the BCR undergoing a Low-to-High transition (Paragraph 3.4.3). The CHANNELS READY transition can be selected as a condition for an interrupt request event.

3.6.3 Multiboard Operation

Multiple PC104P-24DSI12-4-16SDI boards can be connected together to share a common sampling clock and synchronization command. One of the boards is designated as the *initiator*, and the remaining boards are designated as *targets*.

3.6.3.1 External Sample Clock

Clock target boards receive an external clock from the external clock input connection, and duplicate the input clock at the external clock output connection (Figure 3.6.1.1). For calculation of target board sample rates, the **Fgen** frequency discussed in Section 3.6.1.3 is 1/2 the external input clock frequency.

A board is a *clock target* if "External Sample Clock" is selected in the rate assignments register, or is a *clock initiator* for all other rate assignments.

A clock ***initiator*** provides an external clock output directly from the Rate-A generator, while a *target* simply passes the external clock input to the external clock output. Multiple boards can all be configured as initiators and operated in a "star" configuration to operate from a single rate generator. To avoid overloading the TTL source driver, an TTL distribution module may be required in this configuration.

NOTE: The TTL EXTERNAL SYNC-IO control bit in the BCR must be set HIGH to enable the external clocking and sync hardware interface.

3.6.3.2 External Sync

Boards that are hardware-configured for multiboard synchronization execute a *synchronization sequence* each time a sync pulse is generated by the initiator board.

A board is a *sync initiator* if the INITIATOR control bit is HIGH in the BCR, or is a sync target if the bit is LOW.

The SOFTWARE SYNC control bit in the BCR can be used also to clear the buffers on the initiator and target boards simultaneously, by first setting the CLEAR BUFFER ON SYNC control bit HIGH in the BCR.

A ***sync initiator*** provides an external sync output from the SOFTWARE SYNC control bit, while a ***sync target*** passes the external sync input directly to the external sync output.

3.7 Autocalibration

Autocalibration is an embedded utility that calibrates all input channels to a single internal voltage reference. Offset and gain error corrections for each channel are determined during autocalibration, and are applied to each channel in real-time during data acquisition. The correction values are retained until either: (a) power is removed, (b) a PCI reset occurs, or (c) autocalibration is invoked again. Autocalibration is invoked by setting the AUTOCAL control bit HIGH in the BCR. Completion of autocalibration is indicated by the AUTOCAL flag clearing automatically to the LOW state. Clearing of the AUTOCAL control bit is selectable as an interrupt request event.

An autocalibration sequence has a typical duration from 1 to 5 seconds, depending upon the selected sample rate and number of active channels. Read or write access from the PCI bus during autocalibration may disrupt the calibration process, and should be avoided. Either a suitable delay or the "Autocal Completed" interrupt should be used to detect the end of autocalibration.

If a board is defective, the autocalibration process may be unable to successfully calibrate all input channels. If this situation occurs, the AUTOCAL PASS status flag in the BCR will be LOW when the autocal sequence is completed. A HIGH state for AUTOCAL PASS indicates that autocalibration was successful.

To ensure full conformance to the product specification, autocalibration should always be invoked after:

a. Power has been applied to the board,
b. A PCI reset event has occurred,
c. The input range, clock source or sampling rate has been altered,
d. A scan-synchronization sequence has been performed (Section 3.10).

Autocalibration can be invoked at any time, but should not occur while the system is experiencing a major environmental transition such as that which usually occurs directly after power is applied. For optimum performance, a warmup delay of 15 minutes is recommended.

3.8 Interrupt Control

In order for the board to generate a PCI interrupt on INTA#, *both* of the following conditions must occur:

a. The internal controller must generate a Local Interrupt Request
b. The *PCI interrupt* must be enabled.

If the internal controller generates a local interrupt request, a PCI bus interrupt will not occur unless the PCI interrupt has been enabled as described below in Paragraph 3.8.2.

3.8.1 Local Interrupt Request

The single local interrupt request line is controlled by the INTERRUPT A[2:0] and INTERRUPT REQUEST FLAG control bits in the BCR. The condition for the interrupt request is selected as shown in Table 3.8.1. When the selected condition occurs, a local interrupt request is generated and the INTERRUPT REQUEST FLAG bit is set in the BCR. The request remains asserted until the PCI bus clears the BCR request flag. A local interrupt request is generated automatically at the end of initialization.

Detection of an interrupt condition or event is *edge-sensitive*. An interrupt request is generated if, and only if, a specific interrupt condition undergoes a *transition* from 'false' (not-true) to 'true' while that condition is selected.

Table 3.8.1. Interrupt Event Selection

INTERRUPT A[2:0]	INTERRUPT EVENT CONDITION
0	Initialization completed. Default state.
1	Autocal completed
2	Channels Ready
3	Data Buffer threshold flag, LOW-to-HIGH transition
4	Data Buffer threshold flag, HIGH-to-LOW transition
5	(Reserved)
6	(Reserved)
7	(Reserved)

3.8.2 Enabling the PCI Interrupt

A local interrupt request will not produce an interrupt on the PCI bus unless the PCI interrupt is enabled. The PCI interrupt is enabled by setting the *PCI Interrupt Enable* and *PCI Local Interrupt Enable* control bits HIGH in the runtime *Interrupt Control/Status Register* described in Section 4 of the PLX^{TM} PCI-9080 reference manual..

3.9 DMA Operation

DMA transfers from the analog input buffer are supported in either of two DMA channels with the board operating as bus master. Table 3.9.1 illustrates a typical PCI register configuration that controls a non-chaining, non-incrementing '***block-mode'*** Channel-0 DMA transfer, in which a PCI interrupt is generated when the transfer has been completed. Bit 02 (0000 0004h) in the PCI Command register must be set HIGH to select the bus mastering mode. Refer to a PCI-9080 reference manual for a detailed description of these registers.

Table 3.9.1. Typical DMA Register Configuration; DMA Channel-0

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Analog Input Buffer local address (Analog input buffer)	0000 0048h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction; Local bus to PCI bus (Analog inputs)	0000 000Ah
A8h	DMA Command Status	Command and Status Register	0000 0001h 0000 0003h (See Text)

* Determined by specific transfer requirements.

For most applications, the DMA Command Status register would be initialized to the value 0000 0001h, and then changed to 0000 0003h to initiate a transfer.

Bit-12 (0000 1000h) in the Channel-0 DMA Mode configuration register, when HIGH, selects ***'demand-mode'*** DMA operation, in which a DMA transfer is requested automatically when the number of values in the buffer ***exceeds the selected buffer threshold*** *(Table 3.5.3).*

The DMA request is sustained until one of the following events occurs:

(a) The data buffer goes empty,
(b) The number of values read from the buffer equals the threshold value *plus one*,
(c) The buffer is cleared,
(d) The board is reset,
(e) Autocalibration is executed.

The first occurrence of any of these events terminates the DMA request.

3.10 Scan Synchronization

Although the data sequence for any specific channel in the data buffer represents the actual sampling sequence for that channel, the ordering of multiple channels in the buffer can vary due to the asynchronous nature of the sample clock relative to the board's master clock. These variations in channel order can occur even though all channels are synchronized to a common sample clock.

Variations in the ordering of multiple channels can be eliminated by synchronizing the acquisition of each scan to the board's master clock. This ***scan-synchronization*** can be effective only if all active channels are operating from a common clock source.

Note: References to *channel synchronization* in this manual pertain to the situation in which the sampling of all input channels occurs simultaneously. *Scan-synchronization* refers to the synchronization of discrete data scans to the master clock, to ensure a consistent ordering of data channels in the data buffer.

For synchronized scans, the channel sequence for each scan in the buffer is ordered from lowest to highest. All samples in each scan represent the same sample event, and are arranged beginning with the lowest active channel and proceeding upward through the highest active channel. Table 3.10.1 illustrates examples of channel sequences in both synchronized and nonsynchronized scans in which four channels are active.

Table 3.10.1. Channel Order (Channels 00-03 active)

	CHANNEL ORDER	
SAMPLE EVENT	NON-SYNCHRONIZED SCANS (Typical)	SYNCHRONIZED SCANS
Tn	3012	0123
Tn+1	2301	0123
Tn+2	0123	0123
Tn+3	1230	0123
Tn+4	2301	0123

3.10.1 Single-Board Scan Synchronization

Synchronous scanning is disabled after a board reset. To enable synchronous scanning, set the SYNCHRONOUS SCAN control bit HIGH in the BCR, and wait for the CHANNELS READY flag (3.4.3) in the BCR to undergo a LOW-to-HIGH transition. While the CHANNELS READY flag is LOW, the following sequence is executed by the local controller:

1. The Group-0 sample clock (Section 3.6.1) is distributed to all input channels,
2. All ADC's are channel-synchronized (Section 3.6.2),
3. All channels are scan-synchronized.

The buffer clears to empty, and the first two scans are discarded to ensure full synchronization. Subsequent samples are scan-synchronized as described above. The Channels-Ready flag can be used to generate an interrupt at the end of the process.

Notice that all enabled input channels receive the sample clock selected for Group-0 *while operating in the scan-synchronized mode*, and the sample clock settings for Group-1 are ignored. A disabled group remains disabled.

3.10.2 Multiple-Board Scan Synchronization

Use the following sequence to establish synchronous scanning of multiple boards (Paragraph 3.6.3)

Synchronize ADC's:

1. On all boards: Set SYNCHRONOUS SCAN;
   Wait for Channels Ready LOW-to-HIGH on all boards (LOW 1-100ms).
   (Sampling is synchronized on each board, but is sample-skewed between boards)
2. On the Initiator: Set SOFTWARE SYNC;
   Wait for Channels Ready LOW-to-HIGH on all boards (LOW 1-100ms).
   (All ADC's are scan synchronized; but data in the buffers is still skewed)

Global Buffer Clear:

3. On all boards: Set the CLEAR BUFFER ON SYNC bit,
4. On the Initiator: Set SOFTWARE SYNC;
   Wait for Channels Ready LOW-to-HIGH on the initiator. (LOW 10us to 5ms),
   (All ADC's and buffers are now scan-synchronized)
5. On all boards: Clear the CLEAR BUFFER ON SYNC bit.

For optimum DC performance, execute autocalibration on all boards after synchronizing the ADC's on all boards, and follow the procedure with a 'global clear' operation.

NOTE: If autocalibration is executed while scan-synchronized, repeat the global buffer clear sequence (Steps 3 through 5). To simplify this operation, the CLEAR BUFFER ON SYNC control bit can remain HIGH while scan- synchronized.

3.11 Firmware Revision Register

The read-only firmware revision register (Table 3.11.1) contains the existing firmware revision and a status field that indicates the availability of optional features.

Table 3.11.1. Firmware Revision Register

Offset: 0000 003Ch **Default: 000X XXXXh**

BIT FIELD	DESCRIPTION
D00-D11	Firmware Revision *
D12-D14	(Reserved firmware field).
D15	High (Both demand-mode and block-mode DMA are available).
D16	High if 4 input channels are present.
D17	(Reserved)
D18-D31	(Reserved)

* The firmware revision extends through D15.

SECTION 4.0

PRINCIPLES OF OPERATION

4.1 General Description

The PC104P-24DSI12-4-16SDI board contains two dual delta-sigma 24-Bit A/D converters and all supporting functions necessary for adding analog I/O capability to a PMC site. A PCI interface adapter (Figure 4.1) provides the interface between the controlling PCI bus and an internal local controller through a 32-bit local bus. The local controller performs all internal configuration and data manipulation functions, including autocalibration.

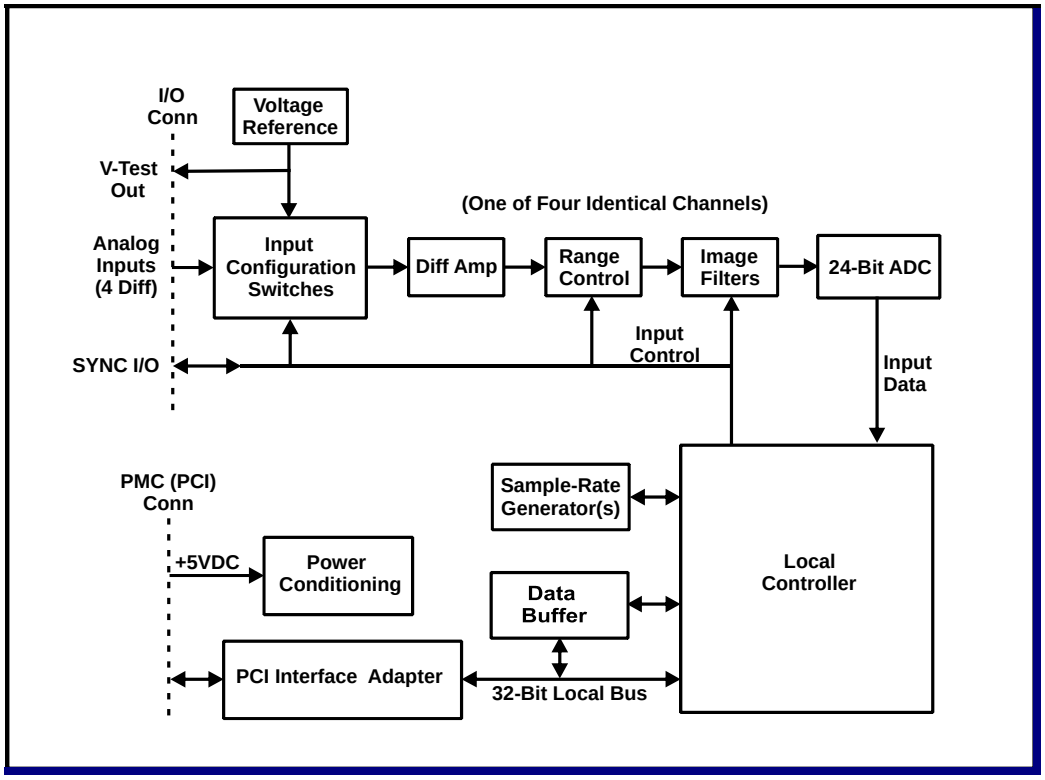

Figure 4.1. Functional Block Diagram

Input configuration switches allow the controller to select any of several signal sources as inputs to the ADC's. This feature is used to establish the internal connections necessary during autocalibration, and also permits verification from the PCI bus of the integrity of all analog input channels. All channels are calibrated against a single precision voltage reference. The offset and gain calibrations for each input channel are adjusted with correction values that are determined during autocalibration.

4.2 Analog Inputs

The analog input channels are arranged in two channel groups, with each group containing one-half of the channels present on the board. Either group can be designated as either active or inactive, with only active groups sending input data to the data buffer. Analog-to-digital conversions can be performed on signals from any of several sources, which are selected by the input configuration switches shown in Figure 4.1. During normal operation, the analog input signal passes through a differential amplifier which removes any common mode voltage that might be present. During selftest and autocalibration operations, the input configuration switches can be used to replace the system input signal with either a precision zero (ground) or positive full-scale reference voltage.

A range control attenuator adjusts the maximum level of the signal to the full-scale input range of 2.0 VRMS required by the ADC. High frequency noise and digital filter images are attenuated by a 2-pole Butterworth lowpass filter, the cutoff frequency of which can be selected from either of two fixed frequencies.

The final conditioned, scaled and filtered input signal is digitized by each ADC into a 24-BIt serial data word that is deserialized into parallel format by the local controller. The local controller then attaches a channel tag to the data word, applies offset and gain corrections, and finally transfers the corrected data to the input data buffer.

Antialias filtering is provided by each ADC in the form of a lowpass digital filter with a sharp cutoff frequency at approximately 40-50 percent of the sampling frequency. The digital filter has no filtering effect at multiples of the sampling clock, which is an integer multiple of the sampling frequency. To prevent extraneous signal frequency components within these "filter images" from appearing in the passband, the hardware image filters shown in Figure 4.1 can be configured to provide filtering within the digital filter images.

4.3 Autocalibration

Autocalibration is an embedded firmware utility that calibrates all input channels to a single internal voltage reference. Application software can invoke the utility at any time.

The offset error of each channel is determined first, by selecting a zero input reference level and storing the values reported from all channels. A precision internal voltage reference then is used to calculate the gain error, and both offset and gain correction values are stored in internal RAM for retrieval during data acquisition.

The internal voltage reference is adjusted to equal 99.00 percent of the selected input voltage range. This in-range value ensures that the ADC's will provide the nonsaturated, or in-range, responses that are necessary during the calibration adjustment process.

4.4 Sampling Clocks

Each of two internal sample rate generators provides a frequency range of 15.36 - 30.72 MHz for sample rates below 50 KSPS, or 12.80 - 25.60 MHz for 50-200 KSPS. The rate generator frequency is divided down by a software-specified integers to provide sample rates from 2 KSPS to 200 KSPS. Either generator can be assigned to either channel group.

An external clock output can replace output of the rate generator. A board from which a rate generator or ADC sample clock originates is a *clock initiator*. Boards that receive and retransmit the external clock are *clock targets*. Multiple targets can be controlled from a single initiator.

4.5 Power Control

Regulated supply voltages of +5 Volts, +6 Volts and ±14 Volts are required by the internal analog networks. Multiple DC/DC converters in the power conditioner use +5V input power from the PCI bus to produce preregulated DC voltages that subsequently are postregulated with linear regulators to the required supply voltages. Linear regulators ensure that the final power voltages delivered to the analog networks are well-regulated and free of noise.

APPENDIX A

LOCAL REGISTER QUICK REFERENCE

APPENDIX A

LOCAL REGISTER QUICK REFERENCE

This appendix summarizes all local registers in the order in which they appear in Section 3.

Table 3.1. Control and Data Registers

LOCAL ADDR	ACCESS MODE *	REGISTER	DEFAULT	DESCRIPTION
00	R/W	**Board Control (BCR)**	0000 383Ch *	Board Control Register (BCR)
04	R/W	**Rate Control A**	0000 0000h	Rate Generator-A control
08	R/W	**Rate Control B**	0000 0000h	Rate Generator-B control.
0C-10	RO	(Reserved)	0000 0000h	---
14	R/W	**Rate Assignments**	0000 0010h	Channel-group rate generator assignment
18	R/W	**Rate Divisors 00-01**	0000 0505h	Channels 00 thru 03 sample rate divisors.
1C	R/W	(Reserved)	0000 0505h	---
20	R/W	(Reserved)	0000 0505h	---
24-34	RO	(Reserved)	0000 0000h	---
38	R/W	**Buffer Threshold**	0000 FFFEh **	Input buffer control and status threshold
3C	RO	**Board Revision**	000X XXXXh	Firmware revision and option straps.
40	RO	**Buffer Size**	000X XXXXh	Number of samples in the input data buffer.
44	R/W	Autocal Values ***	---	---
48	RO (DMA)	**Input Data Buffer**	XXXX XXXXh	Input Data Buffer; Data and channel tag
34-7C	--	(Reserved)	---	---

* Changes to 0000 783Ch when the input buffer fills.
** Changes to 0100 FFFEh when the buffer fills.
R/W = Read/Write; RO = Read-Only.
*** Maintenance register; Shown for reference only.

Table 3.2. Board Control Register

Offset: 0000h **Default: 0000 383Ch ****

DATA BIT	MODE	DESIGNATION	DESCRIPTION	SECTION
D00	R/W	AIM0	Analog input mode. Selects system inputs or selftest mode. Defaults to system inputs.	3.4
D01	R/W	AIM1		
D02	R/W	RANGE0	Analog input range selection. Defaults to (Reserved) range.	3.4.2
D03	R/W	RANGE1		
D04	R/W	OFFSET BINARY	Selects offset binary or two's complement input data format. Defaults HIGH to offset binary.	3.5.2.2
D05	R/W	INITIATOR	Selects INITIATOR or TARGET mode for external clock and sync signals. Defaults to Initiator mode.	3.6.3
D06	R/W	*SOFTWARE SYNC	Initiates a local ADC sync operation when asserted. Also generates an external sync output if INITIATOR mode is selected. Clears automatically.	3.6.3.2
D07	R/W	*AUTOCAL	Initiates an autocalibration operation when asserted. Clears automatically upon completion.	3.7
D08	R/W	INTERRUPT A0	Interrupt event selection. Default is zero.	3.8.1
D09	R/W	INTERRUPT A1		
D10	R/W	INTERRUPT A2		
D11	R/W	INTERRUPT REQUEST FLAG	Set HIGH when the board requests an interrupt. Clears the request when cleared LOW by the bus.	
D12	RO	AUTOCAL PASS	Set HIGH at reset or autocal initialization. Cleared LOW if autocalibration terminates unsuccessfully.	3.7
D13	RO	CHANNELS READY	LOW during any change in channel parameters. Asserted HIGH when ADC clocks are stabilized.	3.4.3
D14	RO	BUFFER THRESHOLD FLAG	Asserted HIGH when buffer contents exceed the assigned threshold.	3.5.3.1
D15	R/W	*INITIALIZE	Initializes the board when asserted HIGH.	3.3.2
D16	R/W	SYNCHRONIZE SCAN	Input channel data is acquired in discrete scans. All active channels must be synchronized and adjusted to a common sample rate.	3.10
D17	R/W	CLEAR BUFFER ON SYNC	Changes the context of the SOFTWARE SYNC control bit changes to CLEAR BUFFER.	3.5.3.2
D18	R/W	(Reserved)	---	---
D19	R/W	FORCE LOW FILTER	When HIGH, selects the low-frequency image filter. When LOW (default), image filter selection is automatic.	3.6.1.4
D20	R/W	TTL EXTERNAL SYNC IO	Enables TTL external sync and clock I/O when HIGH.	3.6.3
D21-31	RO	(Reserved)	---	---

* Cleared automatically. R/W = Read/Write; RO = Read-Only.

** Changes to 0000 783Ch when the input buffer fills.

Table 3.3.1. Configuration Operations

Operation	Maximum Duration
PCI configuration registers are loaded from internal EEPROM	3 ms
Internal control logic is configured from internal ROM	300 ms
Internal control logic is initialized	3 ms
A/D converters and clocks are initialized	**5 seconds**

Table 3.4. Analog Input Function Selection

AIM[..0]	FUNCTION OR MODE
0	Differential analog input mode.
1	(Reserved).
2	ZERO test. Internal ground reference is connected to all analog input channels.
3	+VREF test. Internal voltage reference is connected to all analog input channels.

Table 3.4.2. Analog Input Range Selection

RANGE[1..0]	ANALOG INPUT RANGE
0	±2.5 Volts
1	±2.5 Volts
2	±5 Volts
3	(Reserved)

Table 3.5.2. Input Data Buffer Organization

Offset: 0000 0048h **Default: XXXX XXXXh**

SELECTED DATA WIDTH	RESERVED (Zero)	CHANNEL TAG	ZERO-PAD	CHANNEL DATA VALUE
16 Bits	D[31..19]	D[18..16]	---	D[15..0]
18 Bits	D[31..29]	D[28..24]	D[23..18]	D[17..0]
20 Bits	D[31..29]	D[28..24]	D[23..20]	D[19..0]
24 Bits	D[31..29]	D[28..24]	---	D[23..0]

Table 3.5.2.2. Analog Input Data Coding; 16-Bit Data Field

	DIGITAL VALUE (Hex)	
ANALOG INPUT LEVEL	**OFFSET BINARY**	**TWO'S COMPLEMENT**
Positive Full Scale minus 1 LSB	FFFFh	7FFFh
Zero plus 1 LSB	8001h	0001h
Zero	8000h	0000h
Zero minus 1 LSB	7FFFh	FFFFh
Negative Full Scale plus 1 LSB	0001h	8001h
Negative Full Scale	0000h	8000h

Table 3.5.3. Buffer Threshold Register

Offset: 0000 0038h **Default: 0000 FFFEh**

BIT FIELD	MODE	DESIGNATION	FUNCTION
D[17..00]	R/W	BUFFER THRESHOLD	Buffer Flag Threshold (duplicated in the BCR)
D[18]	R/W	DISABLE BUFFER INPUT	Disables inputs to the data buffer.
D[19]	R/W	CLEAR BUFFER *	Clears (empties) the buffer
D[21..20]	R/W	DATA WIDTH	Controls the width of the buffer data field as: 0 => 16 bits 1 => 18 bits 2 => 20 bits 3 => 24 bits.
D[31..22]	RO	(Reserved)	---

* Clears automatically.

Table 3.6.1.1. Channel Groups

CHANNEL GROUP	INPUT CHANNELS
0	00, 01
1	02, 03

Table 3.6.1.2-1. Rate Assignments Register

Offset: 0000 0014h **Default: 0000 0010h**

BIT FIELD	DESIGNATION	CHANNEL GROUP
D[03..00]	GROUP 0 RATE SOURCE	0
D[07..04]	GROUP 1 RATE SOURCE	1
D[31..08]	(Reserved)	---

Table 3.6.1.2-2. Rate Generator Assignment Codes

ASSIGNMENT CODE	RATE CLOCK SOURCE
0	Rate Generator-A
1	Rate Generator-B
2	(Reserved)
3	(Reserved)
4	External Sample Clock (as Rate-A generator input)
5-7	None (Disabled)
8-15	(Reserved)

Table 3.6.1.3. Rate Divisor Register

Offset: 0018h **Default: 0000 0505h**

	CHANNEL DIVISORS; Ndiv = 3-60
BIT FIELD:	**Rate Divisors 00-01**
D[07..00]	Channels 00,01
D[15..08]	Channels 02,03
D[31..16]	(Reserved)

Table 3.6.1.4-1. Rate Generator Control

Fsamp Range	Ndiv	Nrate Range	Fgen Range	ADC Mode	Fmin
2-50 KSPS	3-60	0-554	7.68-16.00 MHz	Single speed	7.6800 MHz
50-100 KSPS	2	0-511	6.40-12.80 MHz	Dual speed	6.400 MHz
100-200 KSPS	1	0-511	6.40-12.80 MHz	Quad speed	6.400 MHz

Table 3.6.1.4-2. ADC Clocking Control Examples

Rate Control (Nrate)	Channel Group Frequency (Fgen), MHz	Divisor (Ndiv)	Sample Rate (Fsamp), KSPS
0	7.680	**15**	**8.000 ***
511	15.360	**30**	**8.000 ***
511	15.360	**15**	**16.000**
511	15.360	**5**	**48.000**
426	14.083	**10**	**22.00 ****
426	14.083	**5**	**44.00 ****
0	6.400	**2**	**50.00**
511	12.800	**2**	**100.00**
511	12.800	**1**	**200.00**

* Telephony applications.
** Harmonically locked if all channels are assigned to the same rate generator.

Table 3.9.1. Typical DMA Register Configuration; DMA Channel-0

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Analog Input Buffer local address (Analog input buffer)	0000 0048h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction; Local bus to PCI bus (Analog inputs)	0000 000Ah
A8h	DMA Command Status	Command and Status Register	0000 0001h 0000 0003h (See Text)

* Determined by specific transfer requirements.

Table 3.8.1. Interrupt Event Selection

INTERRUPT A[2:0]	INTERRUPT EVENT CONDITION
0	Initialization completed. Default state.
1	Autocal completed
2	Channels Ready
3	Data Buffer threshold flag, LOW-to-HIGH transition
4	Data Buffer threshold flag, HIGH-to-LOW transition
5	(Reserved)
6	(Reserved)
7	(Reserved)

Table 3.10.1. Channel Order (Active channels 00-03)

	CHANNEL ORDER	
SAMPLE EVENT	NON-SYNCHRONIZED SCANS (Typical)	SYNCHRONIZED SCANS
Tn	3012	0123
Tn+1	2301	0123
Tn+2	0123	0123
Tn+3	1230	0123
Tn+4	2301	0123

Table 3.11.1. Firmware Revision Register

Offset: 0000 003Ch **Default: 000X XXXXh**

BIT FIELD	DESCRIPTION
D00-D11	Firmware Revision *
D12-D14	(Reserved firmware field).
D15	High (Both demand-mode and block-mode DMA are available).
D16	High if 4 input channels are present.
D17	(Reserved)
D18-D31	(Reserved)

* The firmware revision extends through D15.

APPENDIX B

MIGRATION FROM PC104P-16SDI

APPENDIX B

MIGRATION FROM PC104P-16SDI

Operation of the PC104P-24DSI12-4-16SDI is similar to that of the PC104P-16SDI with a 24 MHz master clock installed. This appendix summarizes the principal operational similarities and differences between the two products, and is provided as a general guide rather than a definitive list of requirements.

B.1. Comparison of Features

Table B.1 summarizes principal PC104P-24DSI12-4-16SDI and 24 MHz PCI-24DSI32 features.

Table B.1. PC104P-16SDI, PC104P-24DSI12-4-16SDI Features Comparison

Feature	PC104P-16SDI (24 MHz Clock)	PC104P-24DSI12-4-16SDI
Conversion resolution	16 Bits	24, 20, 18 or 16 Bits *
Number of input channels	6, 4 or 2	4
Sample rates	5-220 KSPS	2-200 KSPS
Input Ranges	±1.25, 2.5V, 5V, 10V	±2.5V, 5V
Data Buffer	64K-Sample FIFO	256K-Sample FIFO
DC Gain Accuracy	0.05 %	0.3 % (0.03 dB)
Power Consumption; Typical **	6-Channels: 6.5 Watts 4-Channels: 5.5 Watts	3.5 Watts

* Software-selectable. Defaults to 16 bits.
** With all channels active.

B.2. Migration Issues for a 4-Channel Board Operating at 8 KSPS with 16-Bit Data:

Paragraph 2.4.1 Interboard Connections:

Pin functions and mating connector are modified for a 68-Pin I/O connector.

Paragraph 3.3 Configuration and Initialization:

Initialization time increases to 5 seconds.

Paragraph 3.10 Synchronous Scanning:

The scan-synchronization sequence is reduced to simply setting the SYNCHRONIZE SCAN control bit HIGH in the BCR.

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MAN-PC104P-24DSI12-X-16SDI