General Standards Corporation
High Performance Bus Interface Solutions

Rev: 042711

cPCI6U64-24DSI20C500K

24-BIT, 20-CHANNEL, 500 KSPS
DELTA-SIGMA ANALOG INPUT PMC MODULE

REFERENCE MANUAL

--- PRELIMINARY ---

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SECTION 1.0

INTRODUCTION

1.1 General Description

The CPCI6U64-24DSI20C500K module provides wide-range 24-bit analog input capability in the 6U Compact PCI form factor at sample rates up to 500 KSPS per channel. In addition to providing 20 analog input channels, this product supports multiboard clocking and synchronization. The input range is factory-determined as ±6V fullscale, with optional ranges of ±2.5V, ±5V or ±10V available. The module is functionally and electrically compatible with the IEEE PCI local bus specification Revision 2.3, and to the PICMG Specification Version 2.0, Revision 3.0. Power requirements consist of just +5 VDC from the PCI bus, and operation over the specified temperature range is achieved with nominal air cooling. Specific details pertaining to performance are contained in the CPCI6U64-24DSI20C500K product specification. Figure 1.1 illustrates the general physical configuration of the module.

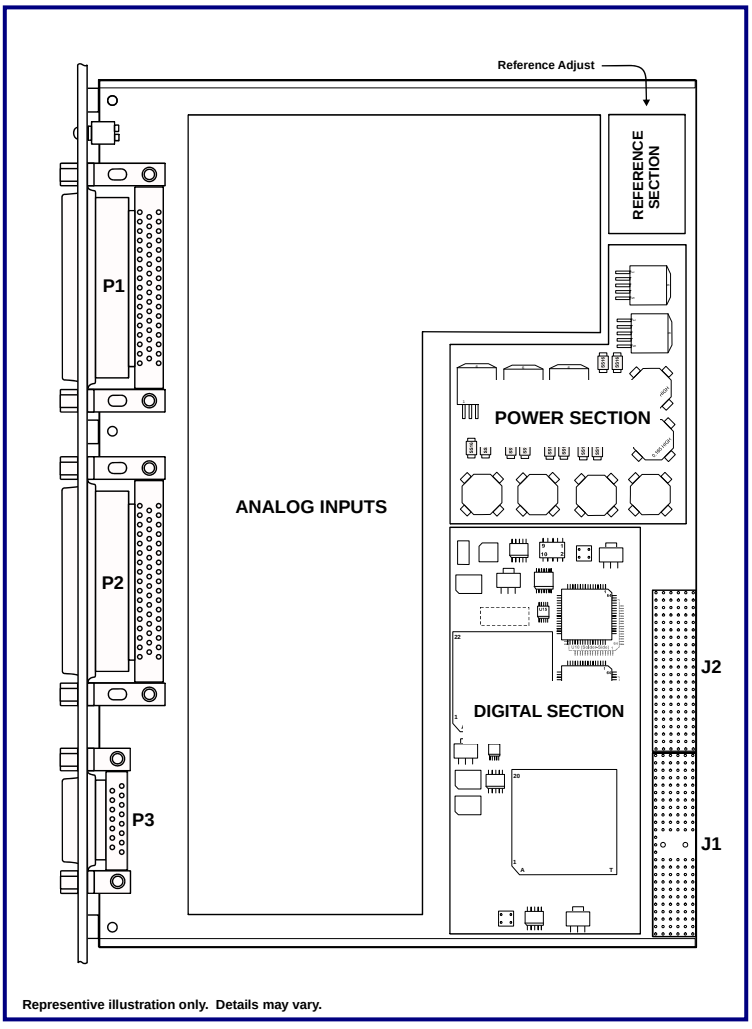

Figure 1.1. Physical Configuration

This product is designed for minimum off-line maintenance. Internal selftest switches permit the calibration and signal integrity of each channel to be verified by the host. An on-demand autocalibration function calibrates all input channels to a single precision internal voltage reference. System input and output connections are made at the front panel through three Subminiature-D connectors.

1.2 Functional Overview

A PCI interface adapter provides the interface between the controlling PCI bus and the internal local controller, through a 32-bit local bus (Figure 1.2). Each input channel contains a dedicated scaling instrumentation amplifier and a 24-Bit delta-sigma A/D converter (ADC) that supports high-resolution data acquisition. Communication with the PCI bus supports universal signalling, with D32/D64 and 33MHz/66MHz operation.

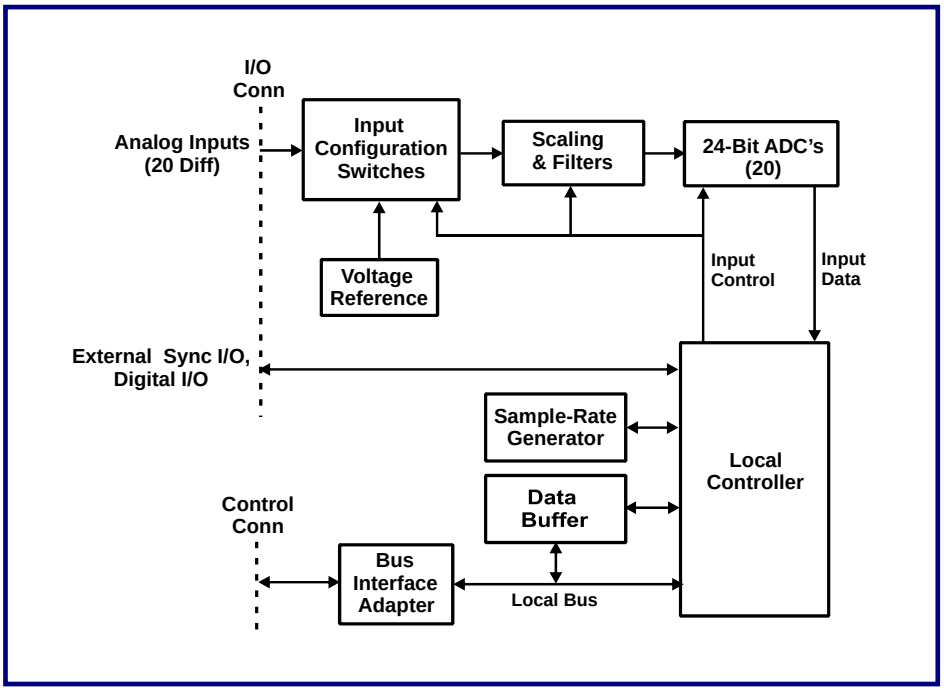

Figure 1.2. Functional Organization

An internal sample-rate clock generator uses a precision reference oscillator to provide sample rates from 10 KSPS to 500 KSPS, or an external clock source can control the sample rate over the same range. The input bandwidth extends down to DC. Conversion data from all active channels is transferred to the PCI bus through a 512K-sample FIFO data buffer.

Multiple boards can be synchronized to perform sampling in "lockstep", either by a software command, or by external hardware sync and clock input signals. Hardware sync and clock input/output signals permit multiple boards to be connected together for phase-locked operation from a common clock.

SECTION 2.0
INSTALLATION AND MAINTENANCE

2.1 Board Configuration

This product has no field-alterable electrical or mechanical features, and is completely configured at the factory.

2.2 Installation

2.2.1 Physical Installation

To minimize the opportunity for accidental damage before installation, the module should be stored in the original protective shipping envelope. System power must be turned OFF before proceeding with the installation.

CAUTION: This product is susceptible to damage from electrostatic discharge (ESD). Before removing the module from the conductive shipping envelope, ensure that the work surface, the installer and the host equipment have been properly discharged to ground.

Before removing the board from the protective shipping envelope, select an empty 6U expansion slot in the host computer and, if a blank panel is located in the slot position, remove the panel. Then remove the board from the shipping envelope and insert the board into the allocated expansion slot, carefully pressing the board firmly to seat the rear-panel connectors. Secure the panel latches to complete the installation.

NOTE: The 20-Channel version of this product requires forced-air cooling at the rate of at least 150 linear feet per minute (LFPM).

2.2.2 Input/Output Cable Connections

System cable signal pin assignments are listed in Tables 2.2.2-1 and 2.2.2-2. Unused input pins may be left disconnected in most applications. However, if very long cables are used or if excessive cable noise is anticipated, the unused analog inputs should be grounded to the input return to minimize the injection of noise into the board.

System input/output cxonnections are made at the front panel through FP-P1, P2 and P3, as shown in Figure 2.2.2. Refer to the product specification for information pertaining to system input/output cable mating connectors. Contact the factory if preassembled cables are required.

Table 2.2.2-1. System I/O Connectors

(50-Pin D-Sub)

	FP-P1		FP-P2
Pin	Signal	Pin	Signal
1	INP CH 00 HI	1	INP CH 10 HI
34	INP CH 00 LO	34	INP CH 10 LO
18	INP RETURN	18	INP RETURN
2	INP RETURN	2	INP RETURN
35	INP CH 01 HI	35	INP CH 11 HI
19	INP CH 01 LO	19	INP CH 11 LO
3	INP RETURN	3	INP RETURN
36	INP RETURN	36	INP RETURN
20	INP CH 02 HI	20	INP CH 12 HI
4	INP CH 02 LO	4	INP CH 12 LO
37	INP RETURN	37	INP RETURN
21	INP RETURN	21	INP RETURN
5	INP CH 03 HI	5	INP CH 13 HI
38	INP CH 03 LO	38	INP CH 13 LO
22	INP RETURN	22	INP RETURN
6	INP RETURN	6	INP RETURN
39	INP CH 04 HI	39	INP CH 14 HI
23	INP CH 04 LO	23	INP CH 14 LO
7	INP RETURN	7	INP RETURN
40	INP RETURN	40	INP RETURN
24	INP CH 05 HI	24	INP CH 15 HI
8	INP CH 05 LO	8	INP CH 15 LO
41	INP RETURN	41	INP RETURN
25	INP RETURN	25	INP RETURN
9	INP CH 06 HI	9	INP CH 16 HI
42	INP CH 06 LO	42	INP CH 16 LO
26	INP RETURN	26	INP RETURN
10	INP RETURN	10	INP RETURN
43	INP CH 07 HI	43	INP CH 17 HI
27	INP CH 07 LO	27	INP CH 17 LO
11	INP RETURN	11	INP RETURN
44	INP RETURN	44	INP RETURN
28	INP CH 08 HI	28	INP CH 18 HI
12	INP CH 08 LO	12	INP CH 18 LO
45	INP RETURN	45	INP RETURN
29	INP RETURN	29	INP RETURN
13	INP CH 09 HI	13	INP CH 19 HI
46	INP CH 09 LO	46	INP CH 19 LO
30	INP RETURN	30	INP RETURN
14	INP RETURN	14	INP RETURN
47	DIGITAL GND	47	DIGITAL GND
31	DIGITAL GND	31	DIGITAL GND
15	DIO 00	15	DIO 04
48	DIGITAL GND	48	DIGITAL GND
32	DIO 01	32	DIO 05
16	DIGITAL GND	16	DIGITAL GND
49	DIO 02	49	DIO 06
33	DIGITAL GND	33	DIGITAL GND
17	DIO 03	17	DIO 07
50	DIGITAL GND	50	DIGITAL GND

[1] In single-ended mode, 'HI' indicates signal, and 'LO' indicates no-connect.

Table 2.2.2-2. Sync I/O Connector

(15-Pin D-Sub)

Pin	Signal
1	EXT SYNC INPUT HI
9	EXT SYNC INPUT LO
2	DIGITAL GND
10	DIGITAL GND
3	EXT CLK INPUT HI
11	EXT CLK INPUT LO
4	DIGITAL GND
12	DIGITAL GND
5	EXT SYNC OUT HI
13	EXT SYNC OUT LO
6	DIGITAL GND
14	DIGITAL GND
7	EXT CLK OUT HI
15	EXT CLK OUT LO
8	DIGITAL GND

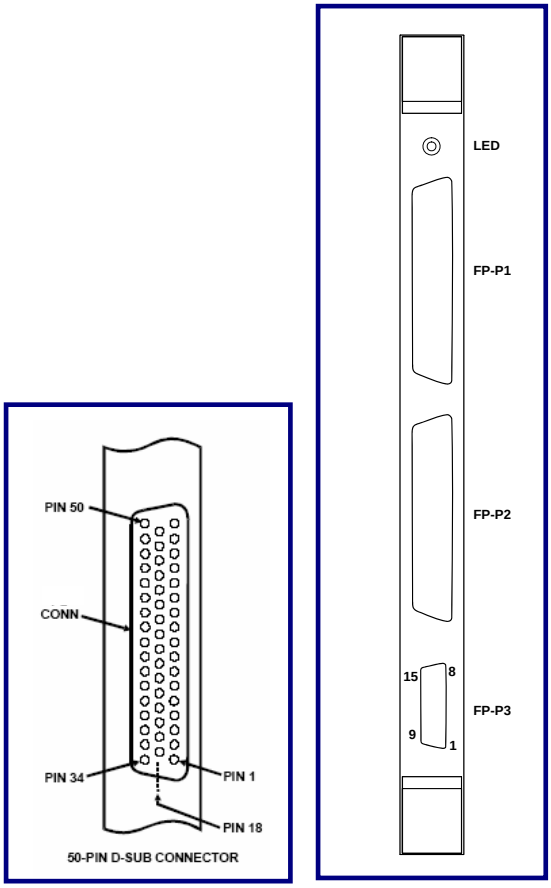

Figure 2.2.2. System I/O Connectors

2.3 Analog Input Configuration

The analog inputs are configured as 20 differential input pairs. Differential operation provides the highest noise immunity, and is recommended for the majority of applications. Pull-down resistors are provided on all analog inputs. Although the input configuration is differential, single-ended signal sources can be accommodated as described in Paragraph 2.3.2.

2.3.1 Differential Inputs

Differential operation is essential when the input source returns are at different potentials. This operating mode also offers the highest rejection of the common mode noise that is characteristic of long unshielded cables. When operating in the differential mode, shown in Figure 2.3.1a, the wire pair from each signal source is connected between the HI(+) and LO(-) inputs of a single input channel. The input return should be connected to system ground (remote common) as closely as possible to the input sources. The average HI/LO signal level relative to the input return is the common mode voltage **Vcm** which, for optimum performance, must not exceed the maximum value indicated in the product specification. (**Vcm** actually is the *mean value* of the HI and LO inputs relative to INPUT RTN, but is shown here for simplicity as the potential between the LO input and INPUT RTN.)

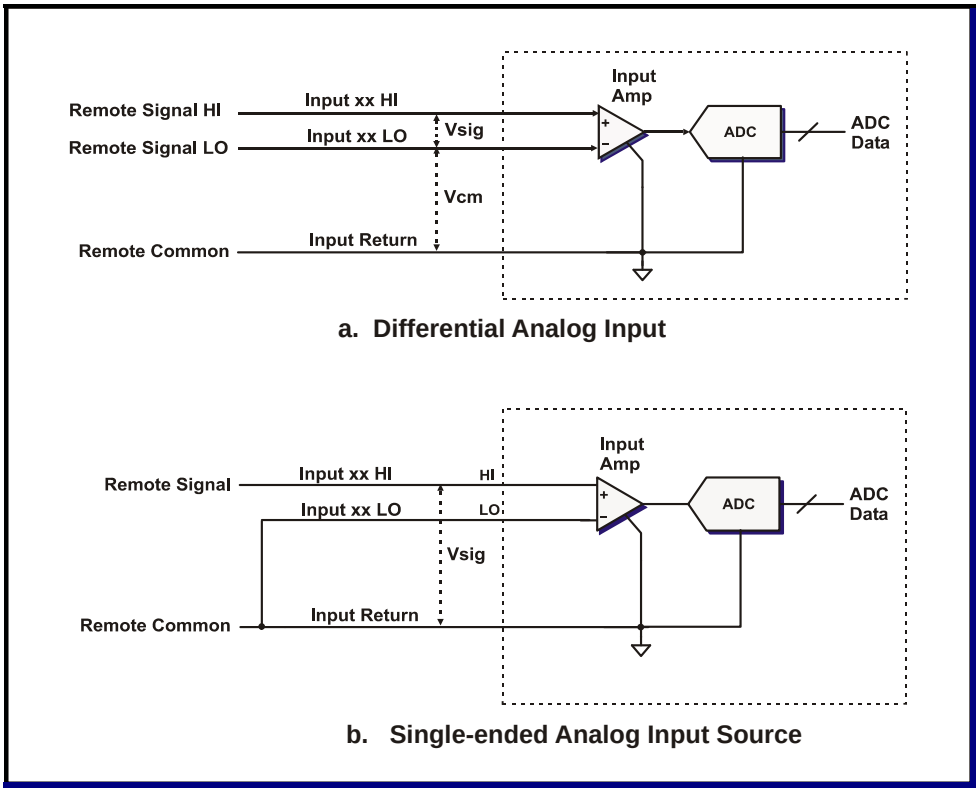

Figure 2.3.1. Input Configurations

2.3.2 Single-Ended Input Sources

Single-ended signal sources can be accommodated as shown in Figure 2.3.1b, with the signal line connected to INP XX HI, and the associated INP XX LO input connected to INPUT RTN at the source. The single-ended operating connection provides suitable performance only when the input signal sources either are isolated from each other, or are common to a single isolated signal return.

CAUTION: If a significant potential difference exists between the remote signal return and INPUT RTN, a low impedance between the two returns can cause excessive current to flow, which in turn can cause erroneous measurements or possible damage to the board. Return-current should be controlled to less than a few milliamps for best performance, and to less than 100 milliamps to avoid damage.

2.4 Multiboard Clocking and Synchronization

Analog input converters on multiple boards can be:

a. Clocked from a single clock source (Multiboard clocking), and/or:

b. Synchronized to a common time reference (Multiboard synchronization).

Clocking multiple converters from a single source prevents the *sampling drift* that occurs when converters are clocked from different sources. *Synchronizing* the converters on multiple boards causes the converters to initiate conversions simultaneously, and can be used to eliminate *sampling skew* between channels.

2.4.1 Interboard Connections

Figure 2.4.1 illustrates how multiple CPCI6U64-24DSI20C500K boards can be daisy-chained together in an initiator-target sequence to provide common clocking between boards. The CLK OUT HI/LO lines from an initiator are connected to the CLK INP HI/LO lines on a target board, and the SYNC output and input pairs are connected similarly. Each target board can serve as an initiator for another target board, and multiple boards can be daisy-chained together for synchronous operation.

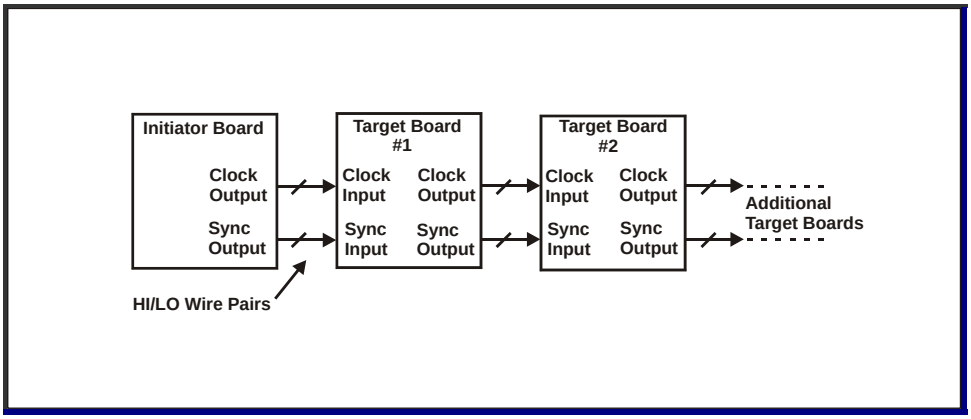

Figure 2.4.1. Multiboard Clock/Sync Connections

The clock output signal is generated internally on an initiator board, or is a duplicate of the clock input signal on a target board. Similarly, the sync output is the software-generated sync signal on an initiator board, or a duplicate of the sync input signal on a target board.

Note: External clock and sync inputs can be provided from external sources other than an initiator board, and can software-configured for either single-ended TTL or differential LVDS logic levels. As a general rule, LVDS levels should be used in applications requiring I/O cable lengths that exceed 20-30 centimeters (10 inches).

In the TTL configuration, clock and sync inputs and outputs are connected through the "HI" I/O pins. LO inputs must be left open or disconnected, and the LO outputs are inactive. TTL signals are referenced to DIGITAL RTN.

Because each board provides active clock and sync outputs for the next board in the chain, the number of boards in the chain is limited only if the propagation delay of approximately 10 nanoseconds introduced by each board becomes significant through multiple boards. For LVDS clock and sync I/O configurations, cable-length between boards should not exceed one meter for general-purpose ribbon cable, while high-quality 100-Ohm cable can extend the length to 10 meters or more. Application software controls the designation of each board as an initiator or a target.

By using an external clock and sync distribution module, multiple boards can be interconnected in a 'star' configuration to eliminate the clock and sync propagation delay introduced by each board in a daisy chain configuration.

NOTE: The EXT SYNC INP signal can also be software-configured to initiate a triggered acquiisition burst.

2.4.2 Multiboard Synchronization

Boards that are interconnected for multiboard synchronization initiate internal *synchronization sequences* each time a sync pulse is generated by the initiator board. The Sync I/O can also be used to reset (clear) the data buffers on target boards.

2.5 Maintenance

This product requires no scheduled hardware maintenance other than periodic reference verification. The optimum adjustment interval will vary, depending upon the specific application, but in most instances an interval of one year is recommended. In the event of a suspected malfunction, all associated system parameters, such as I/O cabling, power voltages, and control bus integrity should be evaluated before a board is returned to the factory for problem analysis and repair.

2.6 Reference Verification and Adjustment

All input and output channels are software-calibrated to an internal voltage reference by an embedded autocalibration software utility. This section describes the adjustment of the internal reference.

2.6.1 Equipment Required

Table 2.6.1 lists the equipment requirements for calibrating the PMC-24DSI16WRC. Alternative equivalent equipment may be used.

Table 2.6.1. Reference Adjustment Equipment

EQUIPMENT DESCRIPTION	MANUFACTURER	MODEL
Digital Multimeter (DMM), 5-1/2 digit, 0.005% accuracy for DC voltage measurements at +10 Volts.	Hewlett Packard	34401A
Host system with PMC site	---	---
DMM test leads suitable for connecting to 2mm header pins.	---	---

2.6.2 Adjustment Procedure

The following procedure describes the single adjustment that is necessary to ensure conformance to the product specification. Adjustment of the internal reference (Vtest) is performed with an internal trimmer and a test connector that are accessible at the top edge of the module as indicated in Figure 1.1. This procedure assumes that the board is installed in a functional 6U Compact PCI system.

1. Connect the digital multimeter between VTEST (+) Pin-3, and REF RTN (-) Pin-4 in the J6 test connector adjacent to the reference adjustment trimmer.
2. If power has been removed from the board, apply power now. Wait at least 10 minutes after power is applied before proceeding..
3. Verify that the digital multimeter indication is 99.000±0.013 percent of the input range (E.g.: +5.9400 VDC ±0.0008 VDC for the ±6V range). If the indication is not within this range, adjust the INTERNAL REFERENCE trimmer accordingly.
4. Verification and adjustment is completed. Remove all test connections.

SECTION 3.0

CONTROL SOFTWARE

3.1 Introduction

The CPCI6U64-24DSI20C500K board is compatible with the PCI Local Bus specification, and is controlled through a PLX™ PCI-9656 PCI adapter that supports both 33MHz and 66MHz bus speeds as well as universal signaling and both D32 and D64 PCI bus widths. Configuration-space registers are initialized internally to support the location of the board on any 32-longword boundary in memory space.

After initialization, communication between the PCI bus and the board takes place through the control and data registers shown in Table 3.1. All local data transfers are long-word D32. The input data buffer supports both block-mode and demand-mode DMA transfers as well as single-reads. To ensure compatibility of applications with subsequent product upgrades, reserved bits should be written as LOW.

Table 3.1. Control and Data Registers

Local Addr [1]	Designation	Access Mode [2]	Default	Primary Function	Ref
00	**Board Control (BCR)**	R/W	0008 3830h	Board Control Register (BCR)	3.2
04	**Rate Control-A**	R/W	0002 8019h	ADC frequency generator control integers Nref, Nvco.	3.6.2
08	**Digital I/O Port**	R/W	0000 0X0Xh	Bidirectional digital I/O port control	3.13
0C	**Clock-Source Assignments**	R/W	0000 0000h	ADC Clock source; Group disables.	3.6.1.2
10	**Rate Divisor**	R/W	0000 0001h	Sample rate divisor.	3.6.1.2
14	(Reserved)	R/W	0000 0000h	---	---
18	(Reserved)	RO	0000 0000h	---	---
1C	**Burst Block Size**	R/W	0000 0001h	Specifies the number of sample sets to be acquired in a triggered burst	3.12.1
20	**Buffer Control**	R/W	0007 FFFEh	Input buffer control and status	3.5.3
24	**Board Configuration**	RO	00XX XXXXh	Installed firmware and hardware options	3.10
28	**Buffer Size**	RO	000X XXXXh	Number of ADC values in the input buffer.	3.5.4
2C	Autocal Values [3]	R/W	---	---	---
30	**Input Data Buffer**	RO (DMA)	XXXX XXXXh	Input Data Buffer; Data and channel tag	3.5
34	(Reserved)	RO	0000 0000h	---	---
38	(Reserved)	RO	0000 0000h	---	---
3C	**Burst Trigger Timer**	R/W	0000 C350h	Internal trigger timer rate divisor	3.12.2
40-7C	(Reserved)	---	---	---	---

[1] Offsets from the PCI base address for local addressing.
[2] R/W = Read/Write; RO = Read-Only.
[3] Maintenance register; Shown for reference only

3.2 Board Control Register

The Board Control Register (BCR) controls primary board functions, including analog input mode and input range selections, and supports up to 32 control bits and status flags (Table 3.2). Control and monitoring functions of the BCR are described in detail throughout the remainder of this section.

Table 3.2. Board Control Register

Offset: 0000h **Default: 0008 3830h**

Data Bit	Designation	Mode	Def	Function	Ref
D00-01	AIM[]	R/W	0h	Analog input mode. Selects system inputs or selftest mode. Defaults to system inputs.	3-4
D02-03	DRATE[]	R/W	0h	Selects oversampling ratio (OSR)	3.6.1.3
D04	OFFSET BINARY	R/W	1	Selects offset binary or two's complement input data format. Defaults HIGH to offset binary.	3.5.2.2
D05	INITIATOR OUTPUT	R/W	1	Selects INITIATOR or TARGET mode for external clock and sync output signals. Defaults HIGH to Initiator mode.	3.6.5
D06	SOFTWARE SYNC [1]	R/W	0	Initiates a local ADC sync operation when asserted. Also generates an external sync output if INITIATOR mode is selected. Clears automatically.	3.6.4, 3.6.5.2
D07	AUTOCAL [1]	R/W	0	Initiates an autocalibration operation when asserted. Clears automatically upon autocal completion.	3.7
D08	INTERRUPT A0	R/W	0h	Interrupt event selection. Default is zero.	3.8
D09	INTERRUPT A1	R/W			
D10	INTERRUPT A2	R/W			
D11	INTERRUPT REQUEST FLAG	R/W	1	Set HIGH when the board requests an interrupt. Clears the request when cleared LOW by the bus.	
D12	AUTOCAL PASS	RO	1	Set HIGH at reset or autocal initialization. Cleared LOW if autocalibration terminates unsuccessfully.	3.7
D13	CHANNELS READY	RO	1	LOW during any change in channel parameters. Asserted HIGH when inputs are ready to acquire data.	3.4.3
D14	BUFFER THRESHOLD FLAG	RO	0	Asserted HIGH when buffer contents exceed the assigned threshold.	3.5.3
D15	INITIALIZE [1]	R/W	0	Initializes the board when asserted. Sets all defaults.	3.3
D16	ENABLE TRIGGER TIMER	R/W	0	Enables the internal burst trigger timer.	3.12.2
D17	CLEAR BUFFER ON SYNC	R/W	0	Changes the context of the SOFTWARE SYNC to CLEAR BUFFER.	3.5.3.2
D18	RATE GEN EXT CLOCK OUT (Initiator Mode only)	R/W	0	When HIGH: Selects the internal rate generator as the external clock output source. When LOW: Selects the Group-00 sample clock. If Group-00 external clocking is selected, the output is driven by the internal rate generator and the Group-00 divisor.	3.6.5.1
D19	FRONT PANEL LED	R/W	1	Illuminates the front-panel LED when HIGH.	3.14
D20	TTL EXTERNAL SYNC I/O	R/W	0	Selects TTL external sync I/O configuration.	3.6.1.2
D21	ENABLE INPUT BURST	R/W	0	Selects triggered-burst acquisition when HIGH.	3.12
D22	S/W BURST TRIGGER	R/W	0	Initiates a triggered burst when asserted. Forced HIGH during any triggered burst.	3.12.1
D23-31	(Reserved)	RO	0h	---	---

[1] Clears automatically.

3.3 Configuration and Initialization

3.3.1 Configuration

Board configuration is initiated by a PCI bus RESET, which should be required only once after the initial application of power. During configuration, initial values for both the PCI configuration registers and the internal control logic are extracted from internal nonvolatile read-only memory. While the PCI configuration registers are being loaded, the response to PCI target accesses is RETRY's. Configuration operations are executed in the sequence shown in Table 3.3.1.

Table 3.3.1. Configuration Operations

Operation	Maximum Duration
PCI configuration registers are loaded from internal EEPROM	3 ms
Internal control logic is configured from internal ROM	300 ms
Internal control logic is initialized	3 ms
A/D converters and clocks are initialized	20 ms

Configuration terminates with the PCI interrupts disabled.

3.3.2 Initialization

Internal control logic can be initialized without invoking configuration by setting the INITIALIZE control bit in the BCR. This action causes the internal logic to be initialized, but does not affect the PCI configuration registers and does not reconfigure the internal control logic. Initialization has a maximum duration of 20 milliseconds, and produces the following conditions:

- The Initiator mode is selected, (3.6.5.1),
- The width of the buffer data field is adjusted to 16 bits (3.5.2),
- The input buffer is disabled and acquisition is suspended (3.5.3.2) *****,
- The internal rate generator is the ADC clock source for all input channels (3.6.1),
- Internal rate generator frequency is 20.480 MHz (3.6.2),
- Rate divisor is preset to 1, and Oversampling Ratio (OSR) is 256. (3.6.1.3),
- The ADC default sample rate is 40.0 KSPS (3.6.2),
- The internal burst-trigger timer is adjusted to 1.00 kHz (3.12.2),
- The analog input buffer is reset to empty; buffer threshold equals 0007 FFFEh (3.5.3),
- All control registers are initialized; all defaults are invoked (3.3),
- The local interrupt request is asserted as an initialization-completed event (3.8).

***** To commence acquisition immediately after initialization, set the ENABLE BUFFER INPUT control bit HIGH in the Buffer Control register (Table 3.5.3)

Upon completion of initialization, the INITIALIZE control bit is cleared automatically.

3.4 Analog Input Configuration

Configuration of the analog input networks is controlled by the BCR control bits designated as AIM[1..0], the effects of which are summarized in Table 3.4. The analog input selection arranges all input channels in differential configuration during normal operation, or invokes one of two selftest modes.

Table 3.4. Analog Input Function Selection

AIM[..0]	Function or Mode
0	Differential analog input mode.
1	(Reserved).
2	ZERO test. Internal ground reference is connected to all analog input channels.
3	+VREF test. Internal voltage reference is connected to all analog input channels.

3.4.1 Selftest Modes

Two selftest modes provide the ability to verify the accuracy of any or all input channels by replacing the system input connections with either a precision internal reference voltage (+VREF) or a zero reference (ZERO). The +VREF test applies a precision test voltage equal to 99.000 percent of range (+5.9400V on the ±6V range) to all input channels, while the ZERO test applies a value of 0.0000 Volts. The accuracy of selftest measurements should correspond to the product accuracy specification.

NOTE: For maximum test accuracy, the internal reference voltage must be allowed to settle completely when the test mode is changed. After selecting either of these test modes, insert a minimum settling delay of 100 milliseconds before acquiring test values:

3.4.2 Input Range

The input voltage range is factory-configured as ±10V, ±6V, ±5V or ±2.5V, as indicated in the Board Configuration register in Table 3.10.

3.4.3 Settling Delays and the Channels-Ready Flag

When a critical parameter such as input mode or sample rate is changed, a settling transition occurs during which input measurements are unpredictable. A settling delay is inserted automatically when any or all of these parameters are changed, and the CHANNELS READY status flag in the BCR goes LOW during the delay. A LOW-to-HIGH transition of this flag is selectable as an interrupt request "channels ready" event (Section 3.8.1). The CHANNELS READY flag goes low during the following operations for the approximate intervals indicated:

20 ms:	Board initialization (3.3),
2 us:	Buffer reset (3.5.3.2).
20 ms:	Modified sample rate parameter ; i.e.: Nrate, Ndiv, Clock source.
1-10 ms:	ADC synchronization (3.6.5.2).

3.5 Input Data Buffer

3.5.1 General Characteristics

Analog input samples accumulate in the analog input data FIFO buffer, which has a capacity of 512K (524,288) data values. Data accumulates in the buffer until extracted by the PCI bus from a single register location, indicated as 'Input Data Buffer' in Table 3.1. Reading an empty buffer returns an indeterminate value. For each input sample set data is arranged in channel order, with Channel-00 appearing first, and the highest-numbered active channel appearing last.

3.5.2 Data Organization

Each value in the data buffer consists of a 4-bit channel tag field, a zero-pad field, and a data field, as shown in Table 3.5.2. The width of the right-justified data field is adjustable from 16 bits to 24 bits by the DATA WIDTH control field in the buffer control register (Table 3.5.3), and the width of the zero-pad field is adjusted accordingly. The zero-pad field becomes a sign-extension field if two's complement data coding is selected.

Table 3.5.2. Input Data Buffer Organization

Offset: 0000 0030h **Default: XXXX XXXXh**

Selected Data Width	Reserved (Zero)	Channel Tag	Zero-Pad	Channel Data Value
16 Bits	D[31..29]	D[28..24]	D[23..16]	D[15..0]
18 Bits	D[31..29]	D[28..24]	D[23..18]	D[17..0]
20 Bits	D[31..29]	D[28..24]	D[23..20]	D[19..0]
24 Bits	D[31..29]	D[28..24]	---	D[23..0]

3.5.2.1 Channel Tags

A 5-Bit channel tag is attached to each data value in the buffer. This tag value equals the associated input channel number. The channel tag can be eliminated by setting the DISABLE CHANNEL TAG control bit in the Buffer Control Register.

3.5.2.2 Input Data Format

Input data values can be represented either in offset binary format by asserting the OFFSET BINARY control bit HIGH (default state) in the BCR, or in two's complement format by clearing the control bit LOW. Both coding conventions are illustrated for 16-Bit data in Table 3.5.2.2.

Table 3.5.2.2. Analog Input Data Coding; 16-Bit Data Field

	DIGITAL VALUE (Hex)	
ANALOG INPUT LEVEL	**OFFSET BINARY**	**TWO'S COMPLEMENT**
Positive Full Scale minus 1 LSB	FFFFh	7FFFh
Zero plus 1 LSB	8001h	0001h
Zero	8000h	0000h
Zero minus 1 LSB	7FFFh	FFFFh
Negative Full Scale plus 1 LSB	0001h	8001h
Negative Full Scale	0000h	8000h

Positive Full Scale is a positive level that equals the selected input voltage range for the board (e.g.: +6.000 Volts for the ±6V range). *Negative Full Scale* is the negative equivalent of positive full-scale. *Full-scale Range* (FSR) is the total input voltage range. For 16-Bit data, one LSB equals the full-scale range divided by 65,536. (e.g.: 183.105 microvolts for the ±6V range).

3.5.3 Buffer Control Register

The buffer control register (Table 3.5.3) contains the threshold value for the buffer threshold flag in the BCR, and also provides control bits for clearing the buffer and for disabling the buffer input.

Table 3.5.3. Buffer Control Register

Offset: 0000 0020h **Default: 0007 FFFEh**

Bit Field	Mode	Designation	Def	Function
D00-D19	R/W	BUFFER THRESHOLD	0007 FFFEh	Buffer Flag Threshold
D20	R/W	ENABLE BUFFER INPUT	0	Enables ADC inputs to the buffer.
D21	R/W	CLEAR BUFFER [1]	0	Clears (empties) the buffer. Asserted HIGH while the buffer is cleared, either locally or externally.
D22-D23	R/W	DATA WIDTH	0	Controls the width of the buffer data field: 0 => 16 bits 1 => 18 bits 2 => 20 bits 3 => 24 bits.
D24	R/W	DISABLE CHANNEL TAG	0	Replaces the channel tag with a zero-field.
D25	R/W	BUFFER OVERFLOW [2]	0	Reports buffer overflow (Write on full)
D26	R/W	BUFFER UNDERFLOW [2]	0	Reports buffer underflow (Read on empty)
D27-D31	RO	(Reserved)	0h	---

[1] Clears automatically. [2] Cleared by writing LOW, or by Initialization.

NOTE: Since delta-sigma converters operate essentially continuously, the initiation and termination of acquisition sequences is controlled by the buffer's 'Clear' and 'Enable' controls. To commence acquisition immediately after initialization, set the ENABLE BUFFER INPUT control bit HIGH.

3.5.3.1 Status Flag and Threshold

The amount of data contained in the input buffer can be used to control the BCR status bit BUFFER THRESHOLD FLAG, which can be selected as an interrupt request event. The interrupt request event can be selected to occur on either the rising or falling edge of the flag (Table 3.8.1).

The threshold flag is asserted HIGH when the number of samples in the buffer ***exceeds*** the BUFFER THRESHOLD value in the buffer control register. A buffer-empty event is produced when the threshold value is adjusted to equal 0000 0000h and the threshold flag undergoes a HIGH-to-LOW transition.

3.5.3.2 Buffer Clearing and Enabling/Disabling

Asserting the CLEAR BUFFER control bit in the buffer control register resets (empties) the buffer. This bit clears automatically, but while the buffer is being cleared, this bit is held HIGH and the CHANNELS READY flag (3.4.3) is LOW.

Termination of a Buffer *clearing* operation is synchronized to the data stream. The buffer is held in reset for approximately two microseconds in order to flush the internal data pipeline, after which the reset is sustained until a new ADC sample set is available.

Asserting the ENABLE BUFFER INPUT control bit enables inputs to the buffer from the ADC input channels, and initiates the accumulation of input data. Clearing this control bit disables the buffer and suspends sample acquisition. Input data already present in the buffer when this bit is deasserted remains in the buffer.

Buffer enabling and disabling operations both are synchronous with the input data stream. Regardless of when ENABLE BUFFER INPUT is set or cleared, actual enabling of the buffer always occurs immediately prior to a complete sample set arriving entering the internal data stream. Disabling always occurs immediately after the last active channel in a sample set is loaded into the buffer.

NOTE: Global Buffer Clear:

The buffer also can be cleared by writing a "one" to the SOFTWARE SYNC control bit in the BCR when the CLEAR BUFFER ON SYNC control bit is HIGH. For multiple synchronized boards:

1. On all boards: Set the CLEAR BUFFER ON SYNC bit,
2. On the Initiator: Set SOFTWARE SYNC;
   Wait for Channels Ready LOW-to-HIGH on the initiator.
   (All ADC's and buffers are now scan-synchronized).
3. On all boards: Clear the CLEAR BUFFER ON SYNC bit.

3.5.4 Buffer Size Register

This read-only register listed in Table 3.1 contains the number of analog input values currently stored in the input data buffer, from zero to 534,288 (80000h).

3.5.5 Buffer Underflow and Overflow Flags

BUFFER OVERFLOW and BUFFER UNDERFLOW status bits in the buffer control register report overflow (write on full) or underflow (read on empty) events. Once set, these status bits remain HIGH until cleared either by writing LOW directly, or by Initialization.

3.6 Input Sampling Control

The local controller establishes the following input sampling parameters:

a. Sample rate,
b. Phase, or skew,
c. Channel synchronization.

The effective input bandwidth is determined by the sample rate, while phase and synchronization control the relative timing of sampling between multiple channels. Phase and synchronization are considerations in applications that require consistent relative timing of sampling among multiple channels or multiple boards.

Clocking multiple converters from a single sample rate clock prevents the *sampling drift* that occurs when converters are clocked from different sources. *Synchronization* causes the converters in all channels to initiate conversions simultaneously, and can be used to eliminate *sampling skew* between channels.

NOTE: It is critically important that the inputs always be synchronized (3.6.4) after changing any parameter that affects the sample rate. Failure to do so can cause the general corruption of input data. Any change to the Rate-A control, Clock Source Assignments, Rate Divisor or the Oversampling Ratio will initiate an automatic synchronization sequence. However any sample-rate change, especially from an external source, should still be followed by synchronization with the SOFTWARE SYNC control bit in the BCR.

3.6.1 Sample Rate Control

3.6.1.1 Sample Clock Organization

Sample rates are derived either from an adjustable internal rate generator, or from a single external hardware clock, as shown in Figure 3.6.1.1. The input channels are divided into two equal groups (Table 3.6.1.1), and all active input channels operate from the same clocking source. Group-1 can be independently designated as either active (enabled) or inactive (disabled). The sample rate for both channel groups is controlled by the following operations:

a. Assignment of both groups to the internal rate generator or to an external clock,
b. Rate generator frequency selection, if the internal rate source is selected,
c. Rate divisor selection, unless the Direct External Sample Clock is selected.

3.6.1.2 Clock Source Assignment

A 4-bit code CLOCK SOURCE in the Clock Source Assignments register (Table 3.6.1.2-1) selects either the internal rate generator or the external sample rate clock as sample rate source. Group selection codes are arranged in the register as shown in the table, and use the assignment codes listed in Table 3.6.1.2-2. ***The Group-0 assignment selects the sample rate source for both groups***, while the Group-1 assignment simply enables or disables the group. A disabled group does not provide data to the input data buffer.

NOTE: External I/O signals EXT CLK INP/OUT and EXT SYNC INP/OUT are configured as LVDS HI/LO pairs if the TTL EXTERNAL SYNC I/O control bit is LOW in the BCR, or for TTL signals on the HI lines if the bit is HIGH.

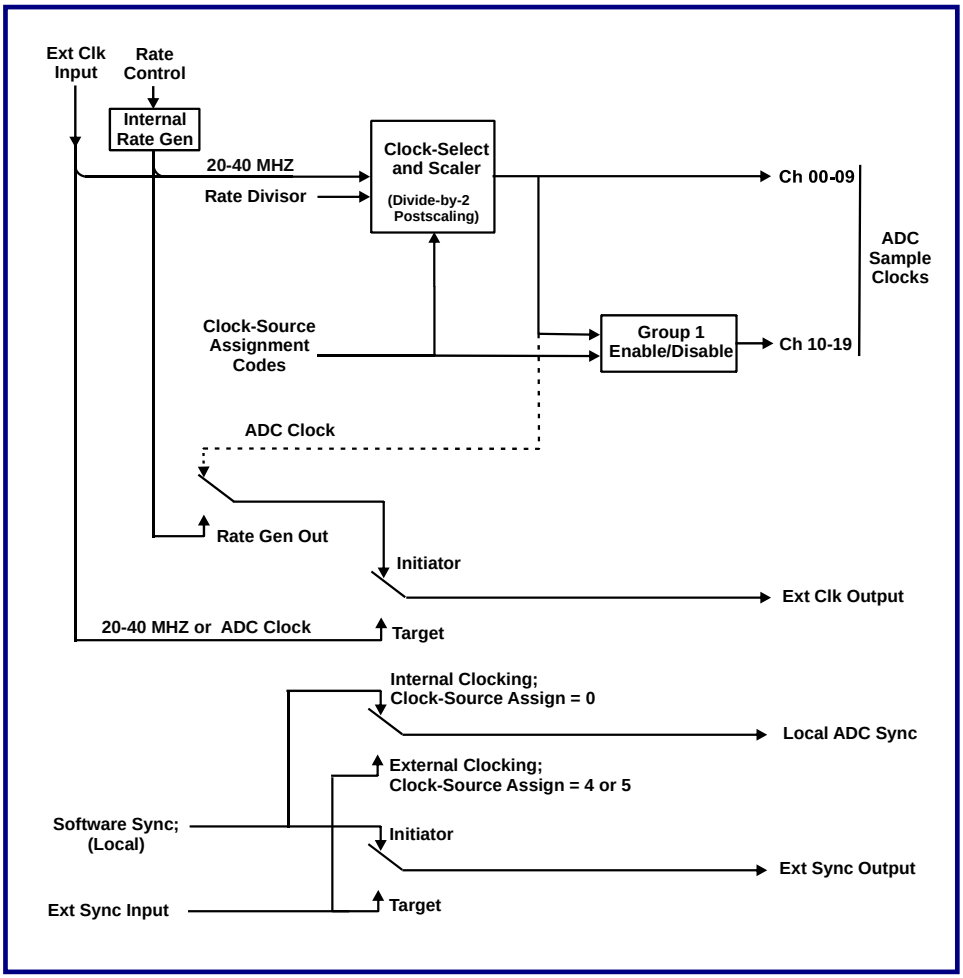

Figure 3.6.1.1. ADC Clock and Sync Organization, 20 Channels

Table 3.6.1.1. Channel Groups

CHANNEL GROUP	20-CHAN BOARD	12-CHAN BOARD	8-CHAN BOARD	4-CHAN BOARD
0	Channels 00-09	00-05	00-03	00, 01
1	Channels 10-19	06-11	04-07	02, 03

Table 3.6.1.2-1. Clock-Source Assignments Register

Offset: 0000 000Ch **Default: 0000 0000h**

BIT FIELD	DESIGNATION	CHANNEL GROUP
D[03..00]	GROUP 0 CLOCK SOURCE	0
D[07..04]	GROUP 1 CLOCK SOURCE	1
D[31..08]	(Reserved)	---

Table 3.6.1.2-2. Clock-Source Assignment Codes

ASSIGNMENT CODE	GROUP 0 ASSIGNMENT	GROUP 1 ASSIGNMENT
0	Internal Rate Generator *	No effect. (Same as Group-0)
1-3	(Reserved)	
4	External Sample Clock (as rate generator input)	
5	Direct External Sample Clock (routed directly to ADC)	
6	**Disabled**	**Disabled**
7-15	(Reserved)	(Reserved)

* Applies to both channel groups. Disabling Group-0 disables both groups.

3.6.1.3 Sample Clock Generation

The ADC's operate in one of four oversampling sampling modes, x256, x128, x64 or x32, as selected by the DRATE[] field in the BCR. Table 3.6.1.3-1 shows the ralationship between DRATE[], the oversampling ratio (OSR), and the effective range of sample rates.

Table 3.6.1.3-1. Oversampling Modes

DRATE[]	Oversampling Ratio	Sample Rate Range
0	x256	9.766 KSPS -78.125 KSPS
1	x128	78.125 KSPS - 156.250 KSPS
2	x64	156.250 KSPS - 312,500 KSPS
3	x32	312,500 KSPS - 500,000 KSPS

NOTE: The signal-to-noise ratio (SNR) is approximately 7dB higher with OSR = 256 than with OSR = 32.

The ADC sample rate **Fsamp** is determined by a rate generator frequency **Fgen** and rate divisor **Ndiv** as:

$$\textbf{Fsamp} = \textbf{Fgen} / (2 * \textbf{OSR} * \textbf{Ndiv}) \qquad \textbf{(3-1)}$$

where **Fsamp** and **Fgen** are in kilohertz, and **Ndiv** is an integer. **Fgen** has a nominal range of 20-40 MHz, and **Ndiv** (Table 3.6.1.3-1) can have any integer value from 1 through 3. To ensure a 50 percent duty cycle for the ADC clock, Fgen is post-scaled by a factor of two. For optimum SNR, the highest possible value of OSR should be used.

Table 3.6.1.3-2. Rate Divisor Register

Offset: 0000 0010h **Default: 0000 0001h**

Bit Field	Designation	Function
D[08..00]	RATE DIVISOR (**Ndiv)**	Scales the rate generator input frequency.
D[31..9]	(Reserved)	---

3.6.2 Rate Generator Control

The internal rate generator is a crystal-based adjustable oscillator that is phase-locked to a stable reference frequency. The frequency of the generator is controlled by the Rate Control-A register listed in Table 3.1, and shown in Table 3.6.2-1.

Fgen can be obtained either externally through the system I/O connector (3.6.5) or from the internal phase-locked loop oscillator, and has a nominal frequency range of 27-54 MHz. The frequency **Fgen** of the internal oscillator is related to a reference frequency **Fref** by integers **Nref** and **Nvco** as:

$$\textbf{Fgen} = \textbf{Fref} * \frac{\textbf{Nvco}}{\textbf{Nref}} \quad , \qquad \textbf{(3-2)}$$

where **Nvco** and **Nref** each has a valid range from 25 to 300, and **Fref** is the frequency of the reference oscillator, which has a standard frequency of **32.768MHz**. Table 3.6.2-2 summarizes the rate generator control parameters.

Table 3.6.2-1. Rate Generator Control Register (Rate Control-A)

Offset: 0004h **Default: 0002 8019h**

Bit Field	Designation	Function
D[11..00]	VCO FACTOR **(Nvco)**	PLL VCO factor; 25-300.
D[23..12]	REF FACTOR **(Nref)**	PLL Reference factor; 25-300.
D[31..24]	(Reserved)	---

* For maximum phase stability, select the lowest possible values for Nvco and Nref.

Notice that the nominal range of Fgen (20-40 MHz) and an Fref value of 32.768MHz imply a valid range of 0.61-1.22 for the ratio Nvco/Nref.

Combining Equations 3-1 and 3-2:

$$\mathbf{Fsamp = Fref * (Nvco/Nref) / (2 * OSR * Ndiv)} \qquad \textbf{(3-3)}$$

Table 3.6.2-2 summarizes the control parameters that determine the ADC sample rate, and the valid range for each parameter. Table 3.6.2-3 lists a number of control parameter examples.

Table 3.6.2-2. Sample-Rate Control Parameters

Parameter	Notation	Valid Range
Sample Rate	**Fsamp**	9.76 - 500 KSPS
Oversampling Ratio *	**OSR**	256, 128, 64 or 32
Reference Frequency	**Fref**	32.768 MHz, Fixed
Rate Divisor	**Ndiv**	1-4
Osc VCO integer	**Nvco**	25-300
Osc Reference integer	**Nref**	25-300
Osc Integer Ratio	**Nvco/Nref**	0.61 - 1.22

* Selected by Drate[] in the BCR.

Table 3.6.2-3. Sample Rate Examples

Sample Rate (KSPS)	Nvco	Nref	Fgen (Mhz)	OSR	DRATE[]	Ndiv
10.000	25	40	20.48000	256	0	4
20.000	30	32	30.72000	256	0	3
40.000	25	40	20.48000	256	0	1
80.000	25	40	20.48000	128	1	1
100.000	25	32	25.60000	128	1	1
300.000	75	64	38.40000	64	2	1
327.680	32	50	20.97152	32	3	1
500.000	125	128	32.00000	32	3	1

Fref = 32.768MHz. All values shown in decimal format.

3.6.3 Direct External Clocking

If the rate assignment selection (Table 3.6.1.2-2) is "Direct External Sample Clock," the signal at the external clock input is routed directly to the ADC's without modification. This configuration eliminates the effect of the **Ndiv**, **Nvco** and **Nref** control variables, and gives the external clock source direct control of the ADC's.

Although the variables **Ndiv**, **Nvco** and **Nref** have no effect in this configuration, the appropriate oversampling ratio (OSR) must be selected with the DRATE[] field in the BCR in order for the ADC's to respond correctly. In general, all boards operating in a multiboard synchronization configuration will use the same value for DRATE[].

3.6.4 Channel Synchronization

Due to the oversampling nature of delta-sigma conversion, each conversion represents a sampling interval consisting of multiple clock cycles, and simply operating all converters from a common clock does not ensure simultaneous, or skew-free, sampling. To ensure simultaneous sampling, the converters must be synchronized to perform conversions simultaneously relative to a common point in time. Thereafter, the converters will continue to sample simultaneously while operating from a common clock.

Synchronization is invoked by setting the self-clearing SOFTWARE SYNC control bit HIGH in the BCR. Completion of the synchronization sequence is indicated by the CHANNELS READY flag in the BCR undergoing a Low-to-High transition (Paragraph 3.4.3). The CHANNELS READY transition can be selected as a condition for an interrupt request event.

NOTE: It is critically important that the inputs always be synchronized after changing any parameter that affects the sample rate. Failure to do so can cause the general corruption of input data. Any change to the Rate-A control, Clock Source Assignments, Rate Divisor or the Oversampling Ratio will initiate an automatic synchronization sequence. However any sample-rate change, especially from an external source, should still be followed by synchronization with the SOFTWARE SYNC control bit in the BCR.

3.6.5 Multiboard Operation

Multiple CPCI6U64-24DSI20C500K boards can be connected together to share a common sampling clock and synchronization command. One of the boards is designated as the *initiator*, and the remaining boards are designated as *targets*. A board is designated as an initiator by setting the INITIATOR control bit HIGH in the BCR, or as a target when the control bit is LOW.

The INITIATOR control bit in the BCR controls only the source of the external clock and sync outputs, and has no other effect.

External clock and sync inputs can be provided from LVDS or TTL sources other than an initiator board.

3.6.5.1 External Sample Clock

Target boards receive an external clock from the external clock input connection, and duplicate the input clock at the external clock output connection (Figure 3.6.1.1). The external clock input is designated as the clocking source by writing either the "External Sample Clock" or "Direct External Sample Clock" assignment code to the target boards' Clock-Source Assignments register (Table 3.6.1.2-2). For calculation of target board sample rates, the external sample clock corresponds to the rate generator frequency **Fgen** described in Section 3.6.1 if "External Sample Clock" is selected, or provides the ADC sample clock directly if "Direct External Sample Clock" is selected.

An ***initiator*** provides an external clock output from either of two sources. If the RATE GEN EXT CLOCK OUT control bit in the BCR is LOW (default), the external clock output frequency equals twice the Group 00 ADC sample clock frequency, and is the internal rate generator output divided by the rate divisor. If the control bit is HIGH, the internal rate generator's unmodified output provides the external clock.

Multiple boards can all be configured as targets and operated in a "star" configuration to operate from a single rate generator. To avoid overloading the LVDS source driver, an LVDS distribution module usually is required in this configuration.

3.6.5.2 External Sync

Boards that are hardware-configured for multiboard synchronization initiate a *synchronization sequence* each time a sync pulse is generated by the initiator board. During synchronization, all ADC's are reset and initialized in a sequence that requires up tp 10 milliseconds for completion. The data buffers also are reset during the sequence, at the end of which, all channels on all boards are synchronized to within one sample clock interval, and all data buffers commence acquiring data simultaneously.

The "CHANNELS READY flag is deasserted on all boards during the synchronization sequence, and returns HIGH when all boards are synchronized and commence acquiring data.

NOTE: A "sample clock interval" is the period of the ADC sample clock (1/Fgen) while the "sample interval" is the interval between data samples (1/Fsamp) and is 32-256 times the sample clock interval (3.6.1).

The SOFTWARE SYNC control bit in the BCR can be used also to clear the buffers on the initiator and target boards simultaneously without executing a full synchronization sequence, by first setting the CLEAR BUFFER ON SYNC control bit HIGH in the BCR. This process requires 4-5 sample intervals for completion. ***If implemented, the CLEAR BUFFER ON SYNC control bit must be asserted on the initiator and all targets before generating the software sync command.***

Notice that In the absence of an ADC clock, the synchronization or buffer-clear interval will be indefinitely long.

Refer to Paragraph 3.12 if burst-triggering is to be implemented.

3.7 Autocalibration

Autocalibration is an embedded utility that calibrates all input channels to a single internal voltage reference. Offset and gain error corrections for each channel are determined and stored during in calibration DAC's during autocalibration. The correction values are retained until either: (a) power is removed, (b) a PCI reset occurs, or (c) autocalibration is invoked again. Autocalibration is invoked by setting the AUTOCAL control bit HIGH in the BCR. Completion of autocalibration is indicated by the AUTOCAL flag clearing automatically to the LOW state. The end of autocalibration is selectable as an interrupt request event (3.8.1).

NOTE: Autocalibration calibrates all channels on all ranges in a single sequence. All installed channels must be active during autocal.

An autocalibration sequence will have a nominal duration of between 2.5 seconds and 16 seconds, depending upon the selected sample rate and the number of active channels.

Tautocal (sec) = 2.5 + (130/Fsamp),

where Fsamp is in kilosamples per second. For example, the nominal autocal duration with the default sample rate of 40KSPS would be 2.5 +(130/40) = 5.8 sec. If fewer than 20 channels are installed on the board, the autocal duration is reduced proportionately.

Read or write access from the PCI bus during autocalibration could disrupt the calibration process, and should be avoided. Either a suitable delay or the "Autocal Completed" interrupt should be used to detect the end of autocalibration.

If a board is defective, the autocalibration process may be unable to successfully calibrate all input channels. If this situation occurs, the AUTOCAL PASS status flag in the BCR will be LOW when the autocal sequence is completed. A HIGH state for AUTOCAL PASS indicates that autocalibration was successful for all channels.

To ensure full conformance to the product specification, autocalibration should always be invoked after:

(a). Power has been applied to the board,

(b). A PCI reset event has occurred,

(c). The clock source or sampling rate has been altered.

Autocalibration can be invoked at any time, but should not occur while the system is experiencing a major environmental transition such as that which usually occurs directly after power is applied. For optimum performance, a warmup delay of 15 minutes is recommended.

3.8 Interrupt Control

In order for the board to generate a PCI interrupt on INTA#, *both* of the following conditions must occur:

a. The internal controller must generate a Local Interrupt Request
b. The *PCI interrupt* must be enabled.

If the internal controller generates a local interrupt request, a PCI bus interrupt will not occur unless the PCI interrupt has been enabled as described below in Paragraph 3.8.2.

3.8.1 Local Interrupt Request

The single local interrupt request line is controlled by the INTERRUPT A[2:0] and INTERRUPT REQUEST FLAG control bits in the BCR. The condition for the interrupt request is selected as shown in Table 3.8.1. When the selected condition occurs, a local interrupt request is generated and the INTERRUPT REQUEST FLAG bit is set in the BCR. The request remains asserted until the PCI bus clears the BCR request flag. A local interrupt request is generated automatically at the end of initialization.

Detection of an interrupt condition or event is *edge-sensitive*. An interrupt request is generated if, and only if, a specific interrupt condition undergoes a *transition* from 'false' (not-true) to 'true' while that condition is selected.

Table 3.8.1. Interrupt Event Selection

Interrupt A[2:0]	Interrupt Event Condition
0	Initialization completed. Default state.
1	Autocal completed
2	Channels Ready; LOW-to-HIGH transition
3	Data Buffer threshold flag, LOW-to-HIGH transition
4	Data Buffer threshold flag, HIGH-to-LOW transition
5	Triggered Burst Completed
6	(Reserved)
7	(Reserved)

3.8.2 Enabling the PCI Interrupt

A local interrupt request will not produce an interrupt on the PCI bus unless the PCI interrupt is enabled. The PCI interrupt is enabled by setting the *PCI Interrupt Enable* and *PCI Local Interrupt Enable* control bits HIGH in the runtime *Interrupt Control/Status Register* described in the PLX™ PCI-9656 reference manual.

3.9 DMA Operation

DMA transfers from the analog input buffer are supported with the board operating as a bus master. Set Bit 02 in the PCI Command register HIGH to select the bus mastering mode. Refer to the PCI-9056 reference manual for a description of DMA configuration registers.

3.9.1 Block Mode

Table 3.9.1 illustrates a *typical* PCI register configuration that would control a non-chaining, non-incrementing ***block-mode*** DMA transfer in DMA Channel 00, in which a PCI interrupt is generated when the transfer has been completed. For most applications, the DMA Command Status Register would be initialized to 0000 0001h, and then changed to 0000 0003h to initiate a transfer.

Table 3.9.1. Typical DMA Register Configuration; Block Mode

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial (constant) local address of buffer	0000 0030h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

* Determined by specific transfer requirements.

3.9.2 Demand Mode

Demand mode transfers are controlled in a manner similar to block mode transfers, with the addition of ***demand-mode*** operation selected in the DMA mode register (D[12] = HIGH). Demand mode operation also requires the ***slow terminate*** mode (D[15] = LOW), which is the default state for this control bit. Table 3.9.2 shows a *typical* PCI register configuration for DMA Channel 00 demand mode operation.

Table 3.9.2. Typical DMA Register Configuration; Demand Mode

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32)	0002 1943h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial (constant) local address of buffer	0000 0030h
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

* Determined by specific transfer requirements.

NOTE: The PCI-9656 adapter extracts data from the 32-Bit (Lword) local bus in 64-Bit (quad-word) increments. Consequently, *if the buffer runs empty or nearly empty*, the situation can arise in which the last one or two samples in an active channel group are retained until subsequent data is acquired. If this occurs, the next sample set flushes the retained data through the PCI-9656 adapter to the PCI bus, and no samples are lost.

3.10 Board Configuration Register

The read-only board configuration register (Table 3.10) contains the existing firmware revision, and a status field that indicates the availability of optional features.

Table 3.10. Board Configuration Register

Offset: 0000 0024h **Default: 00XX XXXXh**

BIT FIELD	DESCRIPTION
D00-D11	Firmware Revision
D12-D15	(Reserved status flags).
D16-D18	Number of input channels: 0 => 20 Channels 1 => 12 Channels 2 => 8 Channels 3 => 4 Channels 4-7 => (Reserved)
D19-D20	Image Filter Frequency: 0 => 2.0MHz, first order. 1 => No filter. 2-3 => (Reserved)
D21-22	Input Range: 0 => ±6V 1 => ±10V 2 => ±5V 3 => ±2.5V
D23-D31	(Reserved)

3.11 Settling Time Considerations

An abrupt change in the analog configuration generally is followed by a 'settling' interval during which the analog networks are transitioning to a new state, and during which specified performance might be suspended. Abrupt changes include:

- A change in sample rate,
- A major input step-change,
- Transitioning into or out of a selftest mode, or out of autocalibration,
- A system or local reset,
- Power application.

The settling time required to reestablish specified performance depends upon the type of disruption, and can vary from tens of milliseconds for a change in voltage-range, to as long as 10-15 minutes after the initial application of power. For *most* configuration changes other than the application of power, specified performance should resume after a settling interval of 20-100 milliseconds. Low-frequency filters will extend the settling interval by an amount that depends upon the filter characteristics. In general, the longest settling delay consistent with application requirements should be implemented.

3.12 Triggered Burst Sampling

3.12.1 Burst Control

If burst sampling is enabled by setting the ENABLE INPUT BURST control bit HIGH in the BCR, a Burst Trigger initiates the acquisition of a specific number of samples for each active channel. During a burst, sampling proceeds at the selected input sample rate until the specified number of samples has been acquired. Sampling then terminates until a subsequent trigger occurs. The number of samples acquired during a triggered burst is specified by the 24-Bit Input Burst Block Size control register (Table 3.1-1). The number of samples acquired in a burst *for each active channe*l equals the value contained in this register. The total number of samples acquired equals this value *times* the number of active channels. If a BURST BLOCK SIZE of zero is selected, a trigger initiates a nonterminating burst that continues as long as bursting is enabled, the buffer is enabled, and a sample clock is present.

A trigger can be generated by (a) asserting the S/W BURST TRIGGER control bit in the BCR, or (b) by implementing the internal burst trigger timer (3.13.2), or (c) by injecting a positive pulse of 150 nanoseconds or greater width as the EXT SYNC INP input signal at the system I/O connector. Regardless of the source of the trigger, the S/W BURST TRIGGER bit in the BCR will always be HIGH during a triggered burst, and the trigger will appear also as a 200 nanosecond positive pulse at the EXT-SYNC OUT output in the I/O connecter for synchronously triggering other boards. *Input triggers are ignored when S/W BURST TRIGGER is HIGH, of if the buffer is disabled (3.5.3.2).*

A software trigger can be applied at any time by setting the INPUT S/W TRIGGER control bit HIGH in the BCR. This bit overrides the existing CLOCK TRIGGER selection, and clears automatically.

Note: While the ENABLE INPUT BURST control bit is HIGH in the BCR, an external SYNC input will be regarded as a burst trigger, and synchronization as described in Paragraph 3.6.5.2 will not occur. To burst-trigger multiple boards, synchronize the boards before asserting ENABLE INPUT BURST.

3.12.2 Internal Burst Timer

When the ENABLE-TRIGGER TIMER control bit is HIGH in the BCR, the internal trigger timer generates a continuous series of burst triggers. The trigger rate is determined as:

TRIGGER RATE (Hz) = Fclk / TRIGGER RATE DIVISOR,

where Fref is the master clock frequency in Hertz, and TRIGGER RATE DIVISOR is defined in the Trigger Rate Divisor register shown in Table 3.12.2. Fclk has a standard value of 50.000MHz.

Table 3.12.2. Trigger Rate Divisor Register

Offset: 0000 003Ch **Default: 0000 C350h**

BIT FIELD:	DESIGNATION	FUNCTION
D[23..00]	TRIGGER RATE DIVISOR	Rate divisor for internally timed triggered bursts.
D[31..24]	(Reserved)	---

3.13 Digital I/O Port

The digital I/O port consists of eight bidirectional TTL I/O lines, with the corresponding data bits shown in Table 3.13. The DIO lines are arranged as two 4-bit nibbles, with the direction of each nibble controlled independently of the other. A nibble is an input to the board if the associated DIO 00 03 OUTPUT control bit is LOW, or is an output if the bit is HIGH. Logic polarities are retained, with a HIGH level at a connector pin associated with a HIGH level for the corresponding bit in the register. All digital I/O lines default to inputs.

Table 3.13. Digital I/O Port Register

Offset: 0008h **Default: 0000 0X0Xh**

DATA BIT	MODE*	DESIGNATION	DEFAULT	DESCRIPTION
D00	RW	DIO 00 DATA	X	Digital I/O Data; Bits 00-03
D01	RW	DIO 01 DATA	X	
D02	RW	DIO 02 DATA	X	
D03	RW	DIO 03 DATA	X	
D04-D06	RW	(Reserved)	0h	---
D07	R/W	DIO 00_03 OUTPUT	0	DATA 00-03 direction control; High for output.
D08	RW	DIO 04 DATA	X	Digital I/O Data; Bits 04-07
D09	RW	DIO 05 DATA	X	
D10	RW	DIO 06 DATA	X	
D11	RW	DIO 07 DATA	X	
D12-D14	RW	(Reserved)	0h	---
D15	RW	DIO 04_07 OUTPUT	0	DATA 04-07 direction control; High for output.
D16-D31	RO	(Reserved)	0h	Read back as all-zero.

3.14 Front Panel LED Indicator

A red LED indicator on the front panel is ON if the FRONT PANEL LED control bit is HIGH in the BCR, or is OFF if the bit is LOW. This control bit defaults to the HIGH state, and the LED can be used during initialization to indicate that the bus has accessed the board by turning the LED off.

SECTION 4.0

PRINCIPLES OF OPERATION

4.1 General Description

The CPCI6U64-24DSI20C500K contains 20 delta-sigma 24-Bit A/D converters and all supporting functions necessary for controlling critical acquisition parameters in a 20-Channel analog input module. A PLX^{tm} PCI9656 PCI interface adapter (Figure 4.1) provides the interface between the controlling PCI bus and an internal local controller through a 32-bit local bus. The local controller performs all internal configuration and data manipulation functions, including autocalibration. The PCI interface adapter supports universal 3V/5V PCI signalling, with D32/D64 and 33MHz/66MHz operation.

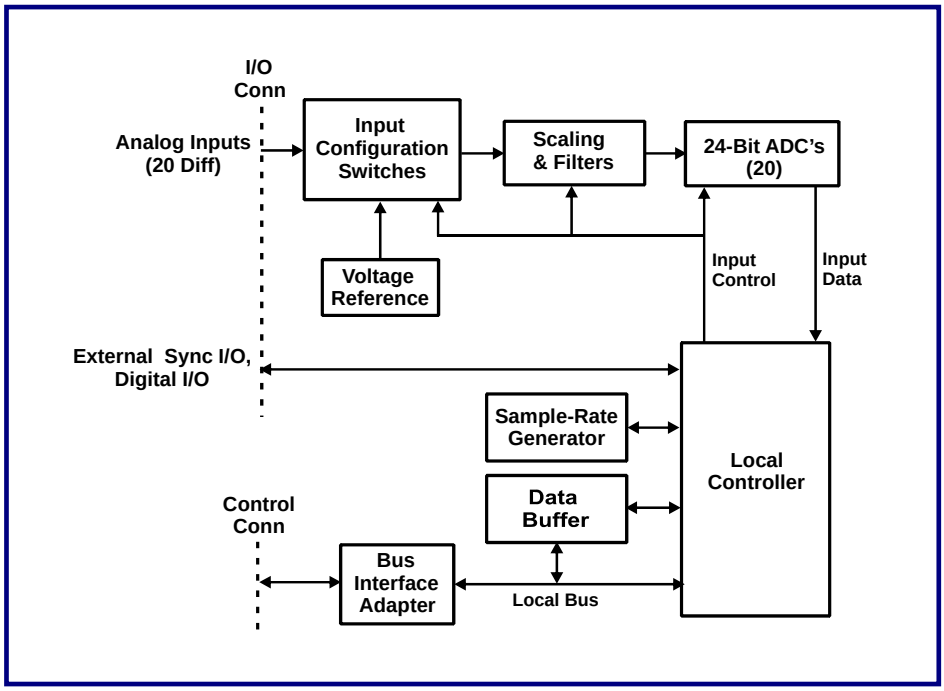

Figure 4.1. Functional Block Diagram

Input configuration switches allow the controller to select any of several signal sources as inputs to the ADC's. This feature is used to establish the internal connections necessary during autocalibration, and also permits verification from the PCI bus of the integrity of all analog input channels. All channels are calibrated against a single precision voltage reference. The offset and gain calibration of each input channel are adjusted with correction values that are determined during autocalibration.

4.2 Analog Inputs

The 20 analog input channels are arranged into two channel groups, with each group containing one-half of the channels present on the board. Either group can be designated as active or inactive, with only active groups sending input data to the data buffer. Analog-to-digital conversions can be performed on signals from any of several sources, which are selected by the input configuration switches shown in Figure 4.1. During normal operation, the analog input signal passes through a scaling differential amplifier which controls the input range, and which suppresses any common mode voltage that might be present. During selftest and autocalibration operations, the input configuration switches can be used to replace the system input signal with either a precision zero (ground) or a positive full-scale reference voltage.

Each ADC implements a sharp-cutoff lowpass digital image filter that has a bandwidth slightly less than one-half the sampling frequency. A characteristic of this filter (and of most digital filters) is a loss of attenuation at multiples of the ADC clocking frequency. Consequently, 'images' of any out-of-band signal components present in the input signal can occur at these frequencies and can be aliased into the passband as interference. For this reason, each input signal passes through a simple first-order lowpass analog filter that is designed to provide some suppression of any image components that might be present in the input signals.

The final conditioned and scaled input signal is digitized by each ADC into a 24-BIt serial data word that is deserialized into parallel format by the local controller. The local controller then attaches a channel tag to the data word, adjusts the reporting data resolution, and finally transfers the data to the input data buffer.

4.3 Autocalibration

Autocalibration is an embedded firmware utility that calibrates all input channels to a single internal voltage reference. The utility can be invoked at any time by the control software.

Correction values determined for each channel during autocalibration are stored in a pair of 16-Bit calibration DAC's that control the offset and gain for the channel.

The gain error of each channel is determined first, by measuring the response of each channel to both a zero input reference level and an internal positive fullscale voltage reference equal to 99.000 percent of the selected input voltage range. The resultant difference determines the gain correction facotor for the channel. The zero reference then is used to determine the offset error for the channel. The in-range value of the fullscale reference ensures that the ADC's will provide the nonsaturated, or in-range, responses that are necessary during the calibration adjustment process.

4.4 Sampling Clocks

An internal sample rate generator provides a frequency range of approximately 20-40 MHz, which is divided down by a software-specified integer to provide sample rates from 10-500 KSPS.

An external clock output can be assigned to replace the output of the internal rate generator, or can serve directly as the ADC sample clock. A board from which a rate generator or ADC sample clock originates is a *clock initiator*. Boards that receive and retransmit the external clock are *clock targets*. Multiple targets can be controlled from a single initiator.

4.5 Power Control

Regulated supply voltages of +5 Volts,and ±12 Volts are required by the analog networks. Multiple DC/DC converters in the power conditioner use +5V input power from the PCI bus to produce preregulated DC voltages that subsequently are postregulated with linear regulators to the required supply voltages. Linear regulators ensure that the final power voltages delivered to the analog networks are well-regulated and free of noise.

APPENDIX A

LOCAL REGISTER QUICK REFERENCE

APPENDIX A

LOCAL REGISTER QUICK REFERENCE

This appendix summarizes all local registers in the order in which they appear in Section 3.

Table 3.1. Control and Data Registers

Local Addr [1]	Designation	Access Mode [2]	Default	Primary Function	Ref
00	**Board Control (BCR)**	R/W	0008 3830h	Board Control Register (BCR)	3.2
04	**Rate Control-A**	R/W	0002 8019h	ADC frequency generator control integers Nref, Nvco.	3.6.2
08	**Digital I/O Port**	R/W	0000 0X0Xh	Bidirectional digital I/O port control	3.13
0C	**Clock-Source Assignments**	R/W	0000 0000h	ADC Clock source; Group disables.	3.6.1.2
10	**Rate Divisor**	R/W	0000 0001h	Sample rate divisor.	3.6.1.2
14	(Reserved)	R/W	0000 0000h	---	---
18	(Reserved)	RO	0000 0000h	---	---
1C	**Burst Block Size**	R/W	0000 0001h	Specifies the number of sample sets to be acquired in a triggered burst	3.12.1
20	**Buffer Control**	R/W	0007 FFFEh	Input buffer control and status	3.5.3
24	**Board Configuration**	RO	00XX XXXXh	Installed firmware and hardware options	3.10
28	**Buffer Size**	RO	000X XXXXh	Number of ADC values in the input buffer.	3.5.4
2C	Autocal Values [3]	R/W	---	---	---
30	**Input Data Buffer**	RO (DMA)	XXXX XXXXh	Input Data Buffer; Data and channel tag	3.5
34	(Reserved)	RO	0000 0000h	---	---
38	(Reserved)	RO	0000 0000h	---	---
3C	**Burst Trigger Timer**	R/W	0000 C350h	Internal trigger timer rate divisor	3.12.2
40-7C	(Reserved)	---	---	---	---

[1] Offsets from the PCI base address for local addressing.

[2] R/W = Read/Write; RO = Read-Only.

[3] Maintenance register; Shown for reference only

Table 3.2. Board Control Register

Offset: 0000h **Default: 0008 3830h**

Data Bit	Designation	Mode	Def	Function	Ref
D00-01	AIM[]	R/W	0h	Analog input mode. Selects system inputs or selftest mode. Defaults to system inputs.	3-4
D02-03	DRATE[]	R/W	0h	Selects oversampling ratio (OSR)	3.6.1.3
D04	OFFSET BINARY	R/W	1	Selects offset binary or two's complement input data format. Defaults HIGH to offset binary.	3.5.2.2
D05	INITIATOR OUTPUT	R/W	1	Selects INITIATOR or TARGET mode for external clock and sync output signals. Defaults HIGH to Initiator mode.	3.6.5
D06	SOFTWARE SYNC [1]	R/W	0	Initiates a local ADC sync operation when asserted. Also generates an external sync output if INITIATOR mode is selected. Clears automatically.	3.6.4, 3.6.5.2
D07	AUTOCAL [1]	R/W	0	Initiates an autocalibration operation when asserted. Clears automatically upon autocal completion.	3.7
D08	INTERRUPT A0	R/W	0h	Interrupt event selection. Default is zero.	3.8
D09	INTERRUPT A1	R/W			
D10	INTERRUPT A2	R/W			
D11	INTERRUPT REQUEST FLAG	R/W	1	Set HIGH when the board requests an interrupt. Clears the request when cleared LOW by the bus.	
D12	AUTOCAL PASS	RO	1	Set HIGH at reset or autocal initialization. Cleared LOW if autocalibration terminates unsuccessfully.	3.7
D13	CHANNELS READY	RO	1	LOW during any change in channel parameters. Asserted HIGH when inputs are ready to acquire data.	3.4.3
D14	BUFFER THRESHOLD FLAG	RO	0	Asserted HIGH when buffer contents exceed the assigned threshold.	3.5.3
D15	INITIALIZE [1]	R/W	0	Initializes the board when asserted. Sets all defaults.	3.3
D16	ENABLE TRIGGER TIMER	R/W	0	Enables the internal burst trigger timer.	3.12.2
D17	CLEAR BUFFER ON SYNC	R/W	0	Changes the context of the SOFTWARE SYNC to CLEAR BUFFER.	3.5.3.2
D18	RATE GEN EXT CLOCK OUT (Initiator Mode only)	R/W	0	When HIGH: Selects the internal rate generator as the external clock output source. When LOW: Selects the Group-00 sample clock. If Group-00 external clocking is selected, the output is driven by the internal rate generator and the Group-00 divisor.	3.6.5.1
D19	FRONT PANEL LED	R/W	1	Illuminates the front-panel LED when HIGH.	3.14
D20	TTL EXTERNAL SYNC I/O	R/W	0	Selects TTL external sync I/O configuration.	3.6.1.2
D21	ENABLE INPUT BURST	R/W	0	Selects triggered-burst acquisition when HIGH.	3.12
D22	S/W BURST TRIGGER	R/W	0	Initiates a triggered burst when asserted. Forced HIGH during any triggered burst.	3.12.1
D23-31	(Reserved)	RO	0h	---	---

[1] Clears automatically.

Table 3.4. Analog Input Function Selection

AIM[..0]	Function or Mode
0	Differential analog input mode.
1	(Reserved).
2	ZERO test. Internal ground reference is connected to all analog input channels.
3	+VREF test. Internal voltage reference is connected to all analog input channels.

Table 3.5.2. Input Data Buffer Organization

Offset: 0000 0030h **Default: XXXX XXXXh**

Selected Data Width	Reserved (Zero)	Channel Tag	Zero-Pad	Channel Data Value
16 Bits	D[31..29]	D[28..24]	D[23..16]	D[15..0]
18 Bits	D[31..29]	D[28..24]	D[23..18]	D[17..0]
20 Bits	D[31..29]	D[28..24]	D[23..20]	D[19..0]
24 Bits	D[31..29]	D[28..24]	---	D[23..0]

Table 3.5.2.2. Analog Input Data Coding; 16-Bit Data Field

	DIGITAL VALUE (Hex)	
ANALOG INPUT LEVEL	OFFSET BINARY	TWO'S COMPLEMENT
Positive Full Scale minus 1 LSB	FFFFh	7FFFh
Zero plus 1 LSB	8001h	0001h
Zero	8000h	0000h
Zero minus 1 LSB	7FFFh	FFFFh
Negative Full Scale plus 1 LSB	0001h	8001h
Negative Full Scale	0000h	8000h

Table 3.5.3. Buffer Control Register

Offset: 0000 0020h **Default: 0007 FFFEh**

Bit Field	Mode	Designation	Def	Function
D00-D19	R/W	BUFFER THRESHOLD	0007 FFFEh	Buffer Flag Threshold
D20	R/W	ENABLE BUFFER INPUT	0	Enables ADC inputs to the buffer.
D21	R/W	CLEAR BUFFER [1]	0	Clears (empties) the buffer. Asserted HIGH while the buffer is cleared, either locally or externally.
D22-D23	R/W	DATA WIDTH	0	Controls the width of the buffer data field: 0 => 16 bits 1 => 18 bits 2 => 20 bits 3 => 24 bits.
D24	R/W	DISABLE CHANNEL TAG	0	Replaces the channel tag with a zero-field.
D25	R/W	BUFFER OVERFLOW [2]	0	Reports buffer overflow (Write on full)
D26	R/W	BUFFER UNDERFLOW [2]	0	Reports buffer underflow (Read on empty)
D27-D31	RO	(Reserved)	0h	---

[1] Clears automatically. [2] Cleared by writing LOW, or by Initialization.

Table 3.6.1.1. Channel Groups

CHANNEL GROUP	20-CHAN BOARD	12-CHAN BOARD	8-CHAN BOARD	4-CHAN BOARD
0	Channels 00-09	00-05	00-03	00, 01
1	Channels 10-19	06-11	04-07	02, 03

Table 3.6.1.2-1. Clock-Source Assignments Register

Offset: 0000 000Ch **Default: 0000 0000h**

BIT FIELD	DESIGNATION	CHANNEL GROUP
D[03..00]	GROUP 0 CLOCK SOURCE	0
D[07..04]	GROUP 1 CLOCK SOURCE	1
D[31..08]	(Reserved)	---

Table 3.6.1.2-2. Clock-Source Assignment Codes

ASSIGNMENT CODE	GROUP 0 ASSIGNMENT	GROUP 1 ASSIGNMENT
0	Internal Rate Generator *	No effect. (Same as Group-0)
1-3	(Reserved)	
4	External Sample Clock (as rate generator input)	
5	Direct External Sample Clock (routed directly to ADC)	
6	**Disabled**	**Disabled**
7-15	(Reserved)	(Reserved)

* Applies to both channel groups. Disabling Group-0 disables both groups.

Table 3.6.1.3-1. Oversampling Modes

DRATE[]	Oversampling Ratio	Sample Rate Range
0	x256	9.766 KSPS -78.125 KSPS
1	x128	78.125 KSPS - 156.250 KSPS
2	x64	156.250 KSPS - 312,500 KSPS
3	x32	312,500 KSPS - 500,000 KSPS

Table 3.6.1.3-2. Rate Divisor Register

Offset: 0000 0010h **Default: 0000 0001h**

Bit Field	Designation	Function
D[08..00]	RATE DIVISOR (**Ndiv)**	Scales the rate generator input frequency.
D[31..9]	(Reserved)	---

Table 3.6.2-1. Rate Generator Control Register (Rate Control-A)

Offset: 0004h **Default: 0002 8019h**

Bit Field	Designation	Function
D[11..00]	VCO FACTOR **(Nvco)**	PLL VCO factor; 25-300.
D[23..12]	REF FACTOR **(Nref)**	PLL Reference factor; 25-300.
D[31..24]	(Reserved)	---

* For maximum phase stability, select the lowest possible values for Nvco and Nref.

Table 3.6.2-2. Sample-Rate Control Parameters

Parameter	Notation	Valid Range
Sample Rate	**Fsamp**	9.76 - 500 KSPS
Oversampling Ratio *	**OSR**	256, 128, 64 or 32
Reference Frequency	**Fref**	32.768 MHz, Fixed
Rate Divisor	**Ndiv**	1-4
Osc VCO integer	**Nvco**	25-300
Osc Reference integer	**Nref**	25-300
Osc Integer Ratio	**Nvco/Nref**	0.61 - 1.22

* Selected by Drate[] in the BCR.

Table 3.6.2-3. Sample Rate Examples

Sample Rate (KSPS)	Nvco	Nref	Fgen (Mhz)	OSR	DRATE[]	Ndiv
10.000	25	40	20.48000	256	0	4
20.000	30	32	30.72000	256	0	3
40.000	25	40	20.48000	256	0	1
80.000	25	40	20.48000	128	1	1
100.000	25	32	25.60000	128	1	1
300.000	75	64	38.40000	64	2	1
327.680	32	50	20.97152	32	3	1
500.000	125	128	32.00000	32	3	1

Fref = 32.768MHz. All values shown in decimal format.

Table 3.8.1. Interrupt Event Selection

Interrupt A[2:0]	Interrupt Event Condition
0	Initialization completed. Default state.
1	Autocal completed
2	Channels Ready; LOW-to-HIGH transition
3	Data Buffer threshold flag, LOW-to-HIGH transition
4	Data Buffer threshold flag, HIGH-to-LOW transition
5	Triggered Burst Completed
6	(Reserved)
7	(Reserved)

Table 3.9.1. Typical DMA Register Configuration; Block Mode

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial (constant) local address of buffer	0000 0030h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

* Determined by specific transfer requirements.

Table 3.9.2. Typical DMA Register Configuration; Demand Mode

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32)	0002 1943h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial (constant) local address of buffer	0000 0030h
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

* Determined by specific transfer requirements.

Table 3.10. Board Configuration Register

Offset: 0000 0024h **Default: 00XX XXXXh**

BIT FIELD	DESCRIPTION
D00-D11	Firmware Revision
D12-D15	(Reserved status flags).
D16-D18	Number of input channels: 0 => 20 Channels 1 => 12 Channels 2 => 8 Channels 3 => 4 Channels 4-7 => (Reserved)
D19-D20	Image Filter Frequency: 0 => 2.0MHz, first order. 1 => No filter. 2-3 => (Reserved)
D21-22	Input Range: 0 => ±6V 1 => ±10V 2 => ±5V 3 => ±2.5V
D23-D31	(Reserved)

Table 3.12.2. Trigger Rate Divisor Register

Offset: 0000 003Ch **Default: 0000 C350h**

BIT FIELD:	DESIGNATION	FUNCTION
D[23..00]	TRIGGER RATE DIVISOR	Rate divisor for internally timed triggered bursts.
D[31..24]	(Reserved)	---

Table 3.13. Digital I/O Port Register

Offset: 0008h **Default: 0000 0X0Xh**

DATA BIT	MODE*	DESIGNATION	DEFAULT	DESCRIPTION
D00	RW	DIO 00 DATA	X	Digital I/O Data; Bits 00-03
D01	RW	DIO 01 DATA	X	
D02	RW	DIO 02 DATA	X	
D03	RW	DIO 03 DATA	X	
D04-D06	RW	(Reserved)	0h	---
D07	R/W	DIO 00_03 OUTPUT	0	DATA 00-03 direction control; High for output.
D08	RW	DIO 04 DATA	X	Digital I/O Data; Bits 04-07
D09	RW	DIO 05 DATA	X	
D10	RW	DIO 06 DATA	X	
D11	RW	DIO 07 DATA	X	
D12-D14	RW	(Reserved)	0h	---
D15	RW	DIO 04_07 OUTPUT	0	DATA 04-07 direction control; High for output.
D16-D31	RO	(Reserved)	0h	Read back as all-zero.

APPENDIX B

Migration From PMC66-24DSI16WRC

Appendix B

Migration From PMC66-24DSI16WRC

Operation of the CPCI6U64-24DSI20C500K is similar to that of the PMC66-24DSI16WRC. This appendix summarizes the principal similarities and differences between the two products, and is provided as a general guide rather than a definitive list of requirements or changes.

B.1. Comparison of Features

Table B.1 summarizes principal PMC-24DSI12 and CPCI6U64-24DSI20C500K features.

Table B.1. PMC66-24DSI16WRC, CPCI6U64-24DSI20C500K Features Comparison

Feature	PMC66-24DSI16WRC	CPCI6U64-24DSI20C500K
Form Factor	**Single-width PMC**	**6U Compact PCI**
Number of Input Channels	**16**	**20**
Input Ranges	**±10V, ±1.0V, ±100mV, ±10mV**	**±6V**
Sample Rate Range	**0.2 KSPS to 105 KSPS**	**10 KSPS to 500 KSPS**
Data Buffer	**256 K-Sample FIFO**	**512 K-Sample FIFO**
PCI Interface	**PCI 2.3; D32; 33MHz/66MHz**	**PCI 2.3; D32/D64, 33MHz/66MHz**
Master Clock Frequency	**40.000 MHz**	**50.000 MHz**
Adjustable Internal clocks	**1**	**1**
Master Clock Freq Fine-Adjust	**Yes**	**Provisional (Not implemented)**
External clock and sync I/O	**LVDS, TTL, Front-panel and Internal**	**LVDS, TTL, Front-panel**
Triggered-Burst Sampling	**Yes**	**Yes**
Digital I/O	**Yes**	**Yes**
Native Resolution	24 Bits	
Native Input Configuration	Differential	
Input Impedance	High (1-2 Megohms)	
Buffer DMA Access	Block and Demand Mode DMA	
Autocalibration	On-demand	

B.2. Migration Issues

Section 2.2. Installation:

I/O pin assignments have changed.

Table 3.1. Control and Data Registers

The 'Auxiliary Sync I/O Control' and 'Master Clock Adjust' control registers are deleted.
Default values have changed.

Table 3.2: Board Control Register:

The RANGE[] field is replaced with a DRATE[] field.
The 'High Speed ADC Mode' control bit is reassigned as 'Front Panel LED'

Table 3.3.2: Initialization:

The default sample rate is changed from 10KSPS to 20KSPS. Associated control fields are adjusted accordingly.

Table 3.5.2. Input Data Buffer Organization:

The width of the channel tag field is increased from four bits to five.

Table 3.5.3. Buffer Control Register:

The width of the Buffer Threshold field is increased from 19 bits to 20.

Table 3.6.1. Sample Rate Control

Sample-rate calculations are modified to accommodate the ads1672 ADC.

Section 3.12 Auxiliary External Clock and Sync

Function deleted. Replaced with 'Burst Sampling' function**.**

Section 3.13 Master Clock Adjustment

Function deleted. Replaced with 'Digital I/O Port' function.

Sections 3.14 and 3.15:

Relocated to Sections 3.12 and 3.13.

Revision History:

03-07-2011: Origination as preliminary draft.

04-27-2011: Table 3.13: Corrected default value.

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